A 512kb 8T SRAM Macro Operating Down to 0.57V with an AC-Coupled Sense Amplifier and Embedded Data-Retention-Voltage Sensor in 45nm SOI CMOS

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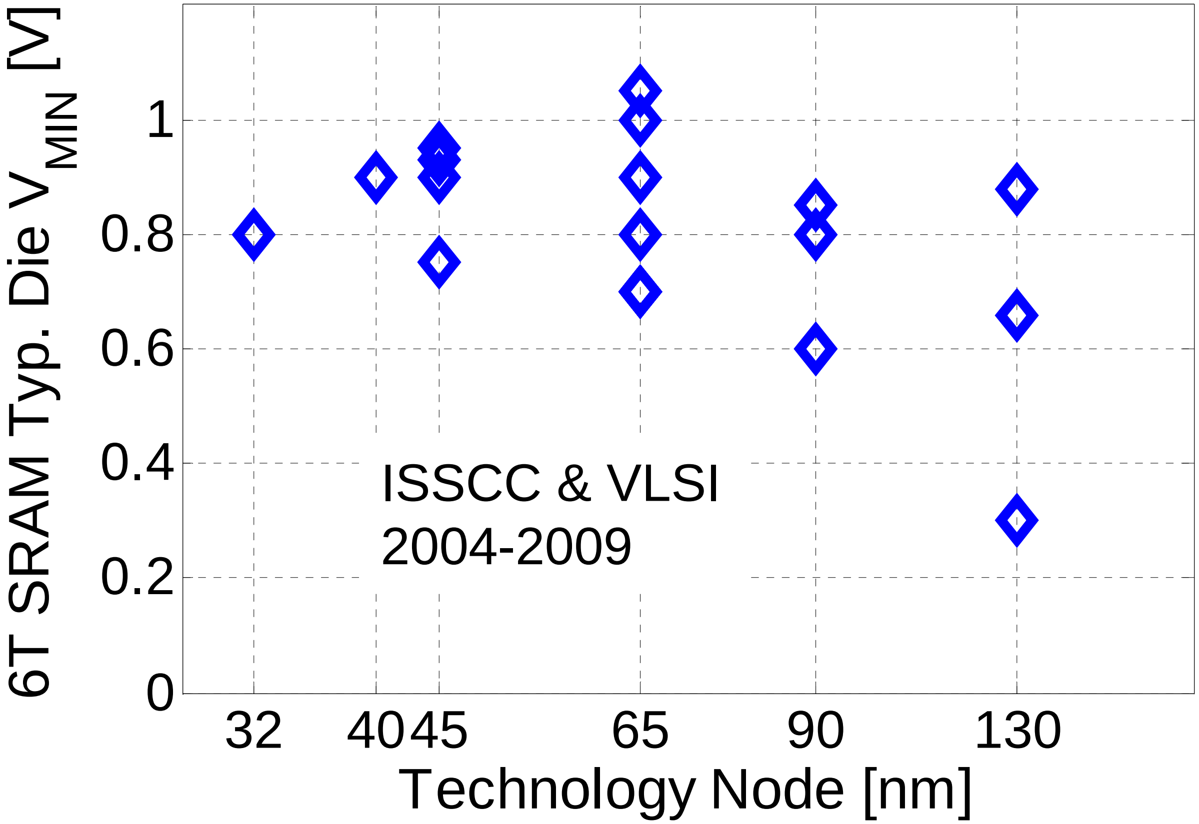
CMOS Voltage Scaling



- **Need**: A memory compatible with the limits of static CMOS logic
- **Solution**: A voltage scalable, single-supply, 8T SRAM with no dynamic assists that minimizes area and standby power

Features of This Work

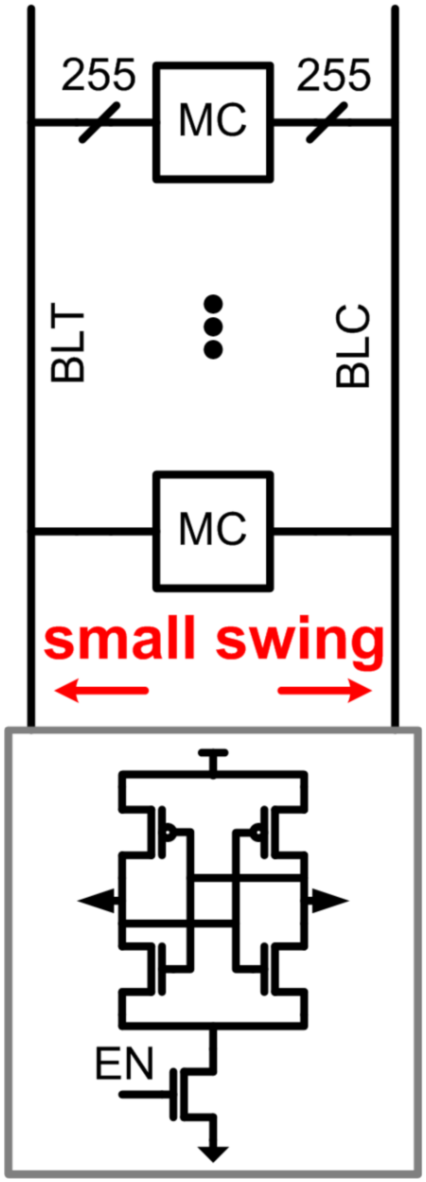
- AC-Coupled Sense Amplifier (ACSA)
- Regenerative Global Bitline Scheme
- Data-Retention-Voltage Sensor

Sensing Approaches

CONVENTIONAL TECHNIQUES

THIS WORK

128 to 256 ROWS



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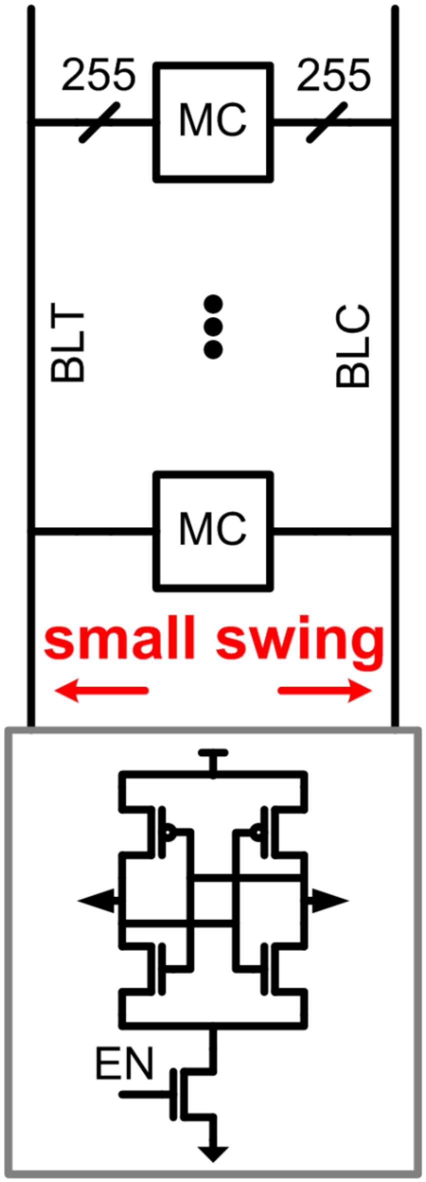
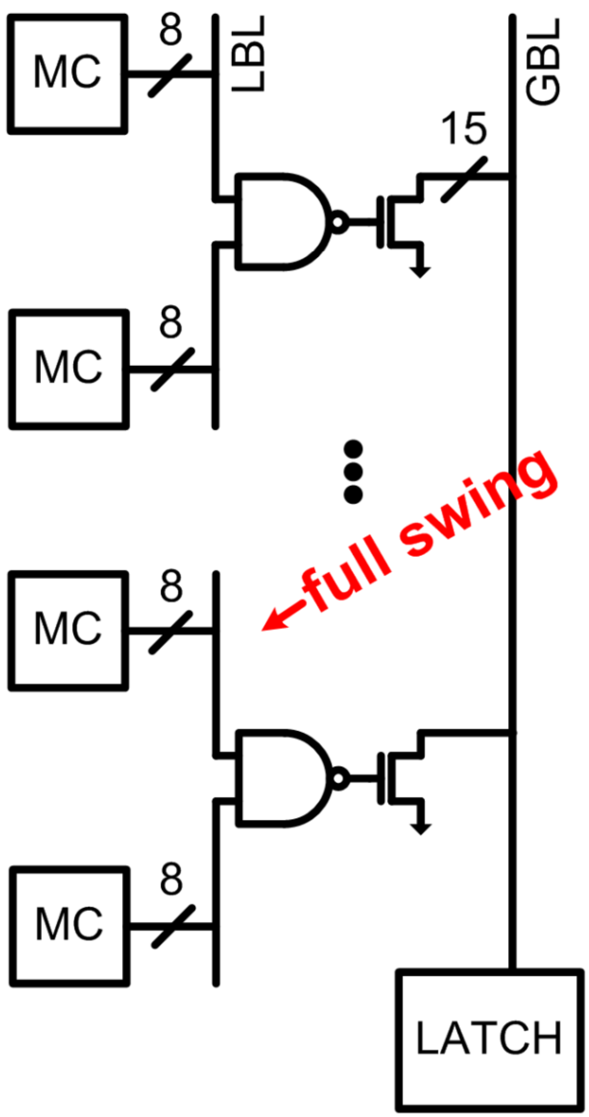


128 to 512 ROWS



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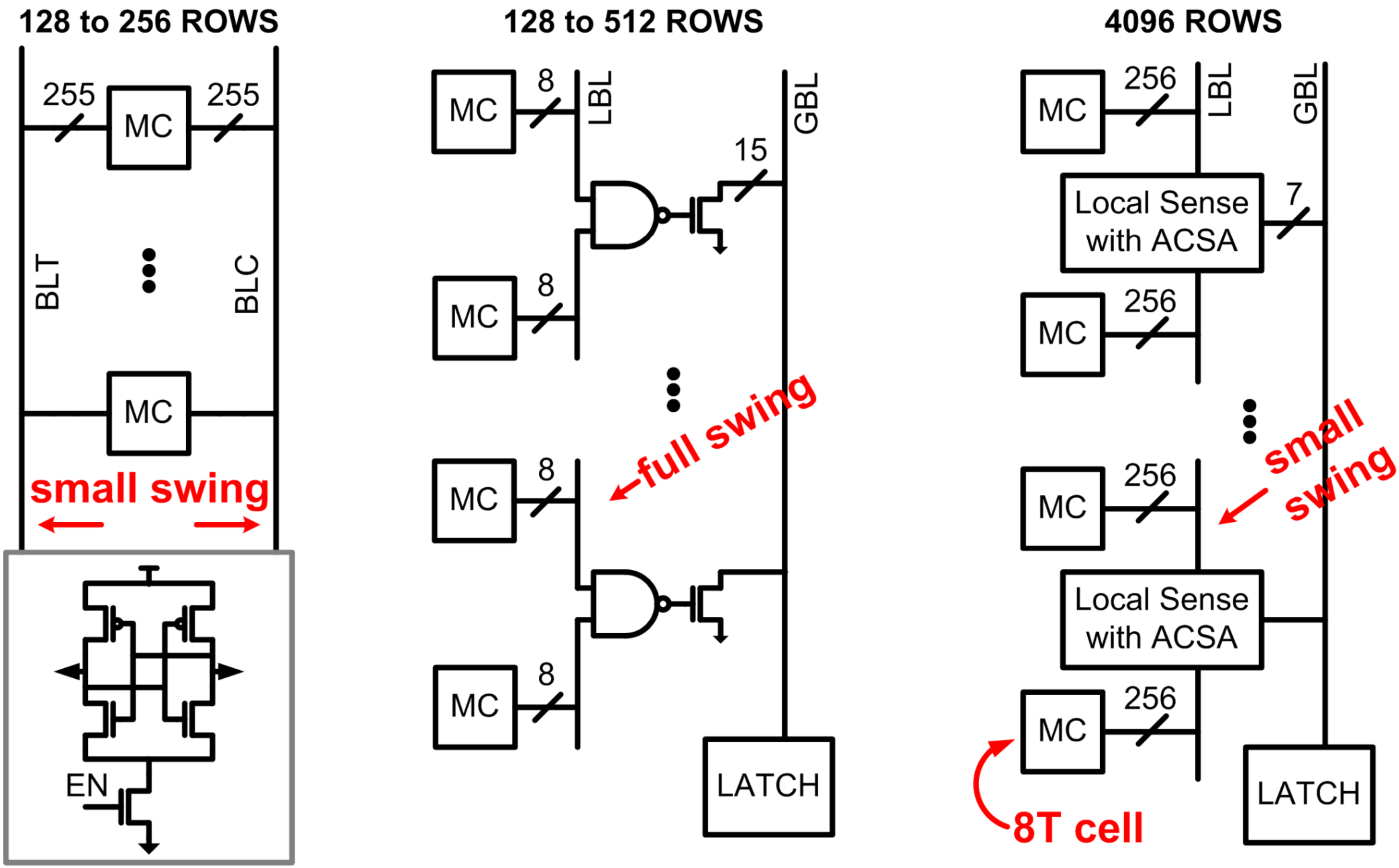
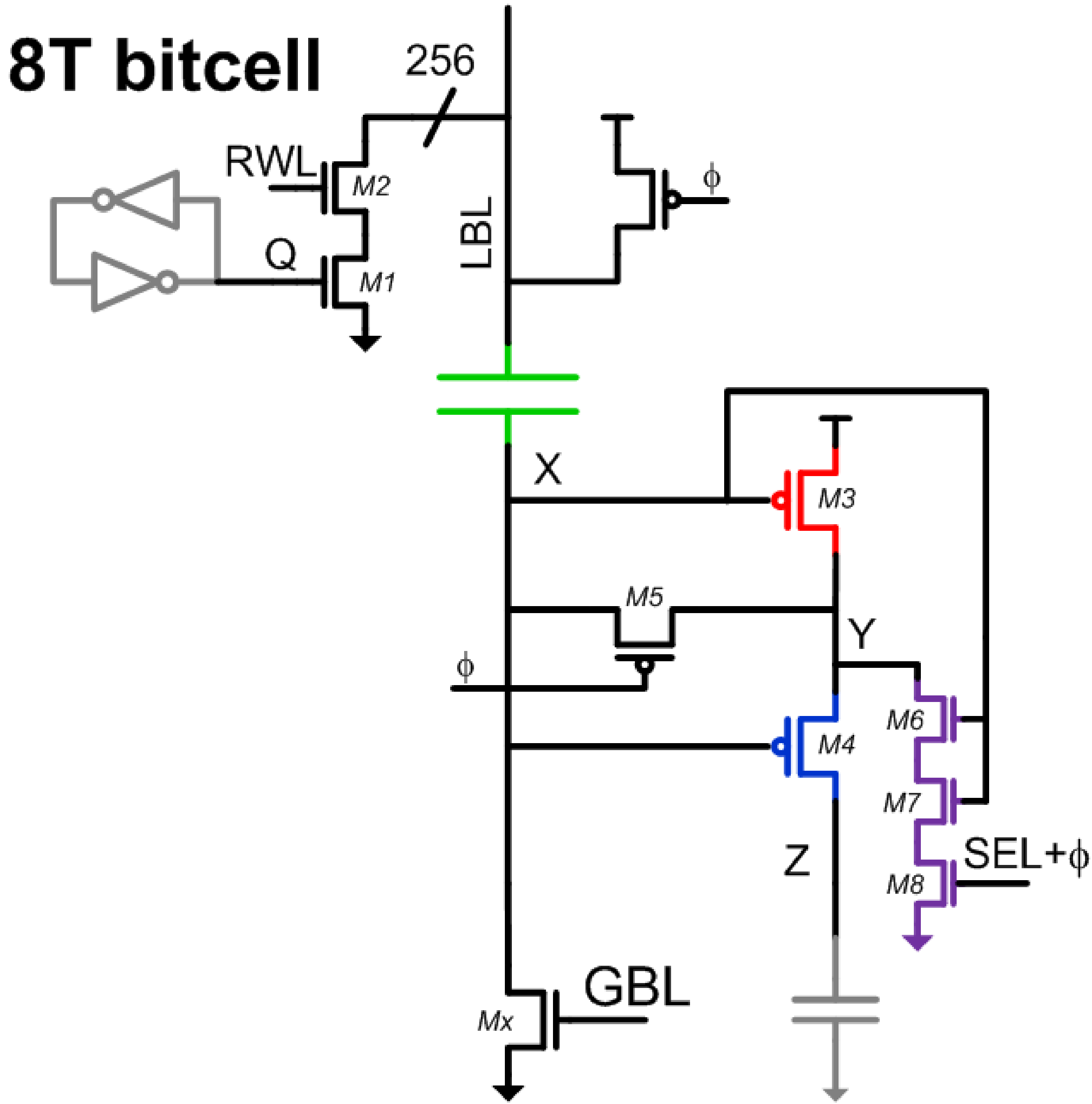


AC Coupled Sense Amplifier (ACSA)



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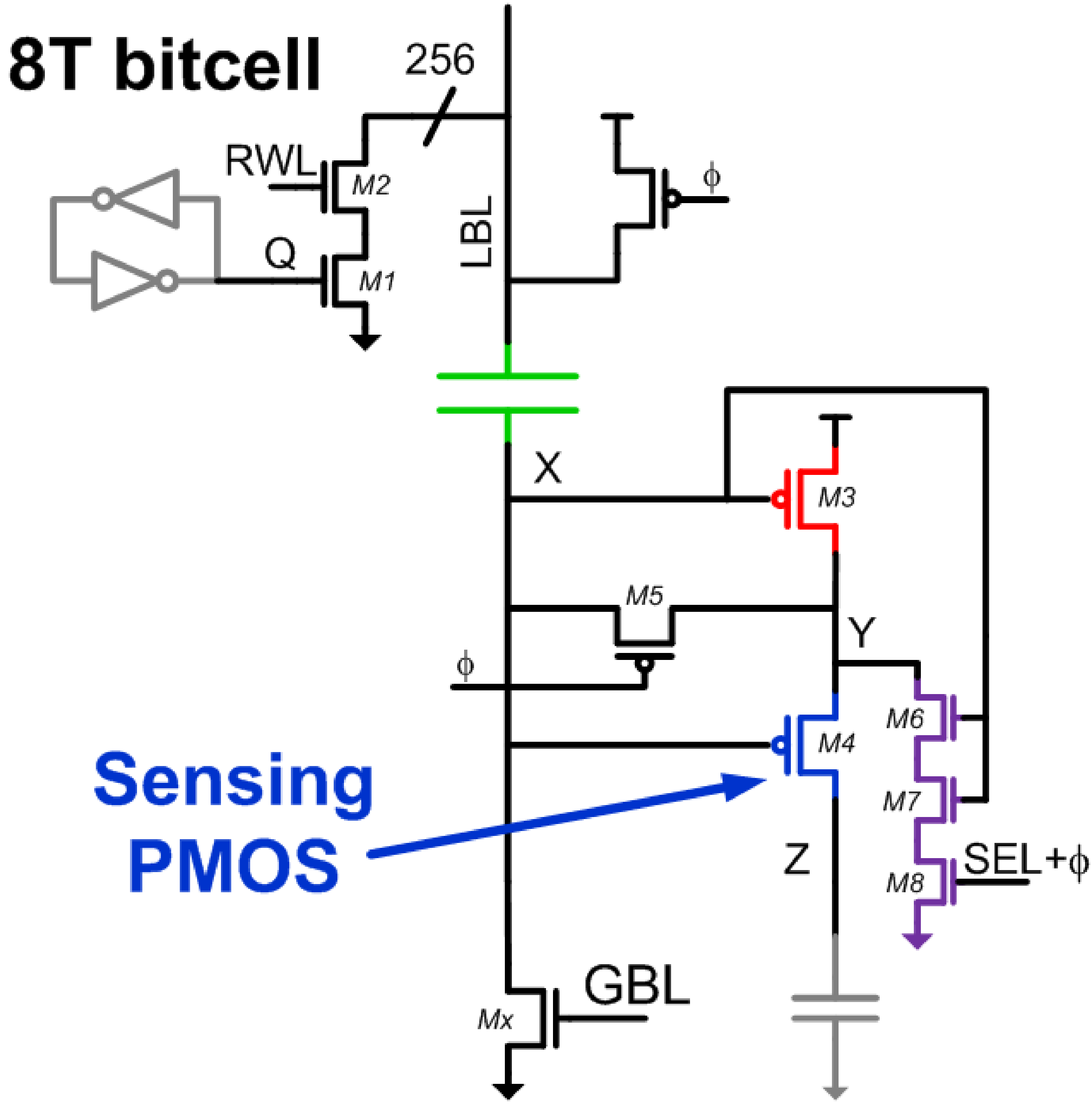

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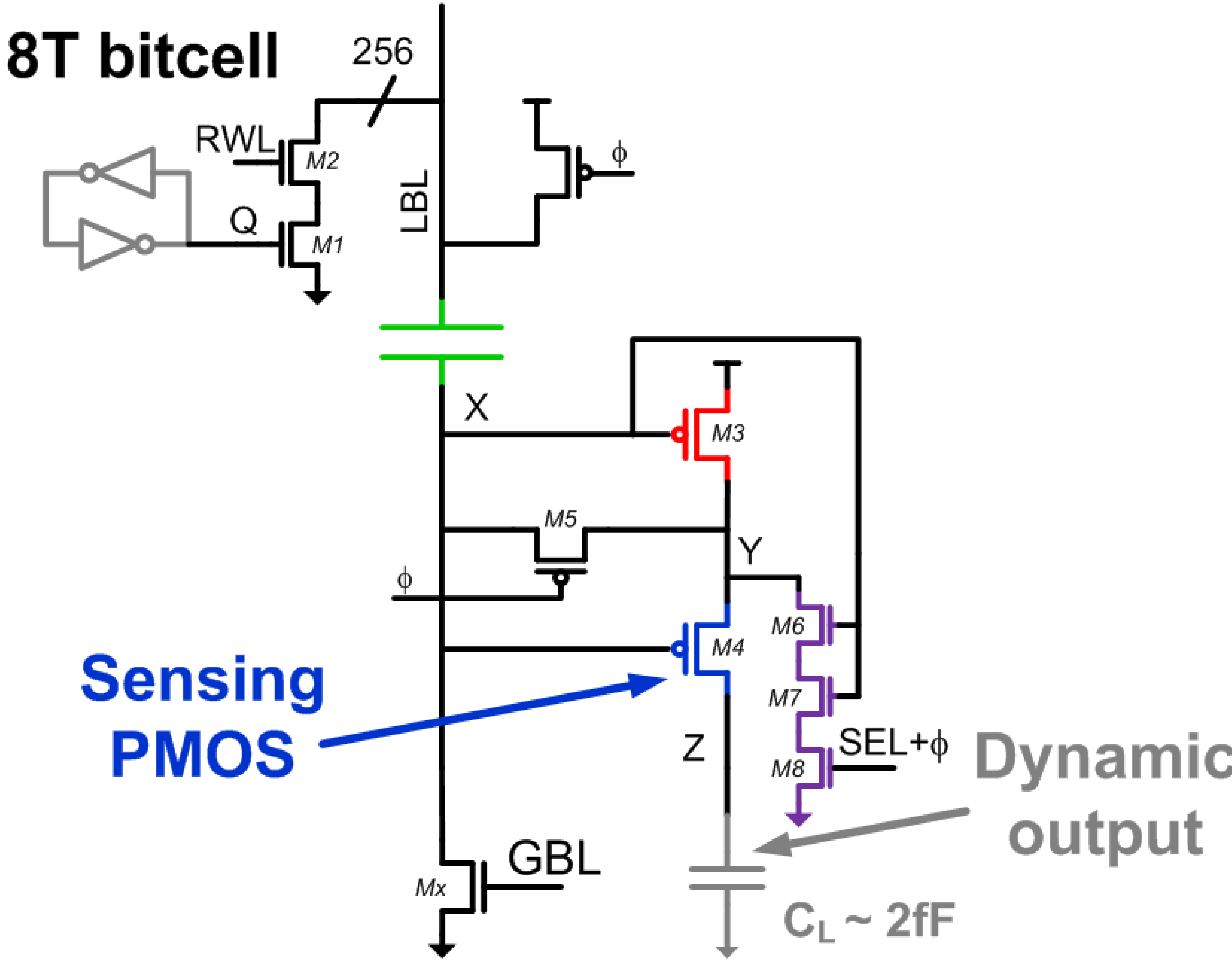

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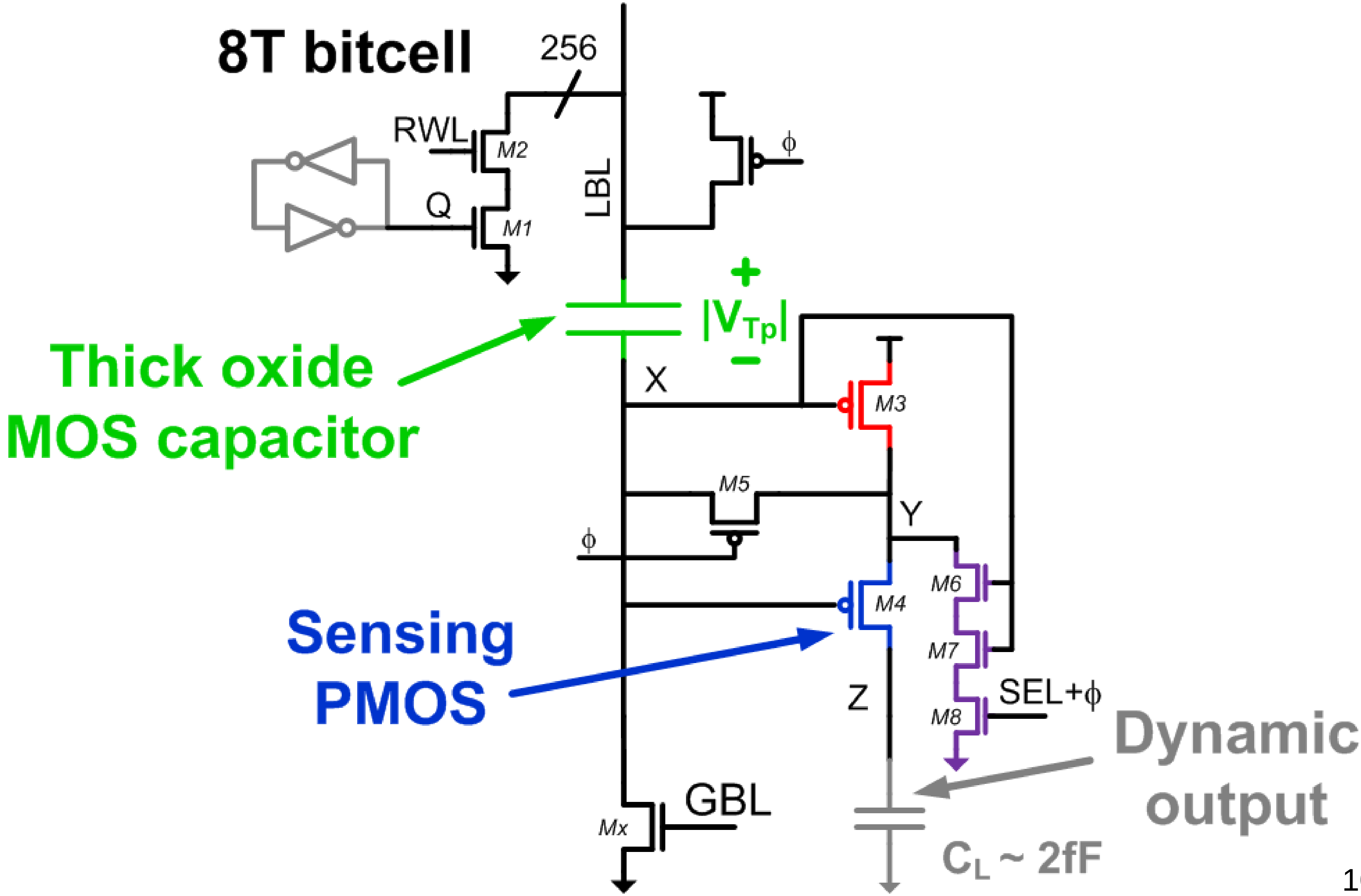

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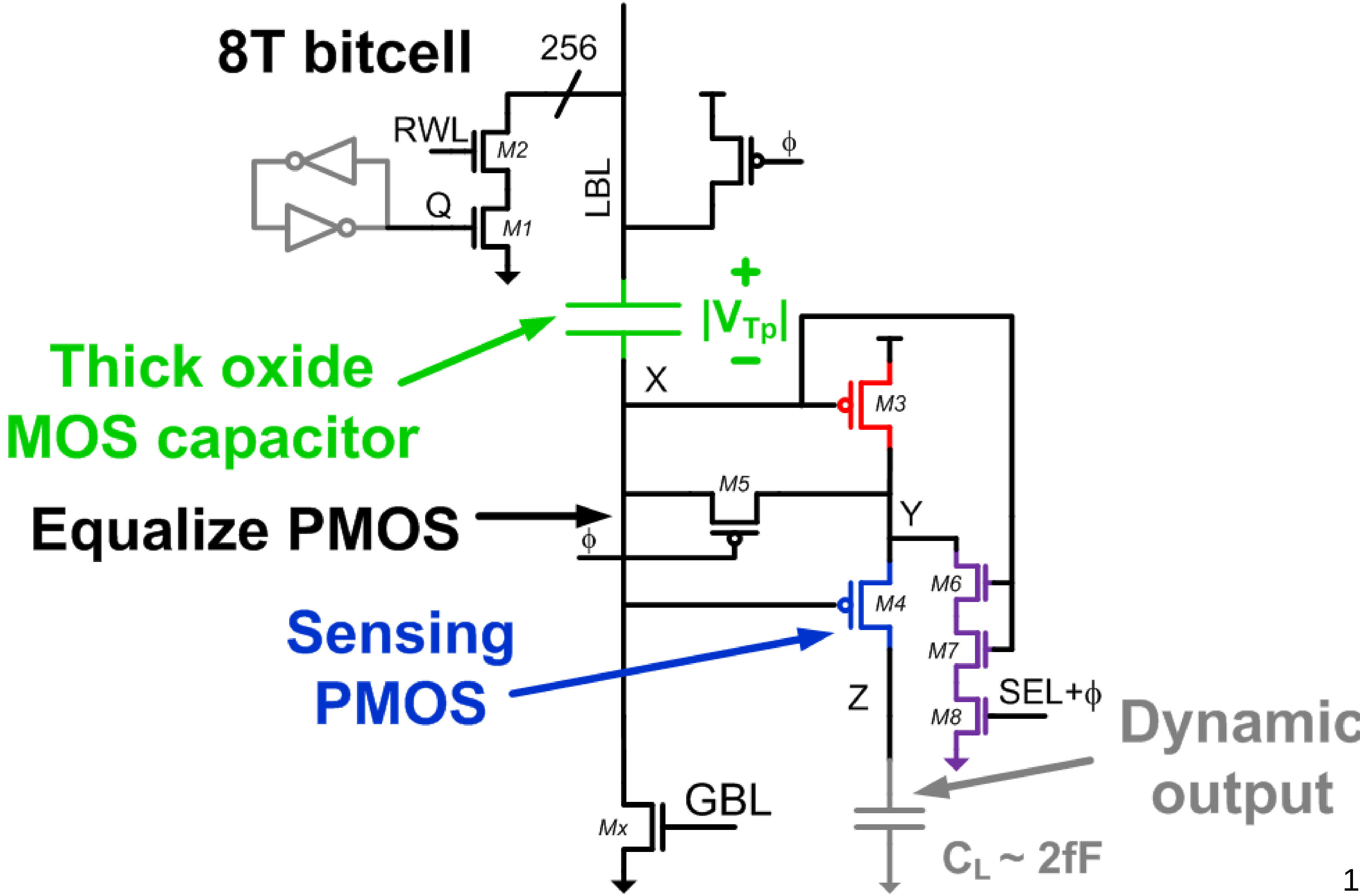

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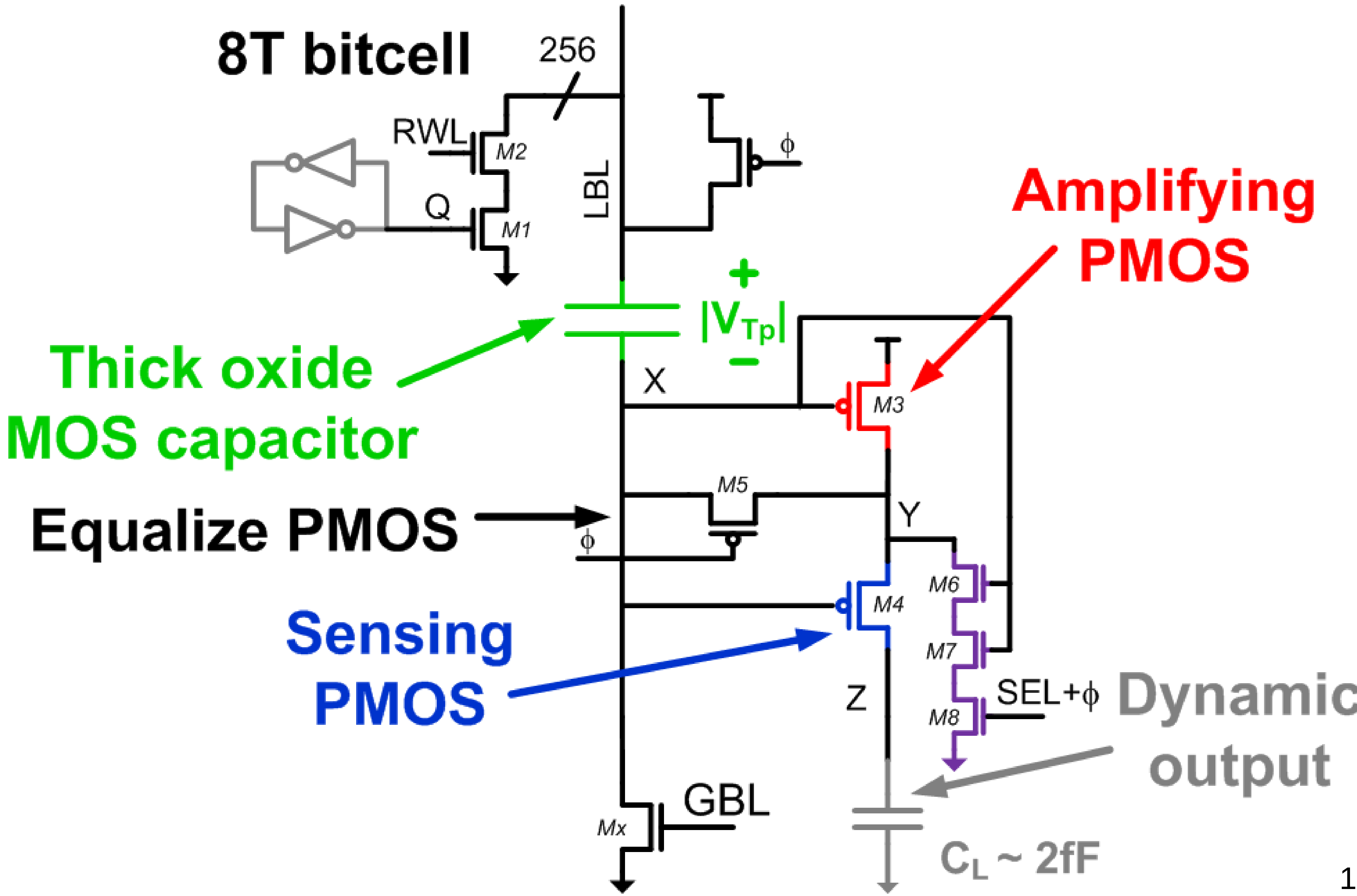

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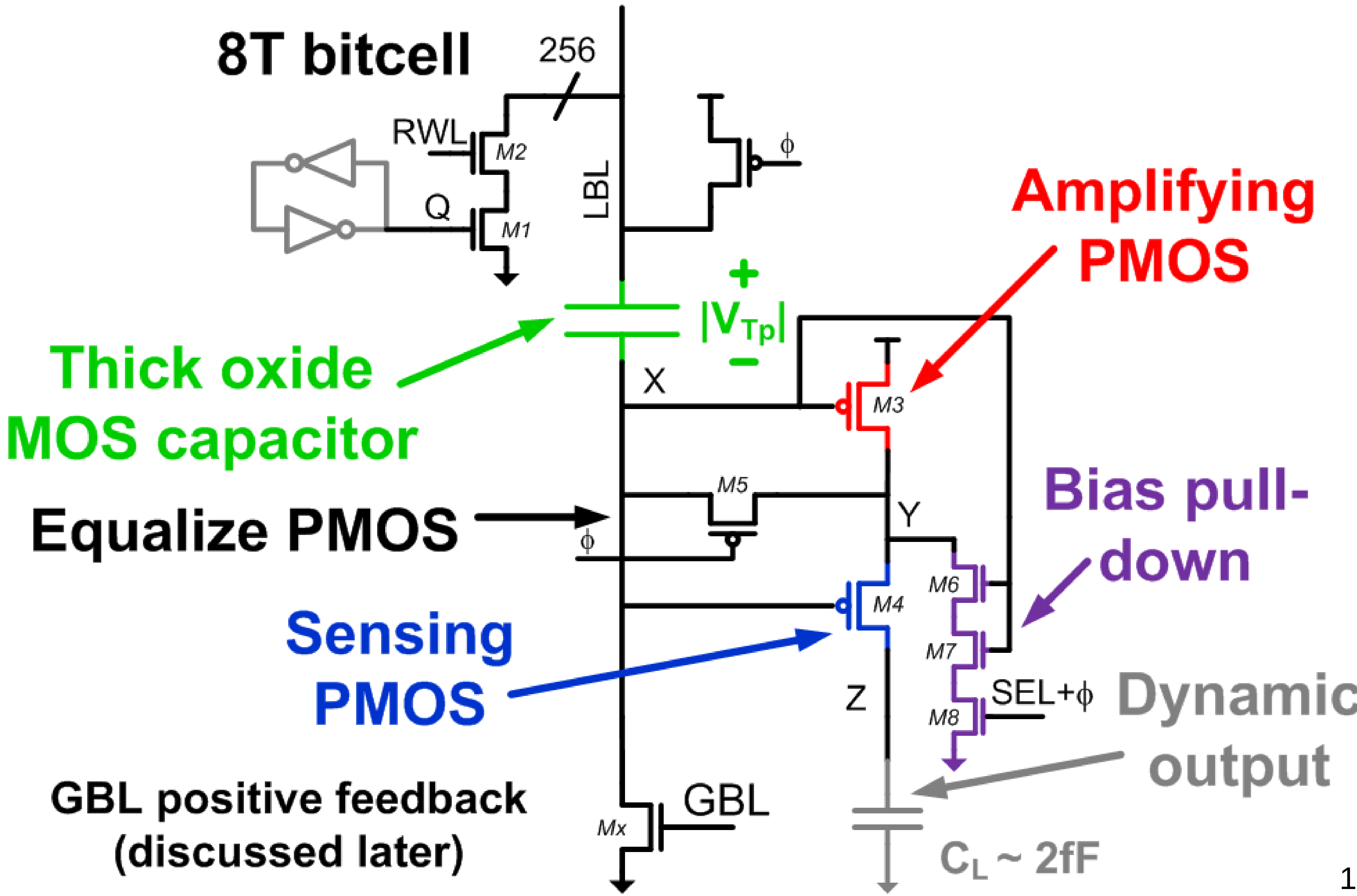
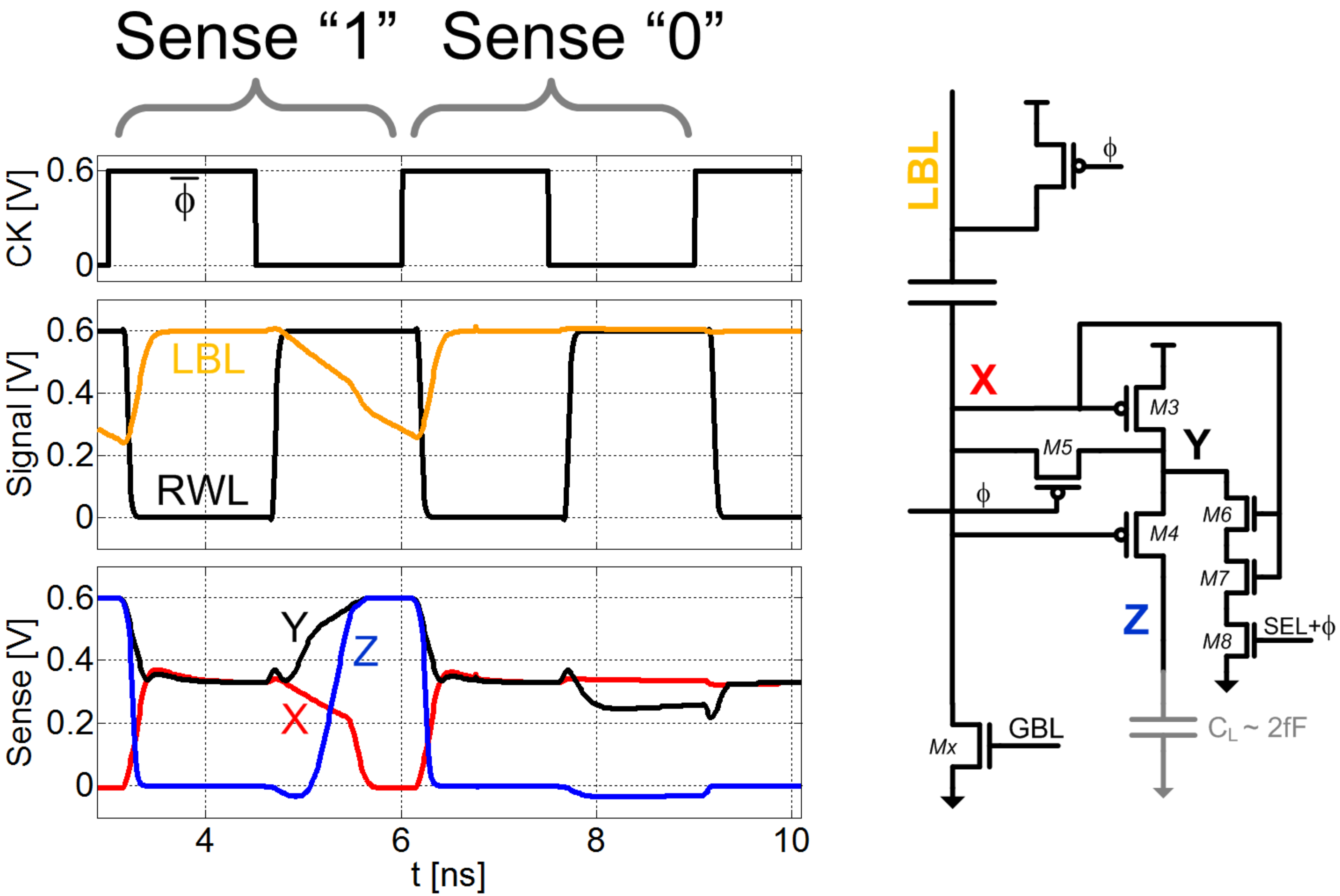
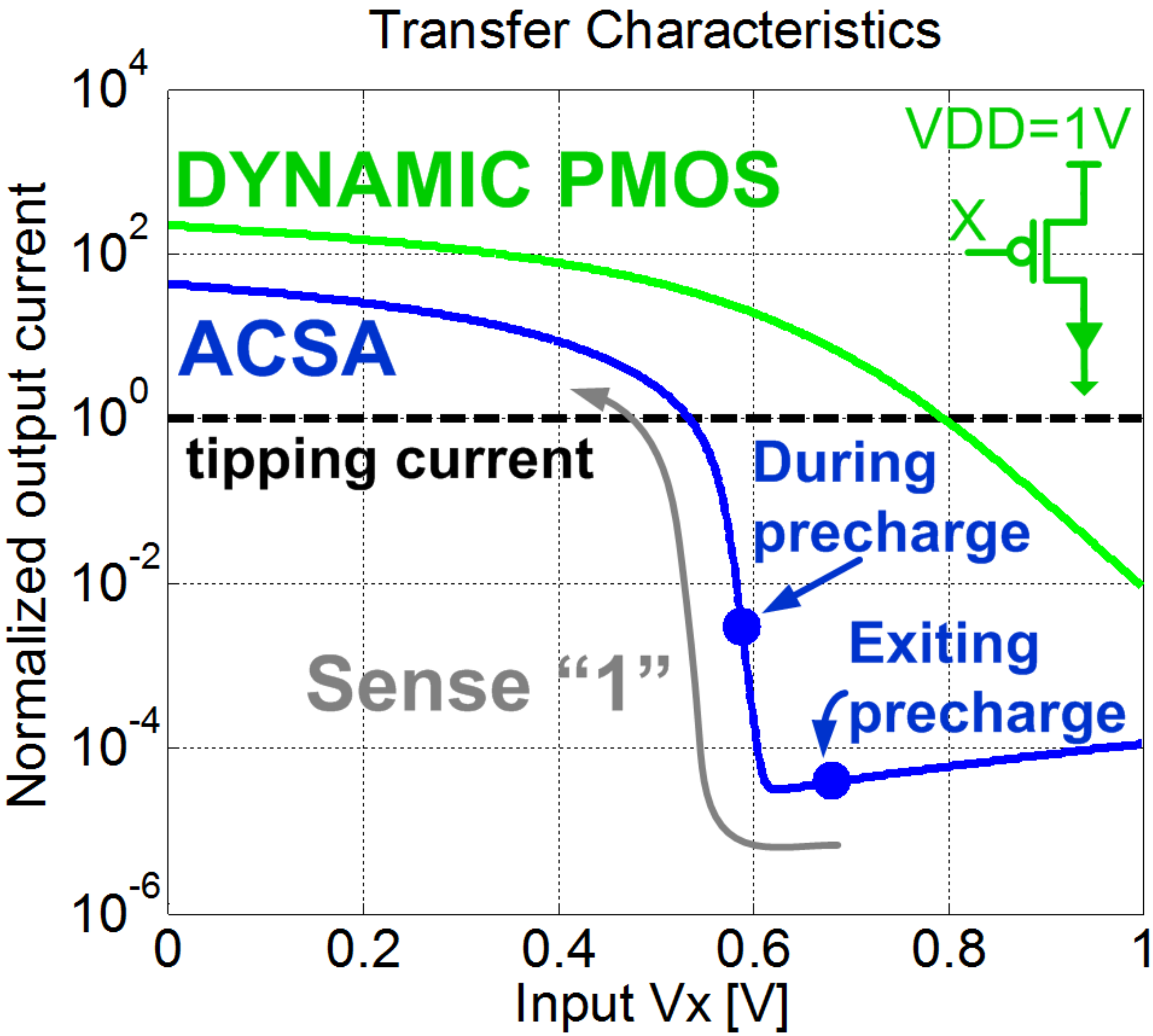
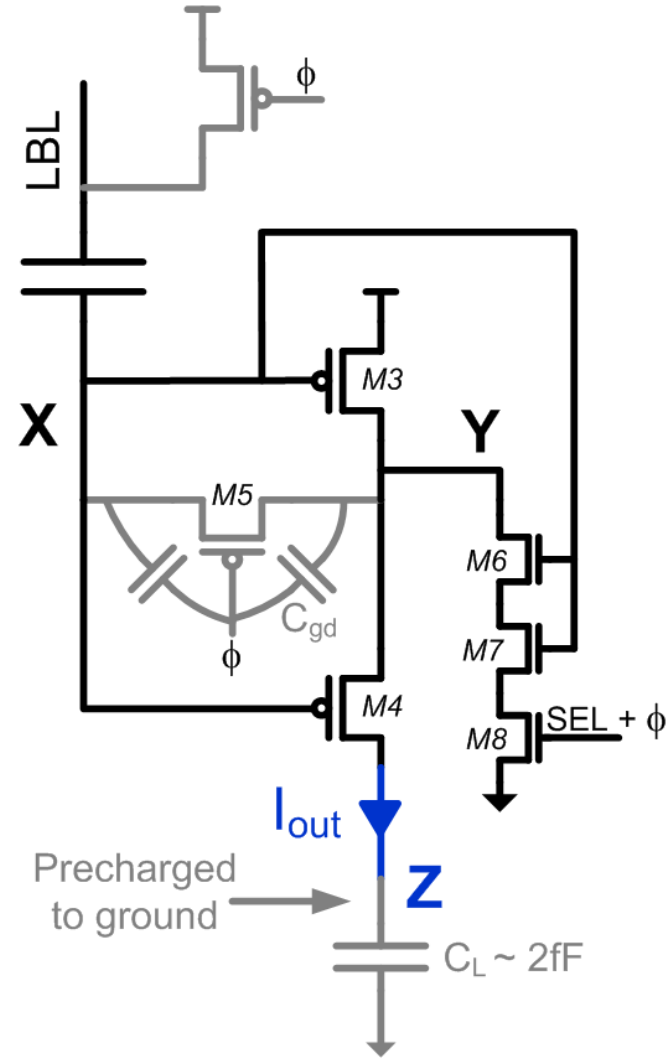


ACSA Operation



ACSA Output Current

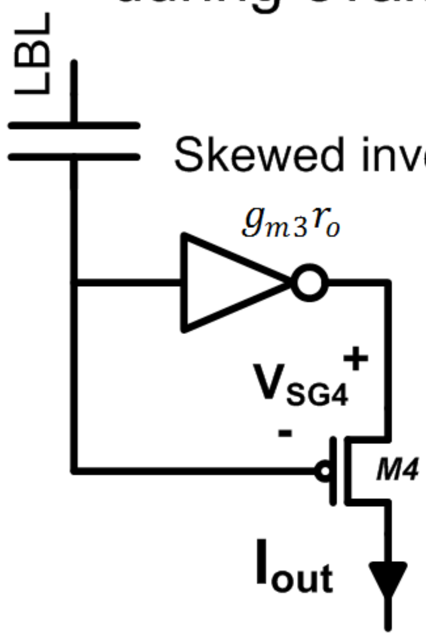




Steep cutoff of PMOS stack M3-M4 distinguishes "1" and "0"

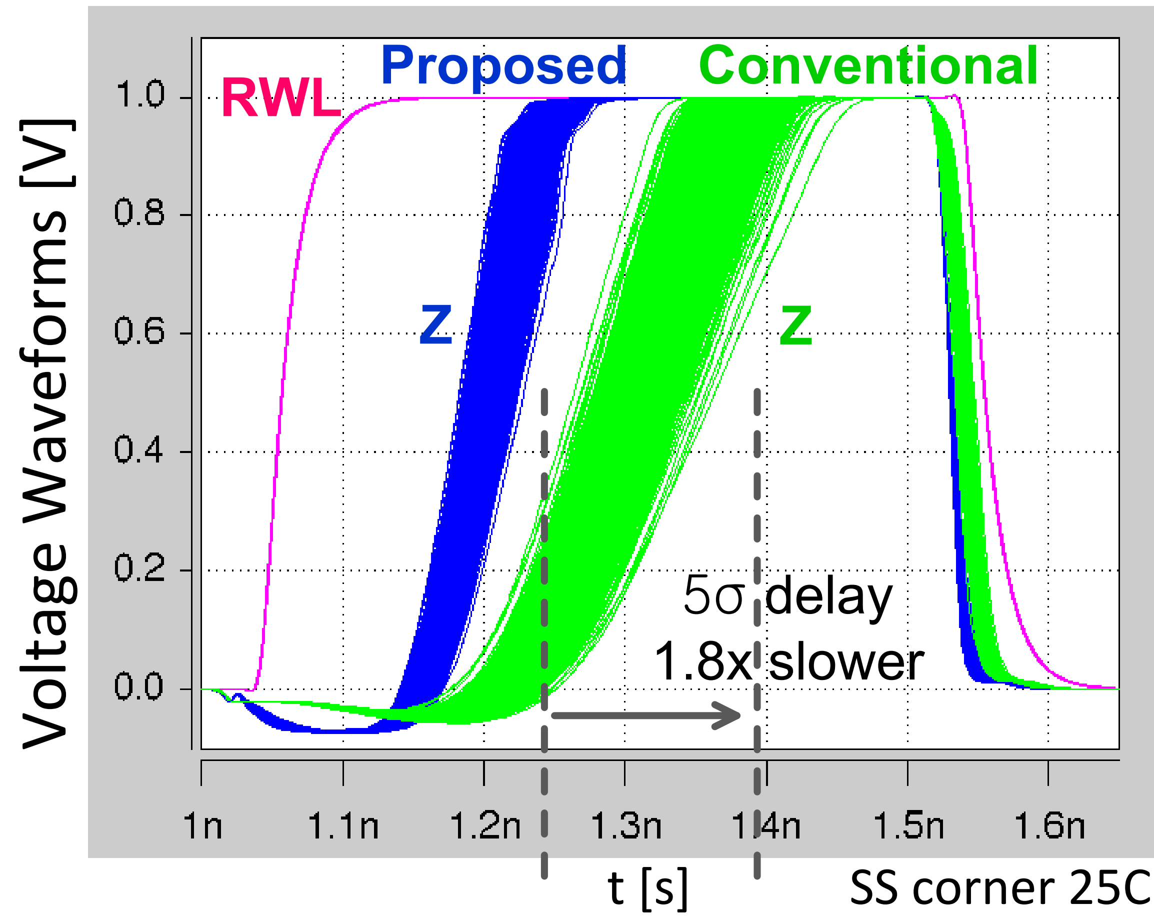
Offset Compensation Reduces Delay

Simplified schematic
during evaluation



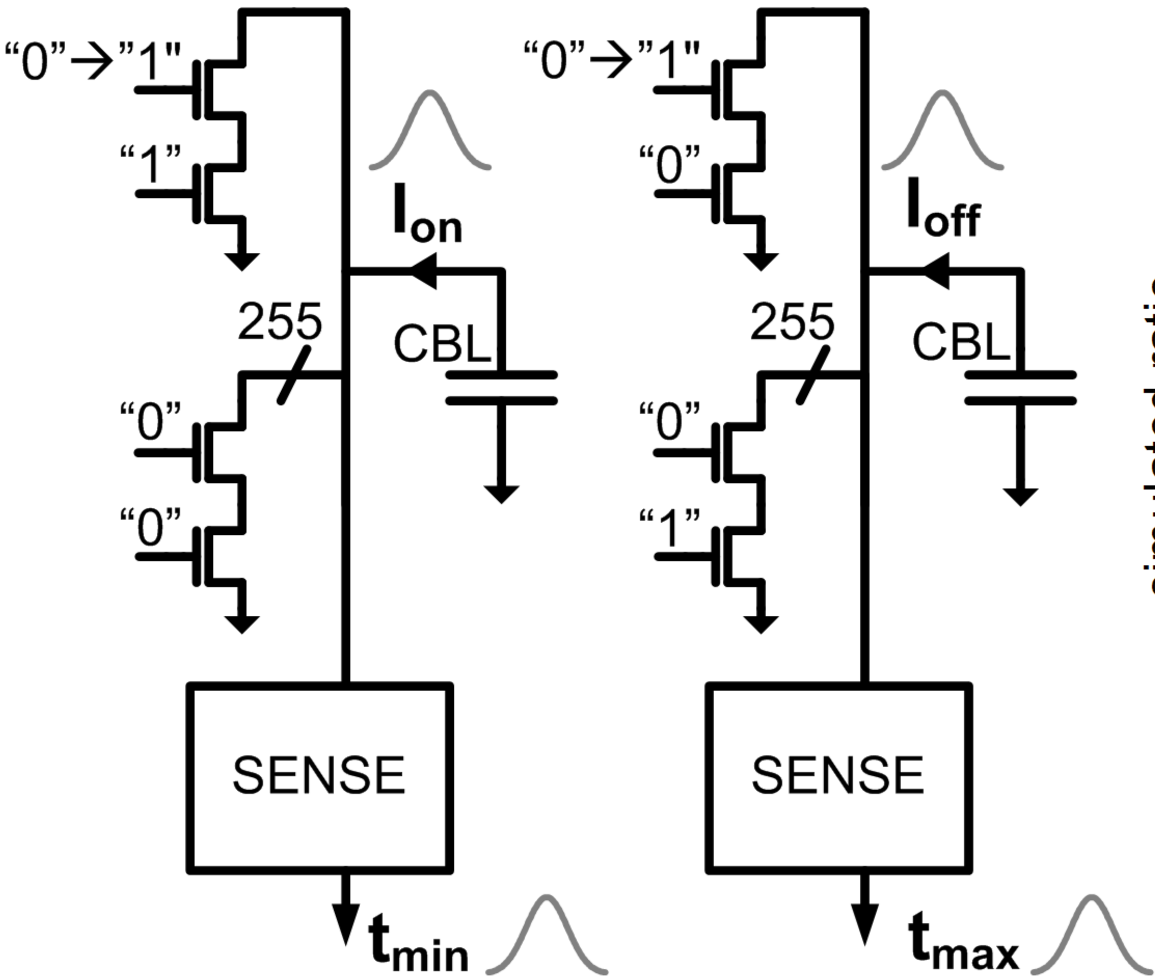
$$I_{\text{out}} = f\left(V_{SG4} - |V_{Tp}| + \Delta V_T\right)$$

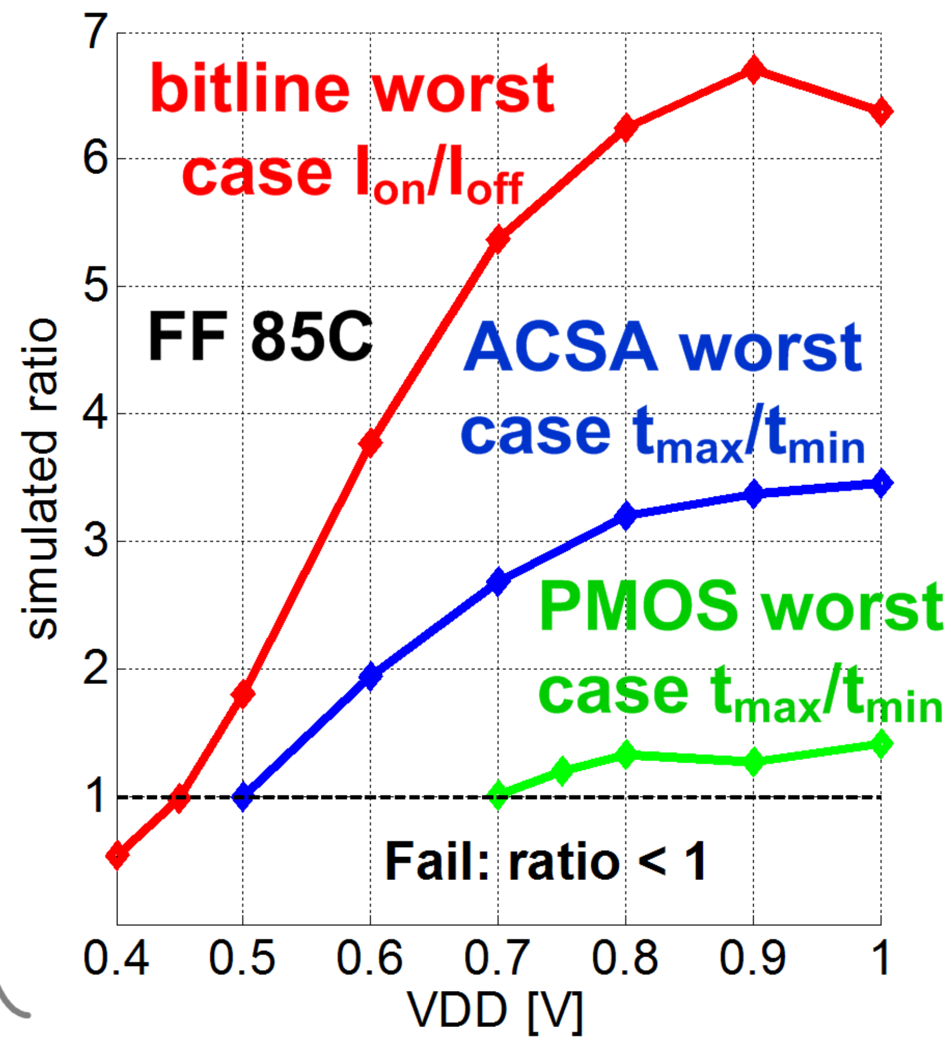
$$I_{\text{out}} = f\left(|\Delta V_{LBL}| - \frac{|V_{Tp}| + \Delta V_T}{1 + g_{m3}r_o}\right)$$



Amplification by M3 suppresses variation

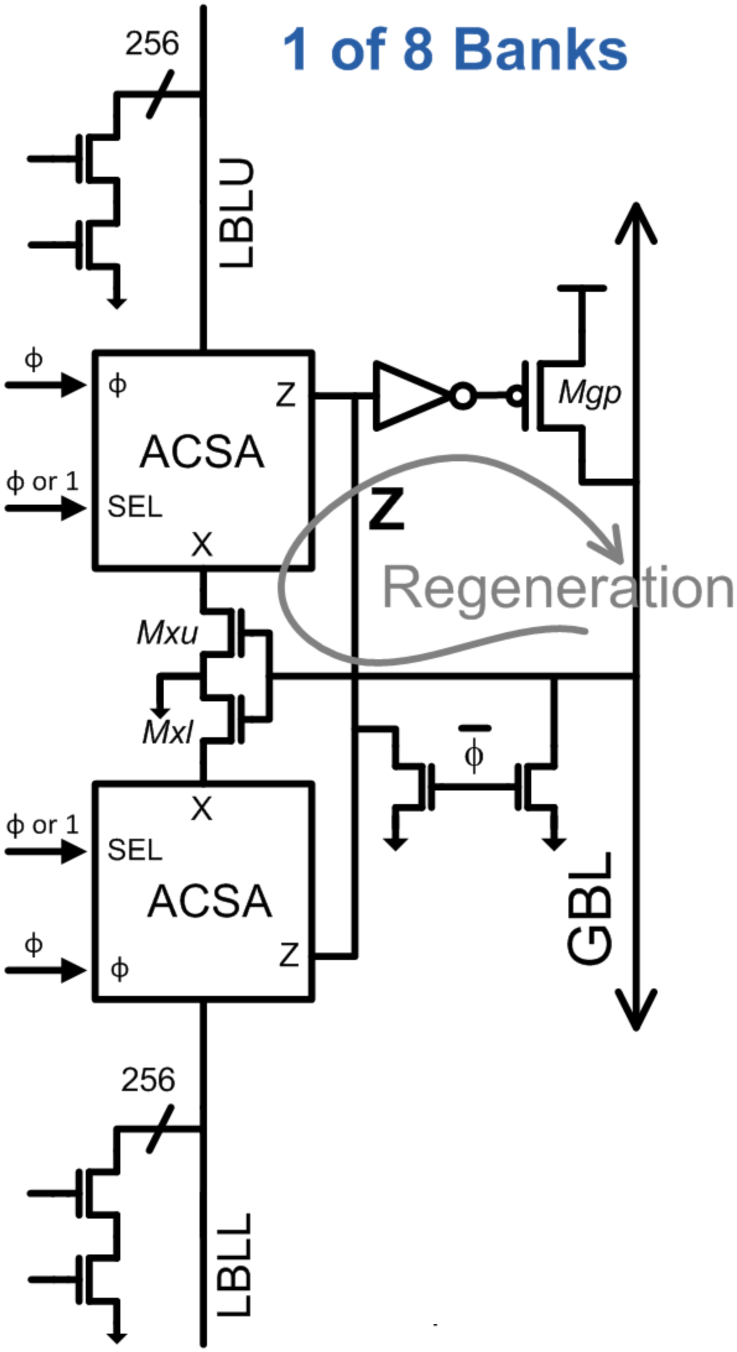
Offset Compensation Lowers V_{MIN}



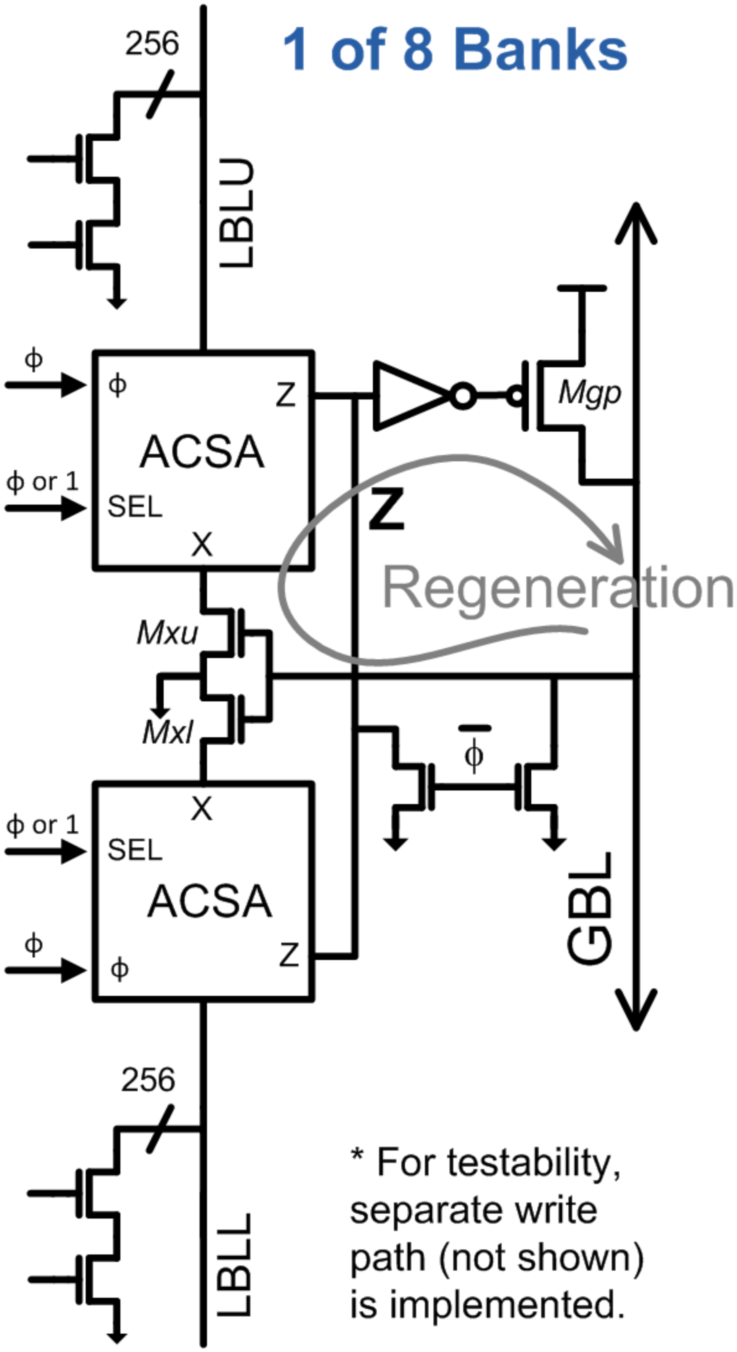


Variation in sensing network is critical to V_{MIN}

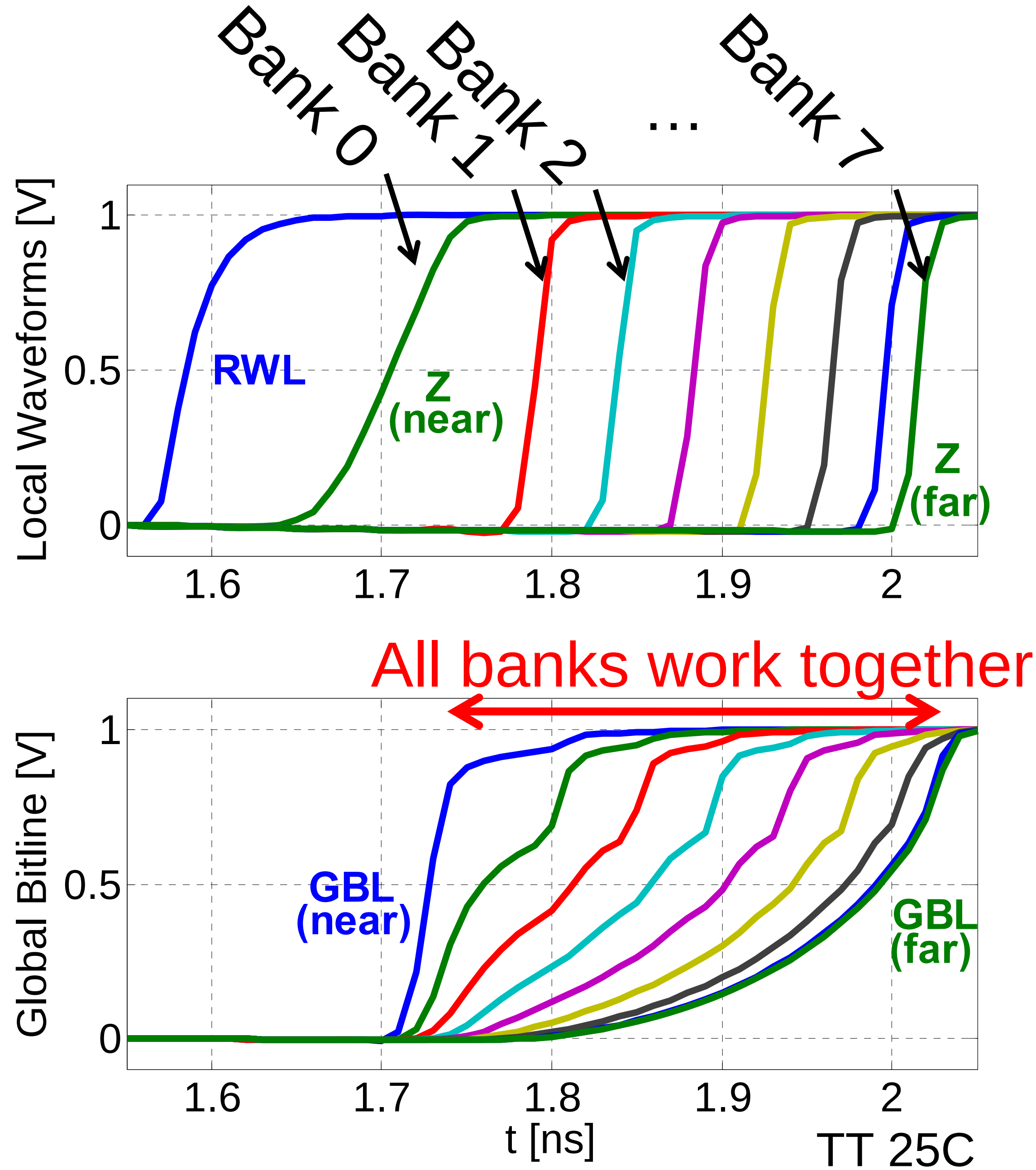
Regenerative Global Bitline Scheme



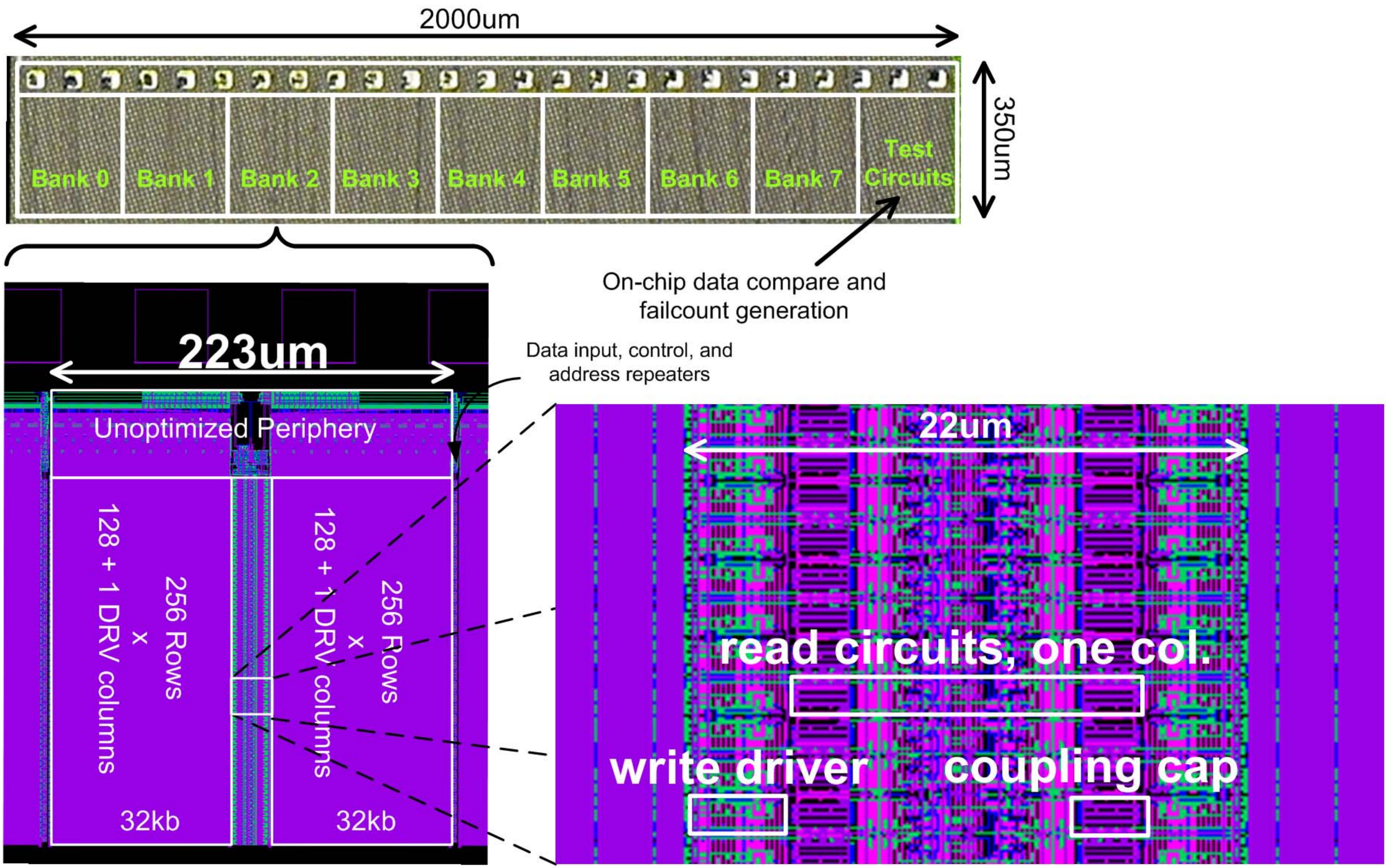
Regenerative Global Bitline Scheme



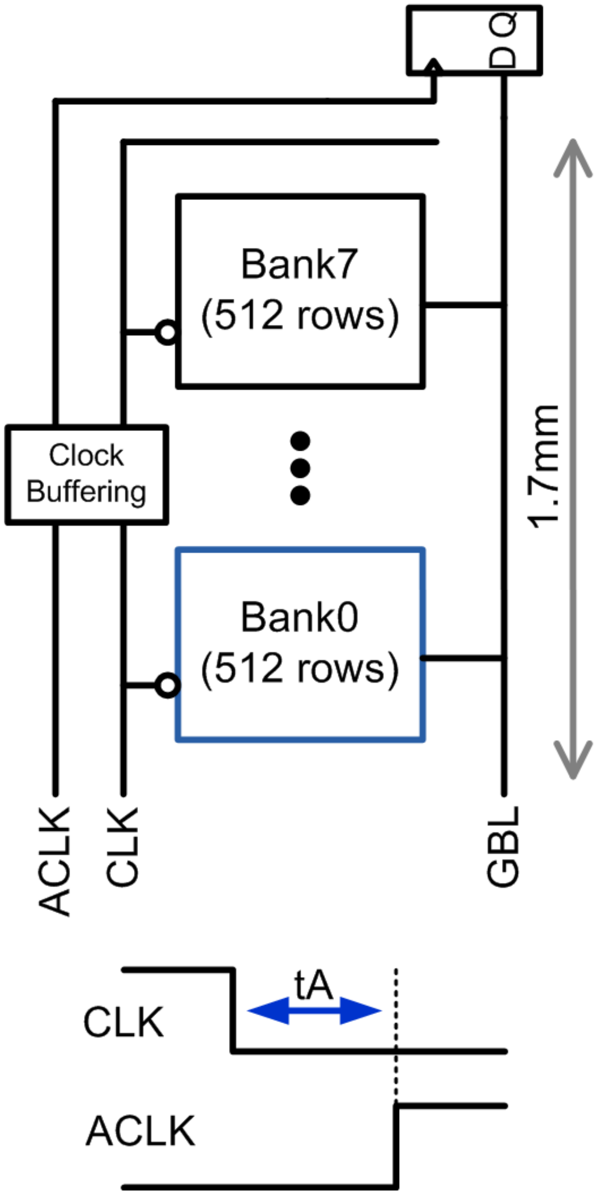
* For testability, separate write path (not shown) is implemented.



Die Photo and Area of Sensing Network



Measured Read Access Time



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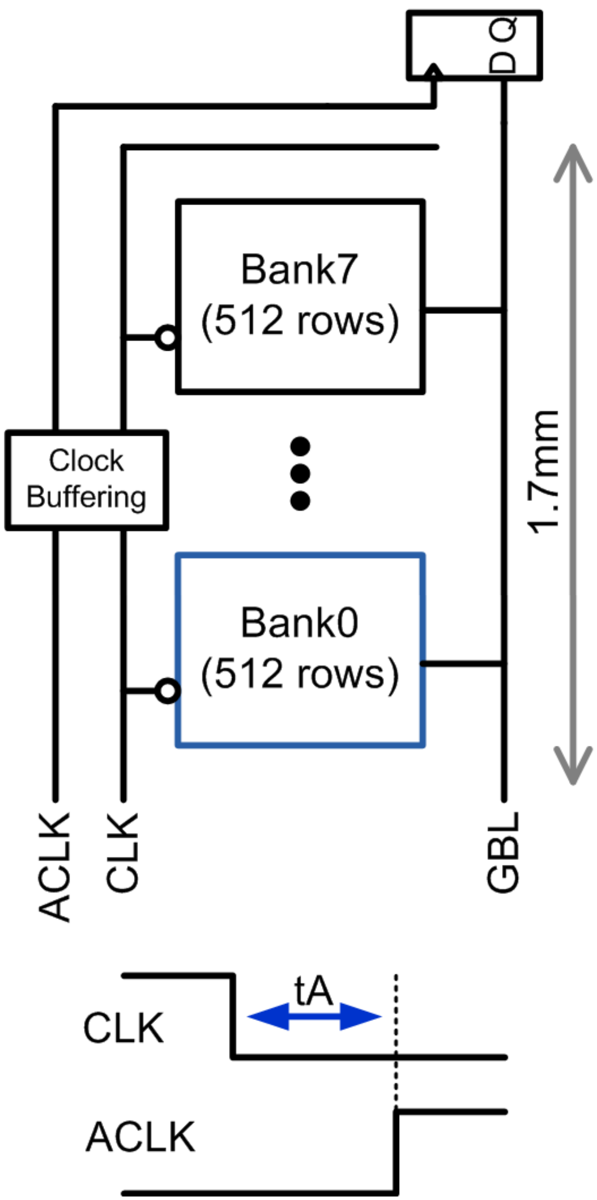
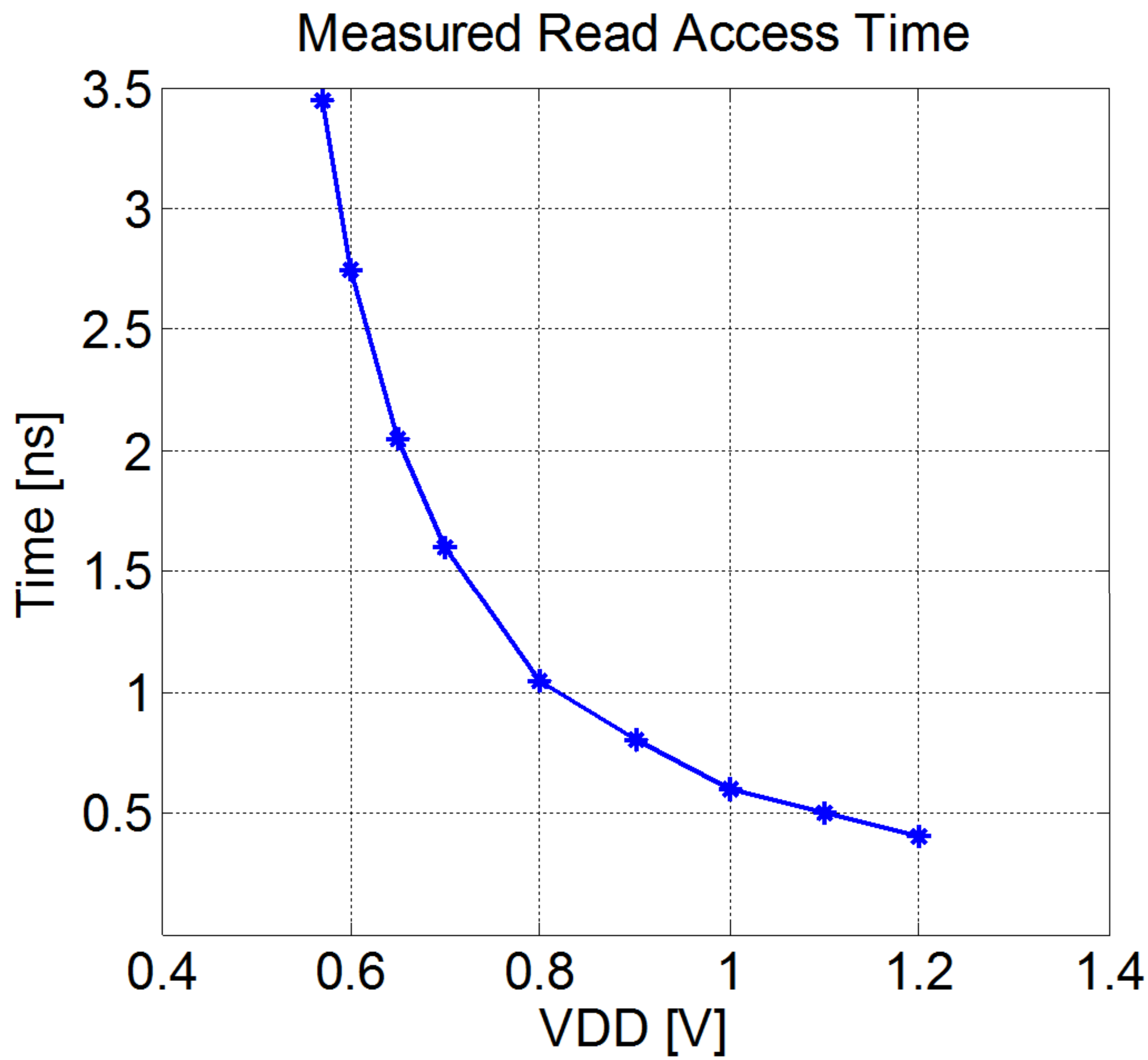
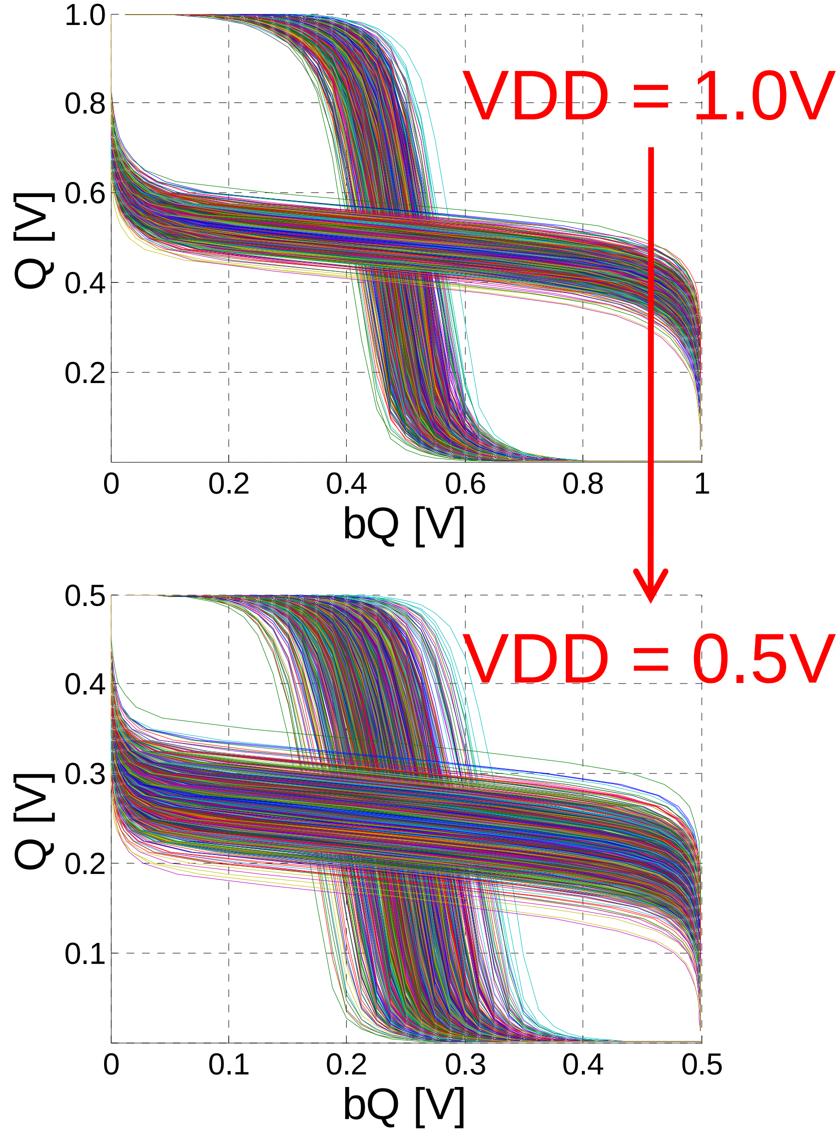
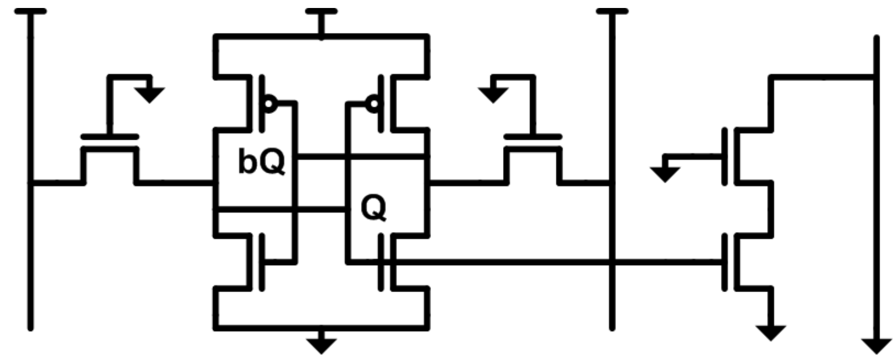


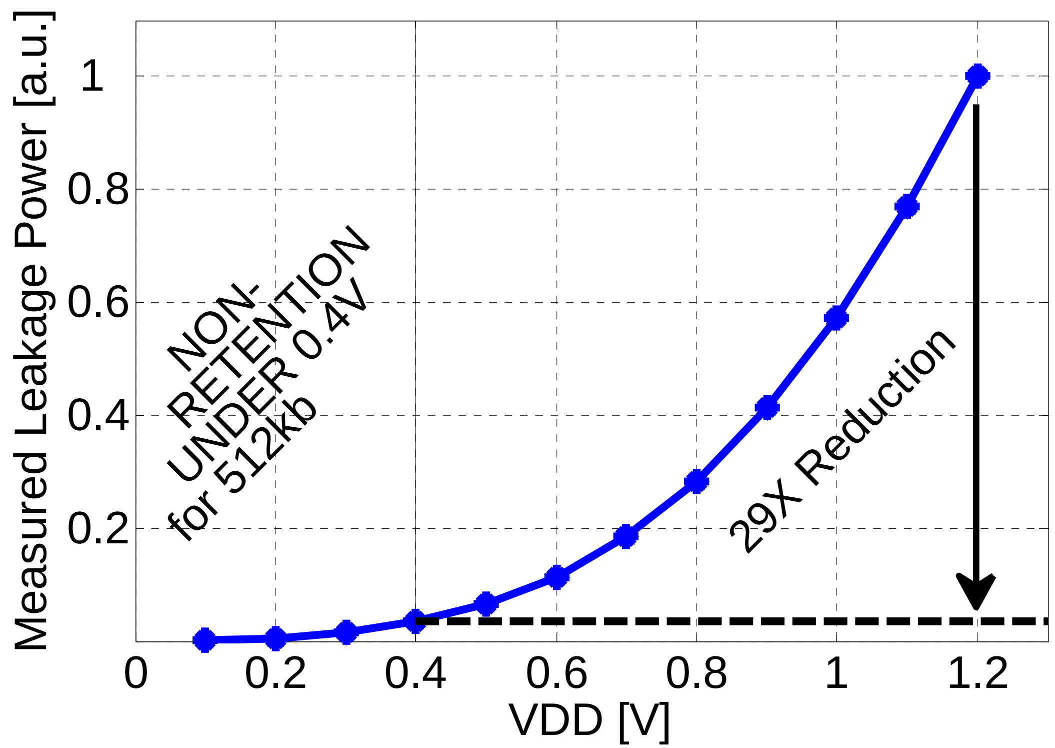


* The two measurements below 0.65V
require partial turn-on of a bleeder PMOS.

Data Retention and Standby Power

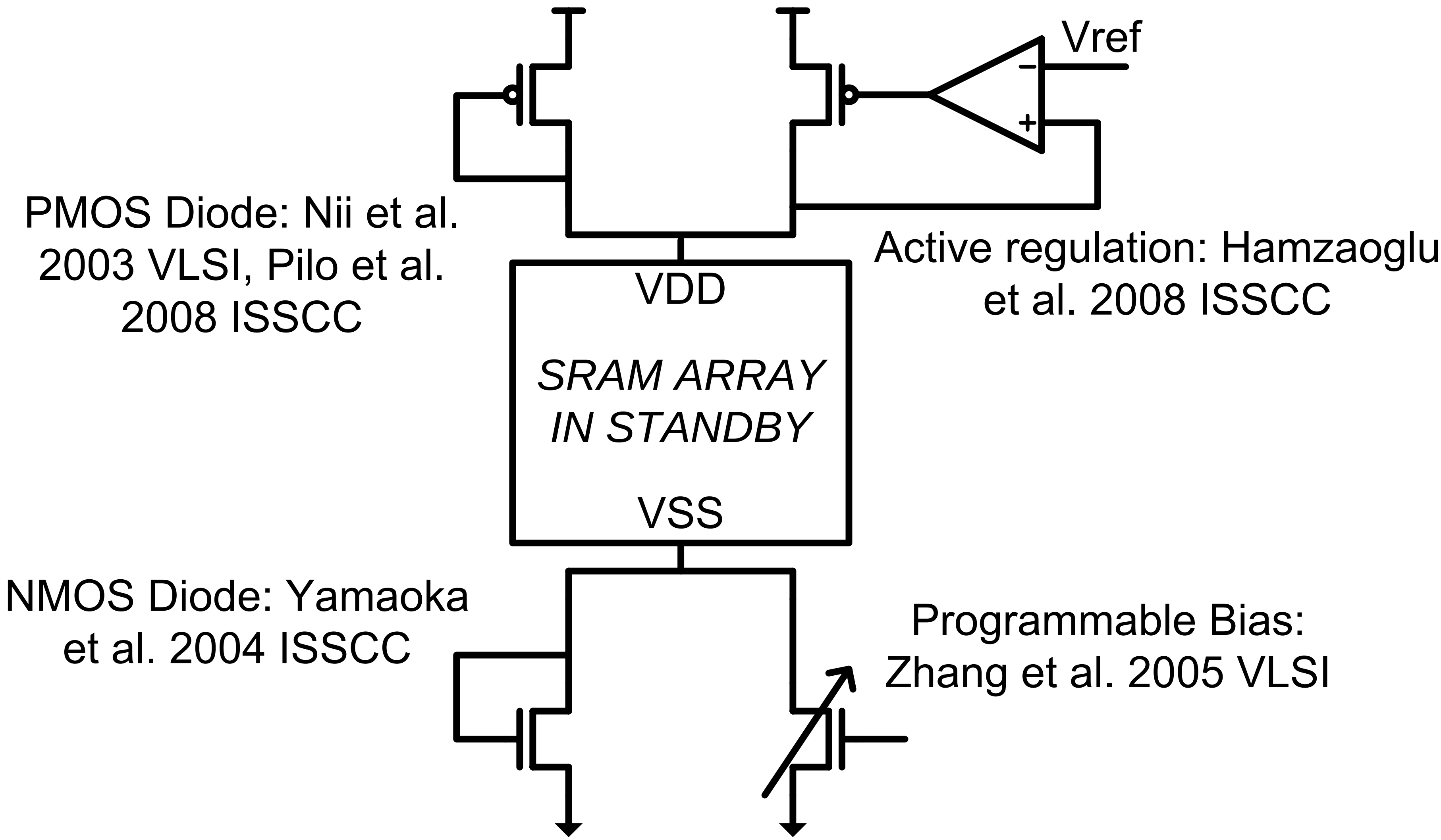






Knowing the limit of the data-retention-voltage (DRV) enables dramatic reduction of standby power.

Current Approaches to the DRV



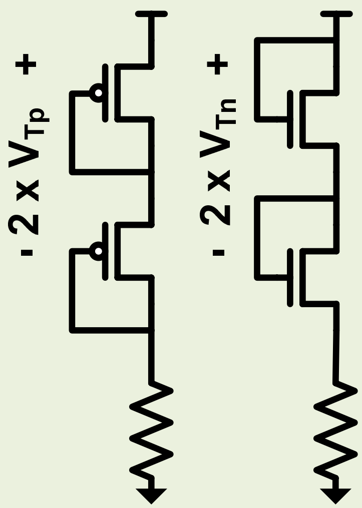
Conventional approaches cannot track global variation and require separate knowledge of the DRV.

Tracking the DRV

The DRV is a function of process corner and temperature.

Replica Cell Biasing

[Takeyama et al. 2005 VLSI]

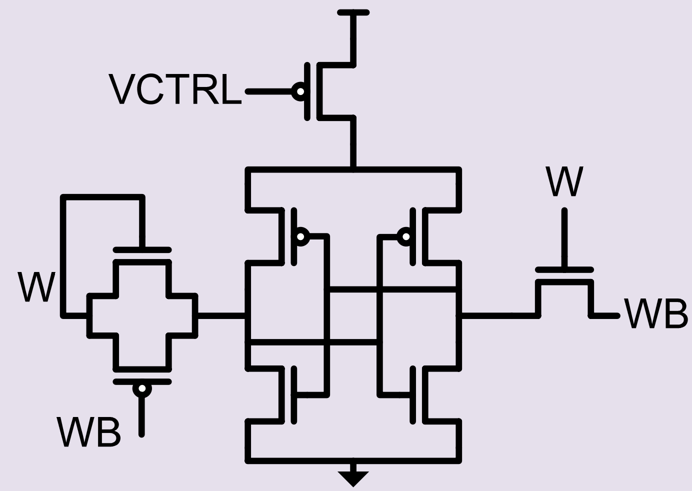


Bias Array voltage to:

$$VDD - VSS = 2 \times V_T$$

Canary Replica

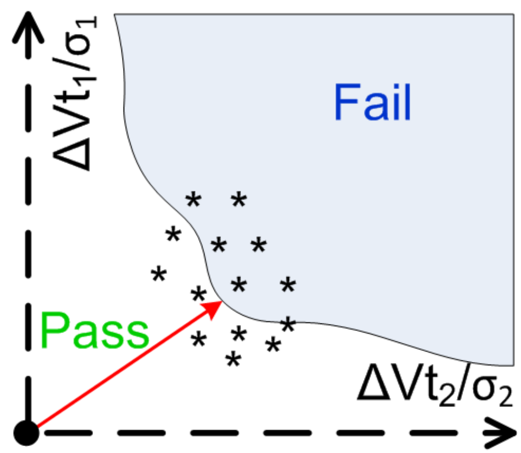
[Wang et al. 2007 CICC]



Calibrate against known DRV distribution.

Key challenge: Predict the DRV on-chip while preserving the state of the memory and the array efficiency of the design.

5σ Measurement with 2σ Sampling

	General method, Easy to implement	Efficient utilization of resources
Simulation Realm	Monte Carlo: $N_{MC}=100/p$ $p \sim 10^{-5}$ to 10^{-7} $N \sim 10^{7}$ to 10^{9} [N. Metropolis and S. Ulam 1949]	Importance Sampling & worst-case point:  [Antreich et al. 1991 ICCAD, Dolecek et al. 2008 ICCAD, Qazi et al. 2010 DATE]
Hardware Realm	Yield learning vehicle	?

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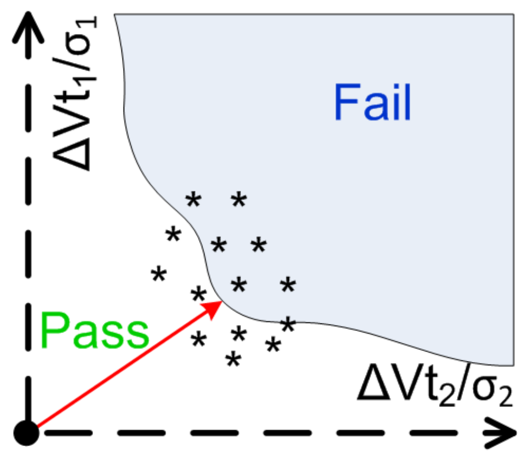
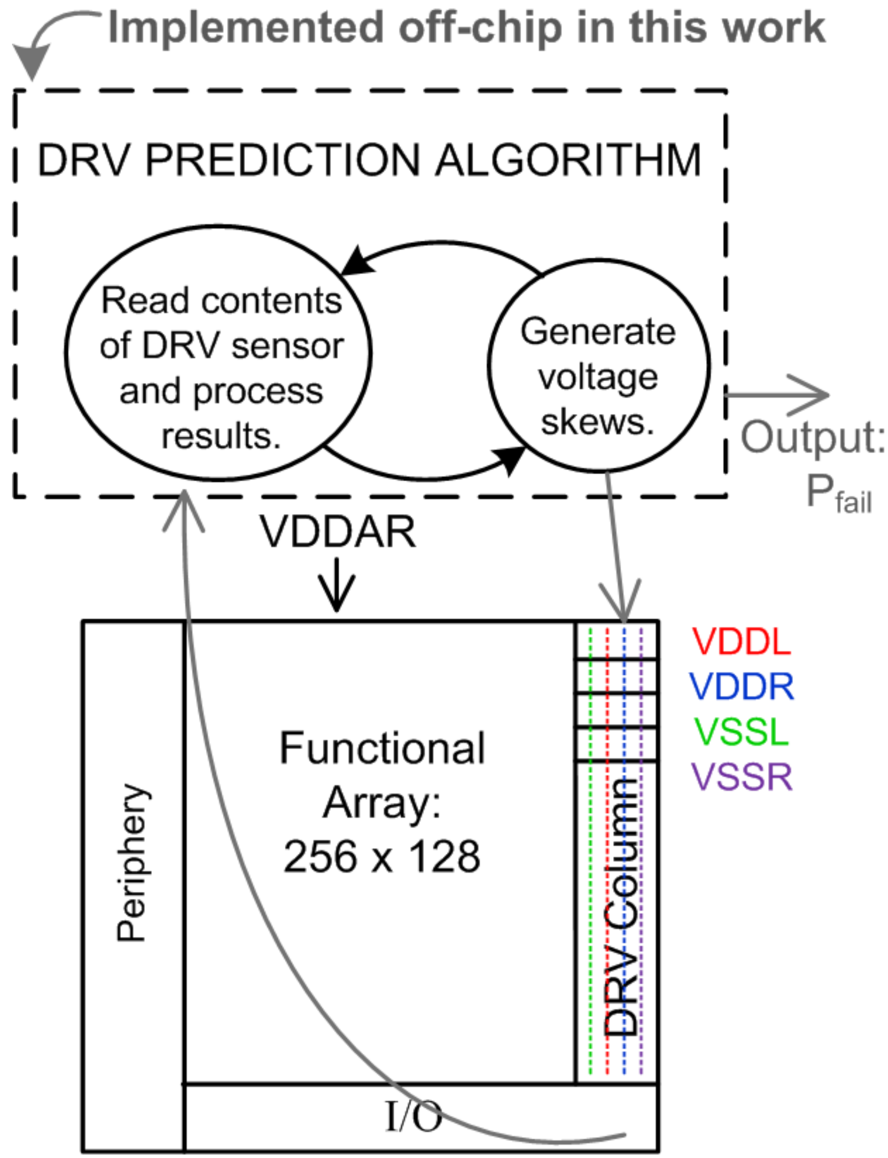
Simulation Realm	Monte Carlo: $N_{MC}=100/p$ $p \sim 10^{-5}$ to 10^{-7} $N \sim 10^{7}$ to 10^{9} [N. Metropolis and S. Ulam 1949]	Importance Sampling & worst-case point:  [Antreich et al. 1991 ICCAD, Dolecek et al. 2008 ICCAD, Qazi et al. 2010 DATE]
Hardware Realm	Yield learning vehicle	**THIS WORK**

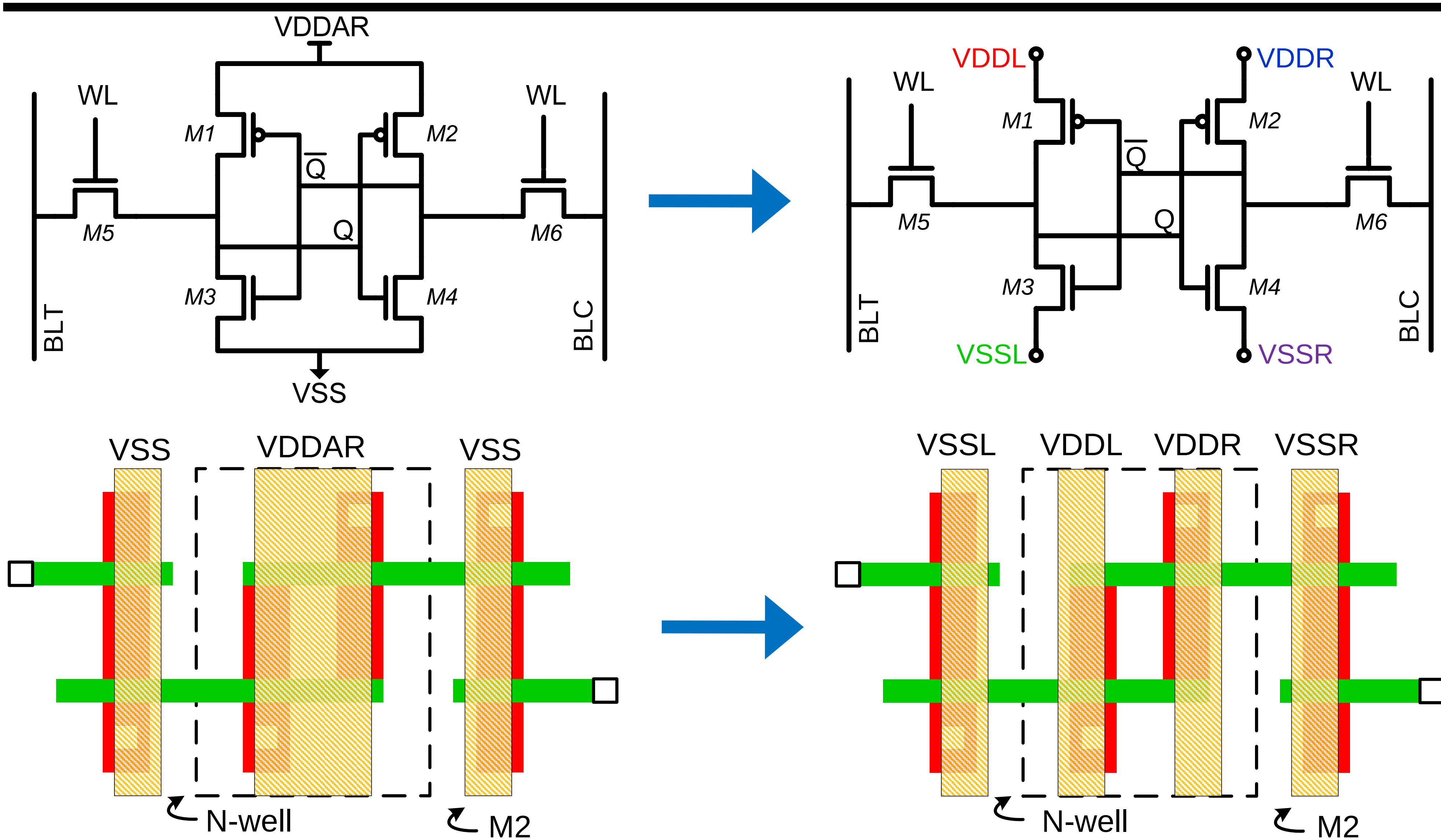
The DRV Sensor Overview

- Single column of 256 memory cells for each 32kb half-bank
- < 2% area overhead
- Split supply wiring
- Independent programming path
- **Recover functional relation between V_T and SNM**



$$SNM(\boldsymbol{\Delta V_T}) = 1 + c_1\Delta V_{T1} + c_2\Delta V_{T2} + c_3\Delta V_{T3} + c_4\Delta V_{T4} + c_5\Delta V_{T5} + c_6\Delta V_{T6}$$

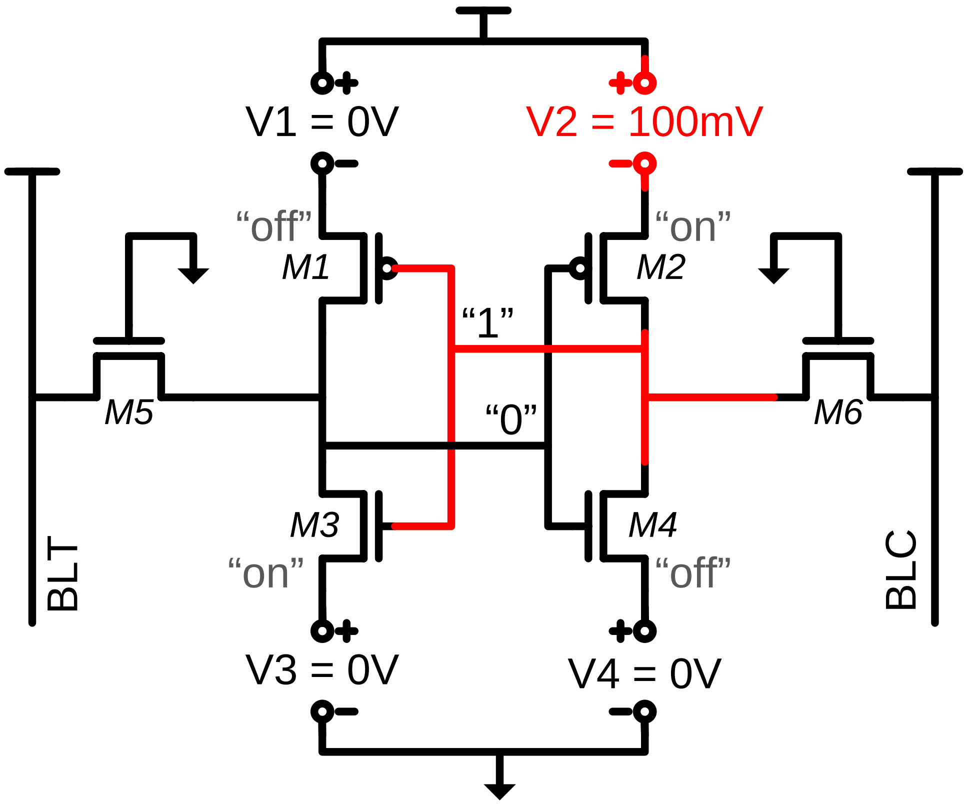
DRV Sensor Cell with Split Supplies



Identical layout of sensor cell transistors will track RDF mismatch

*2T read stack not shown for clarity.

Skew on Supply Emulates V_T Shift



General matrix representation:

$$\begin{bmatrix} \Delta V_{T1eff} \\ \Delta V_{T2eff} \\ \Delta V_{T3eff} \\ \Delta V_{T4eff} \\ \Delta V_{T5eff} \\ \Delta V_{T6eff} \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 & 0 \\ 0 & 1 & 1 & 0 \\ 0 & 1 & 1 & 0 \\ 0 & 0 & -1 & 1 \\ 0 & 0 & 1 & 0 \\ 0 & -1 & 0 & 0 \end{bmatrix} \begin{bmatrix} V1 \\ V2 \\ V3 \\ V4 \end{bmatrix}$$

$$\mathbf{\Delta V_{Teff}} = \mathbf{T_{0\rightarrow 1}} \quad \mathbf{V}$$

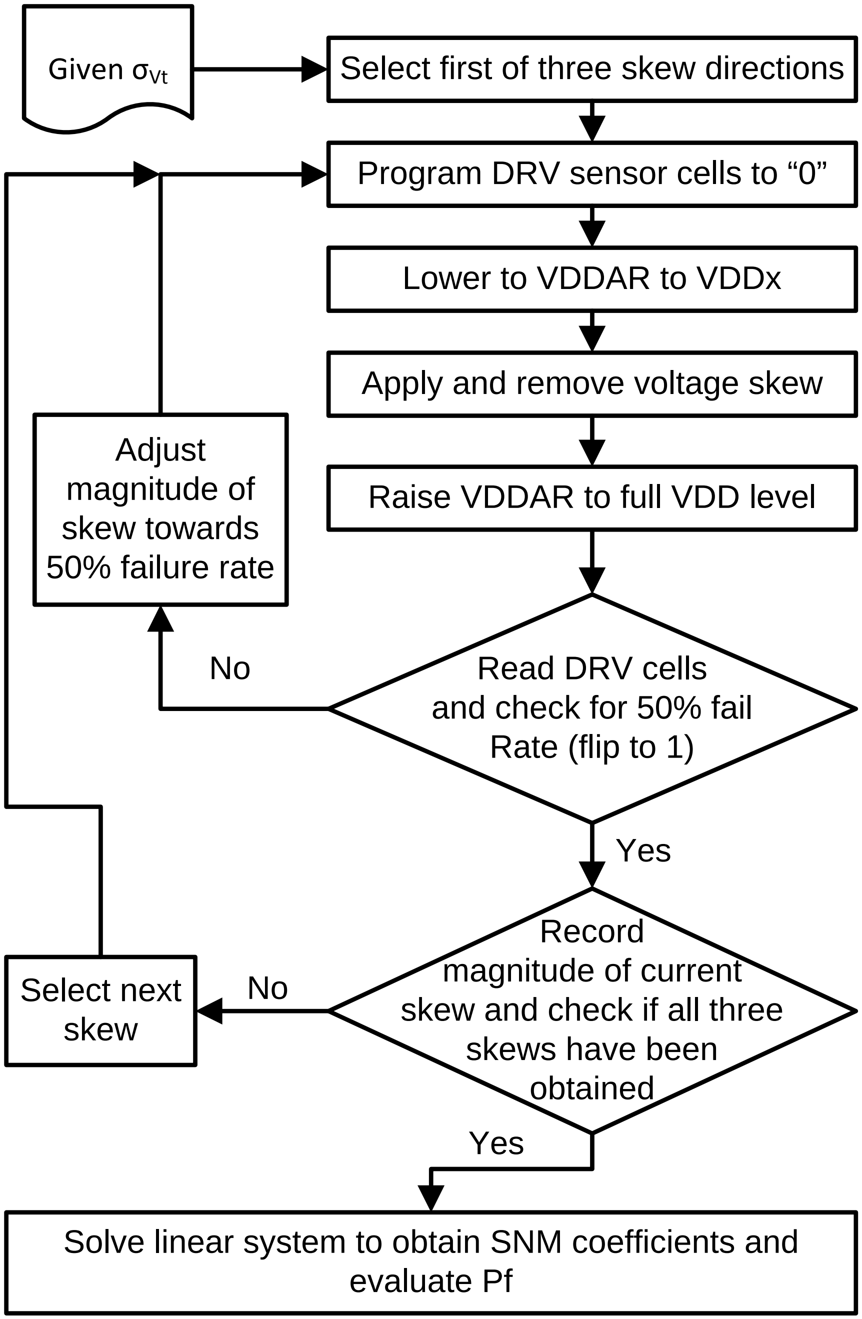
* positive V_T convention for PMOS devices.

Example supply skew (Q = "0"):

$$\Rightarrow \mathbf{\Delta V_{Teff}^{T}} = [-100mV \quad 100mV \quad 100mV \quad 0 \quad 0 \quad -100mV]$$

Effective threshold shift achieved by degenerating VGS

The DRV Sensor Algorithm



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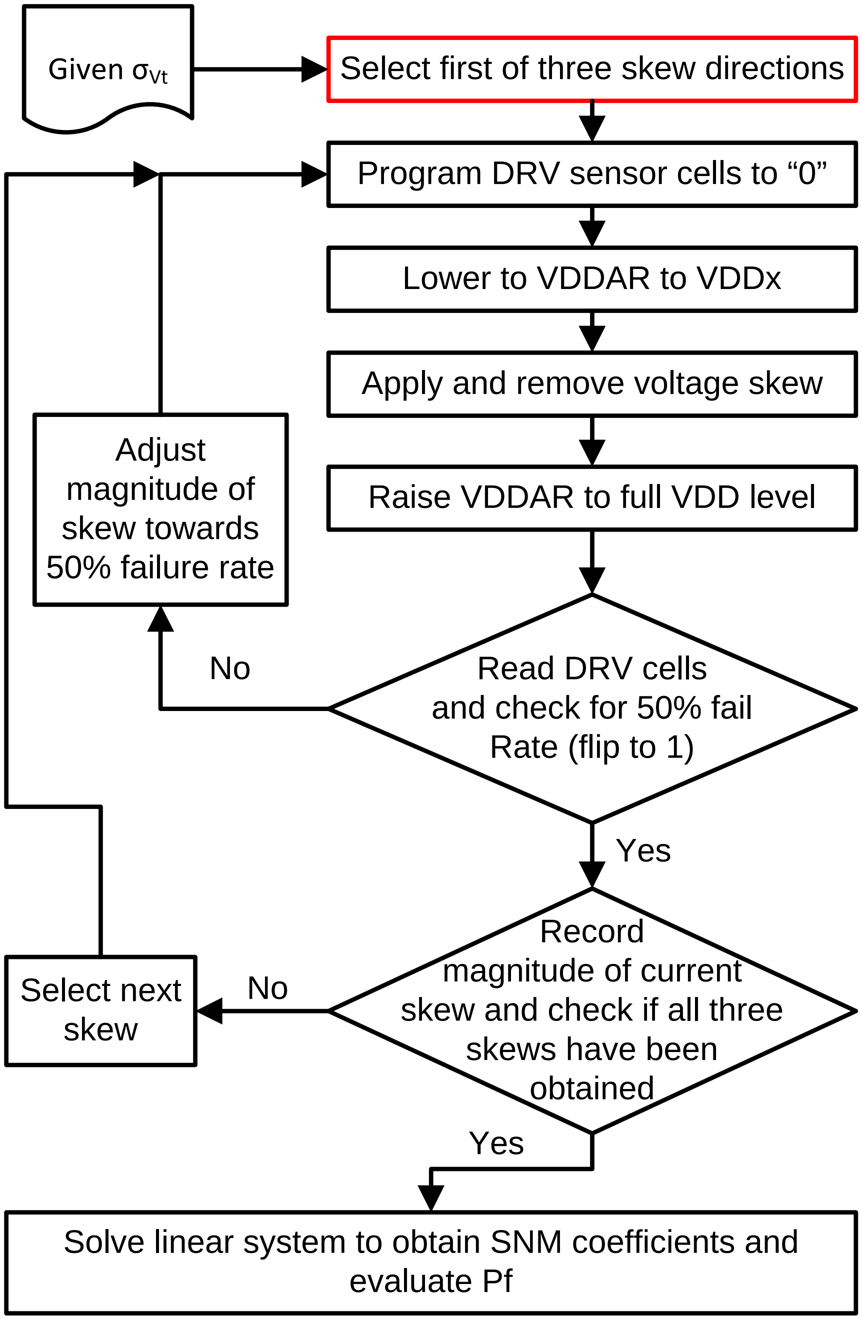


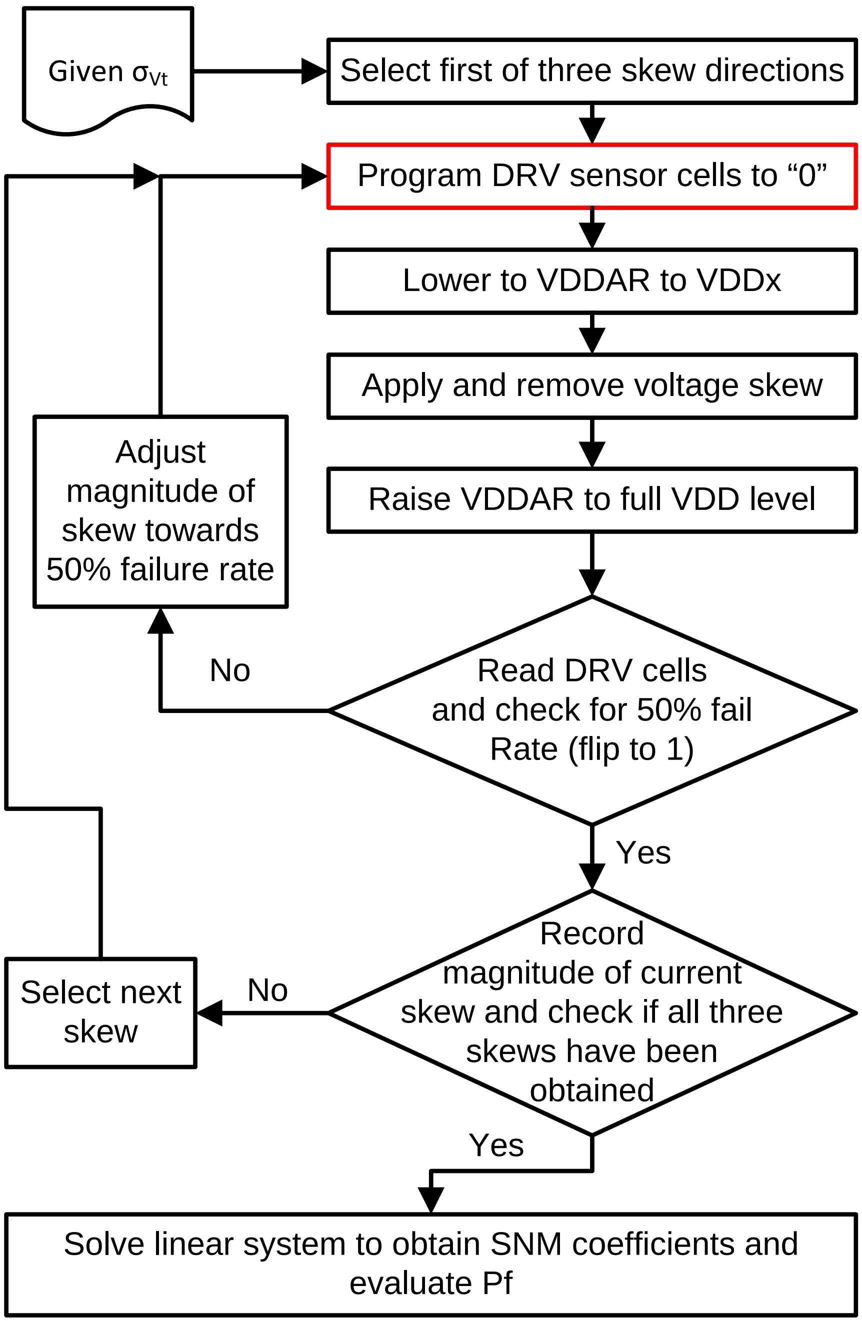
$$\mathbf{v}^{1T} = \frac{k}{\sqrt{2}} \begin{bmatrix} 0 & 1 & 0 & -1 \end{bmatrix}$$

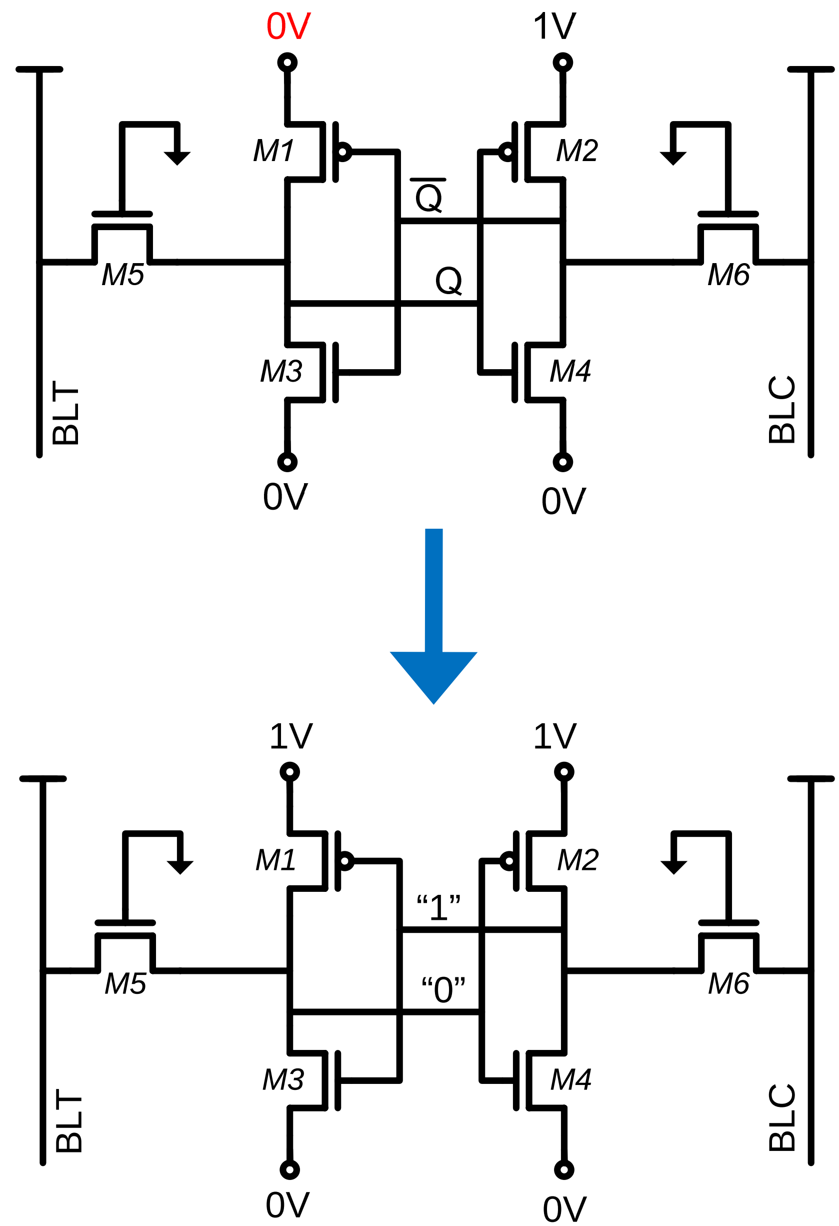
$$\mathbf{v}^{2T} = k \begin{bmatrix} 0 & 1 & 0 & 0 \end{bmatrix}$$

$$\mathbf{v}^{3T} = k \begin{bmatrix} 0 & 0 & 1 & 0 \end{bmatrix}$$

*SNM equation appropriately simplified to 3 degrees of freedom.

The DRV Sensor Algorithm





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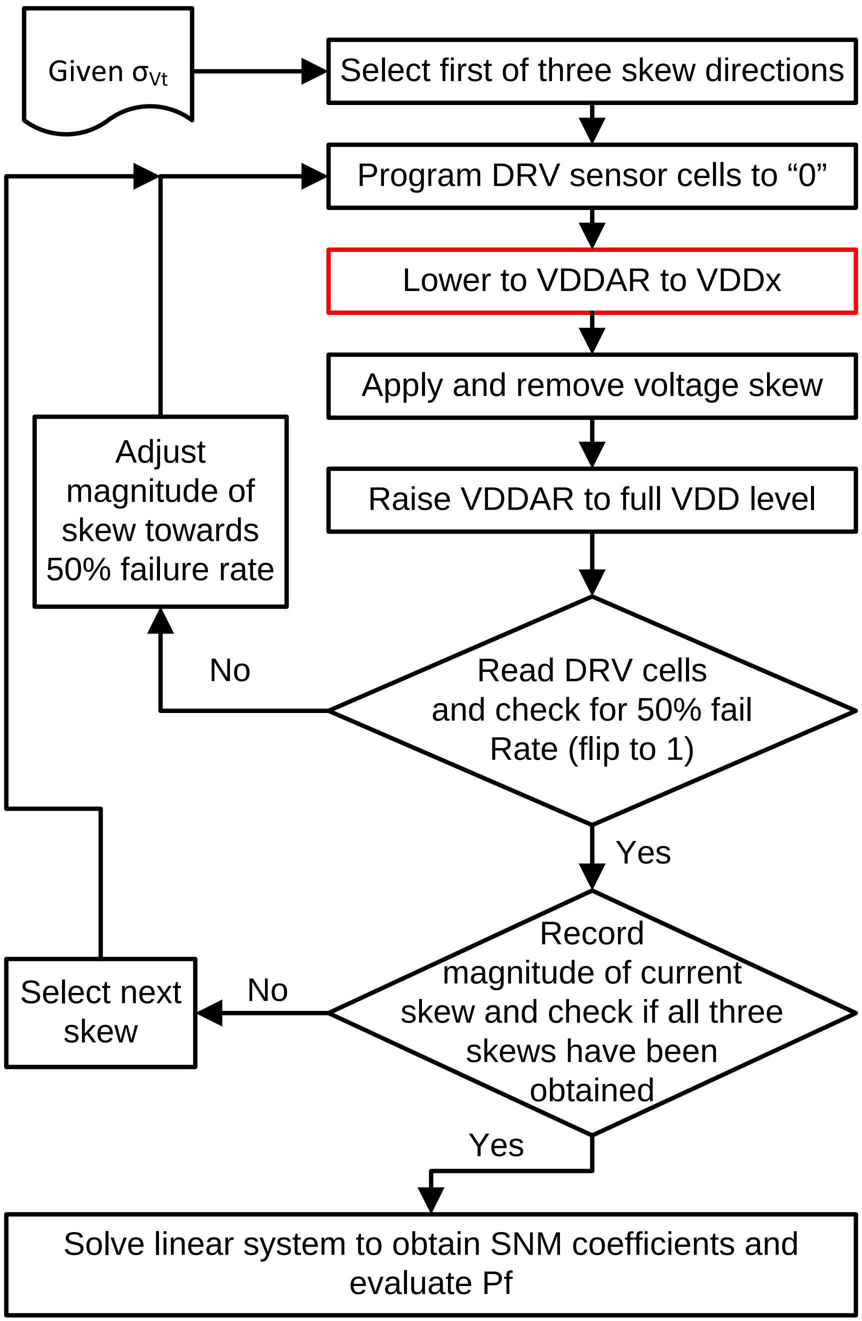
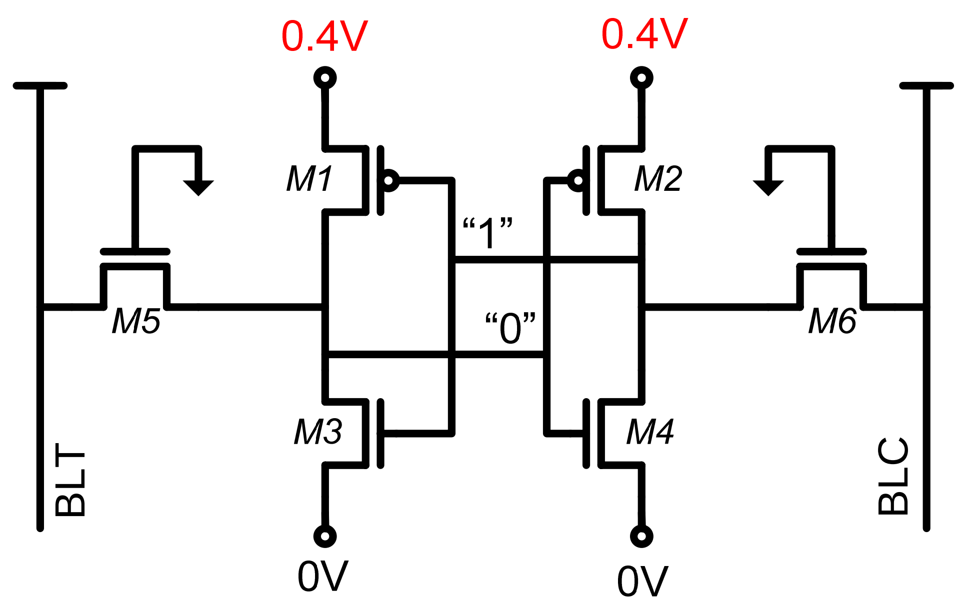


Example VDDx = 0.4V



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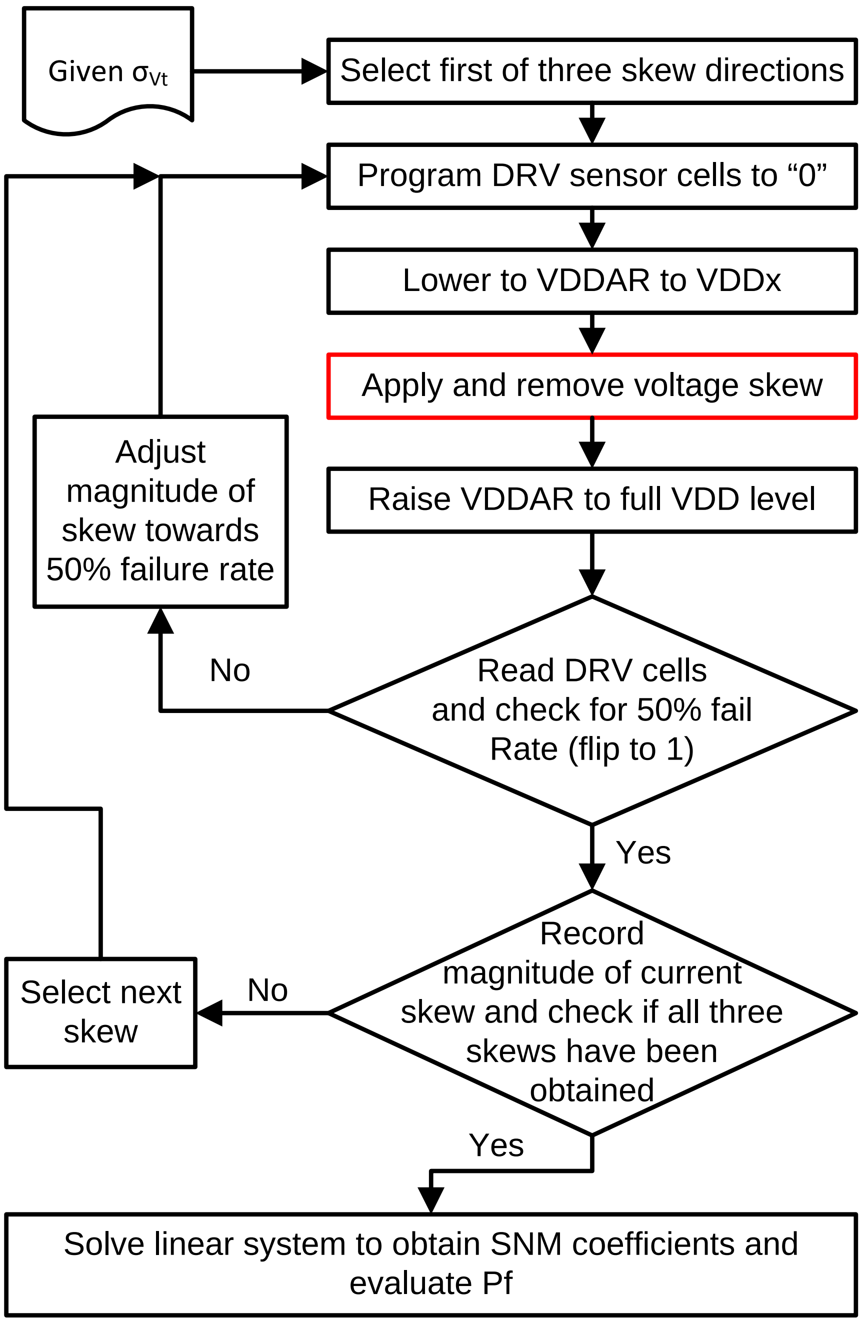

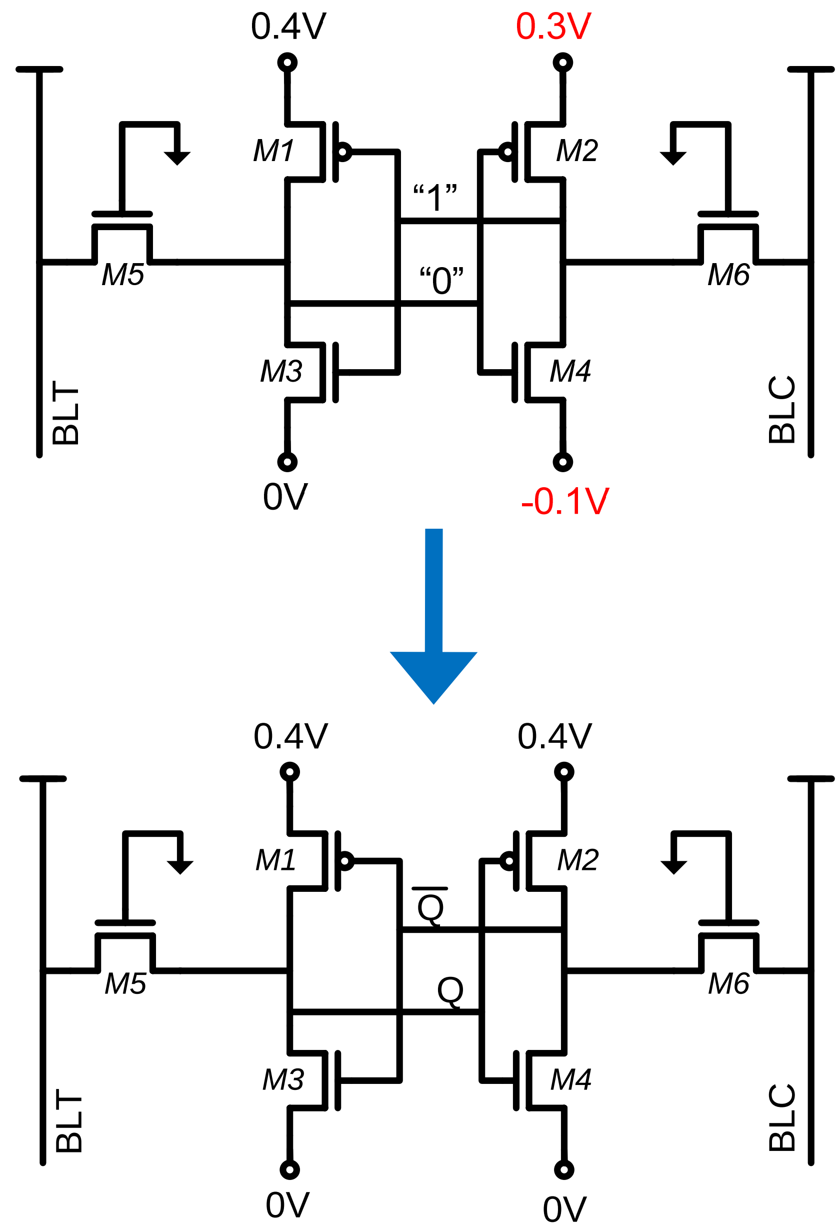

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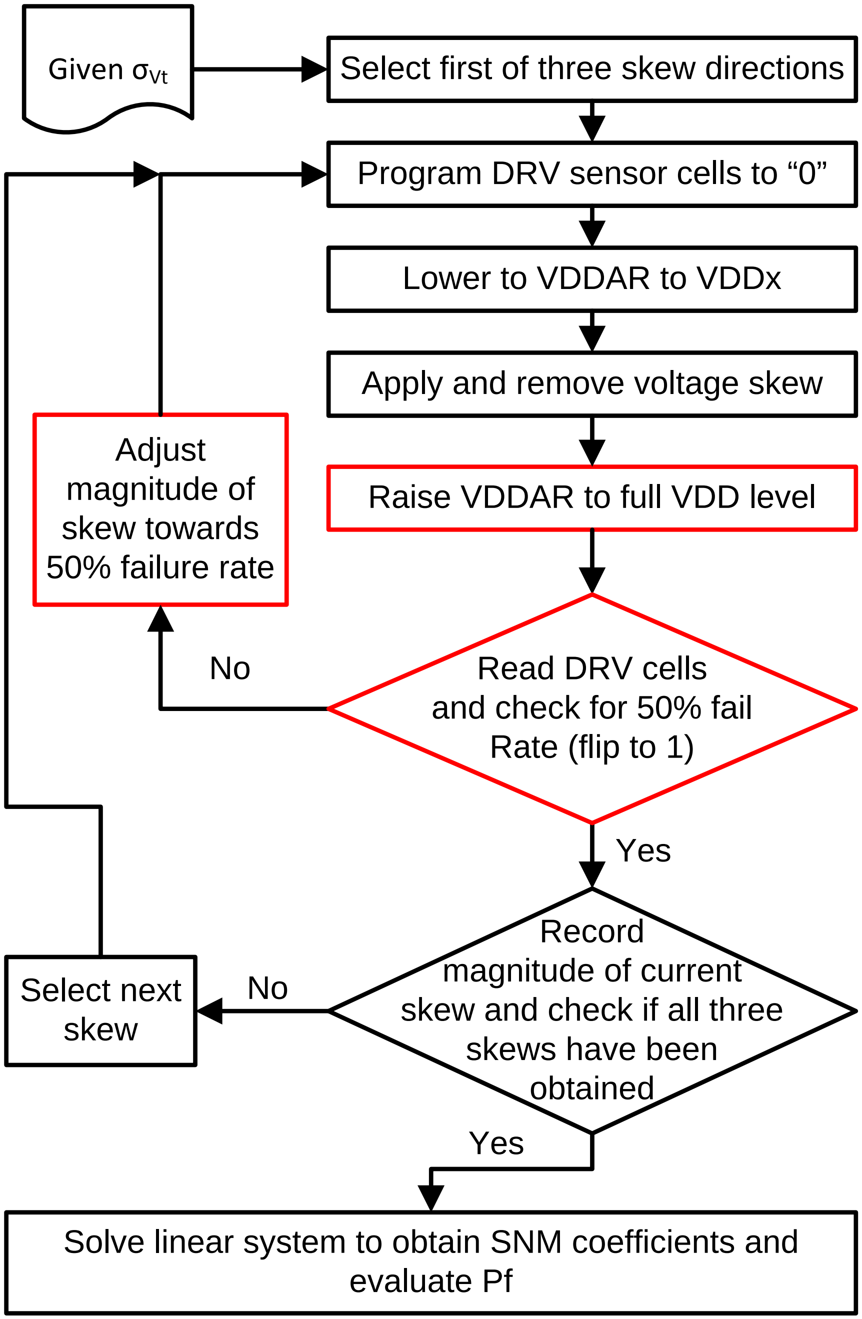

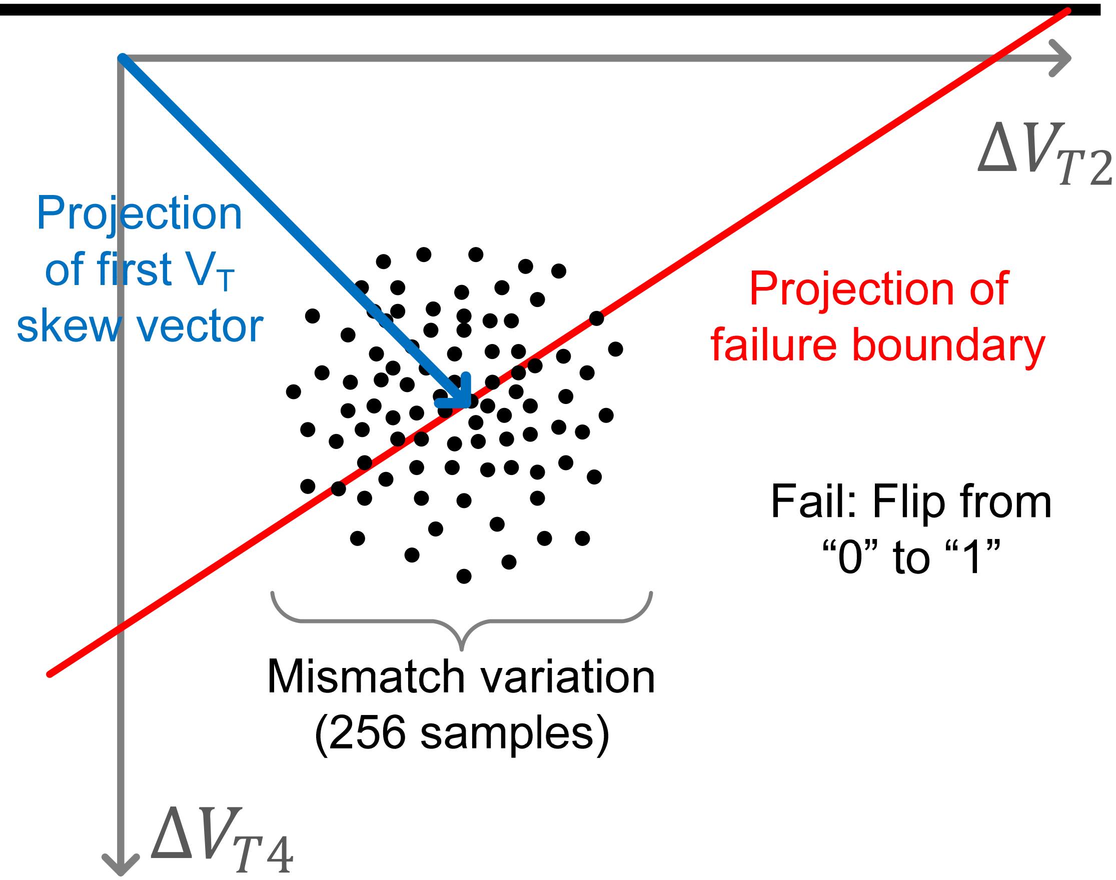

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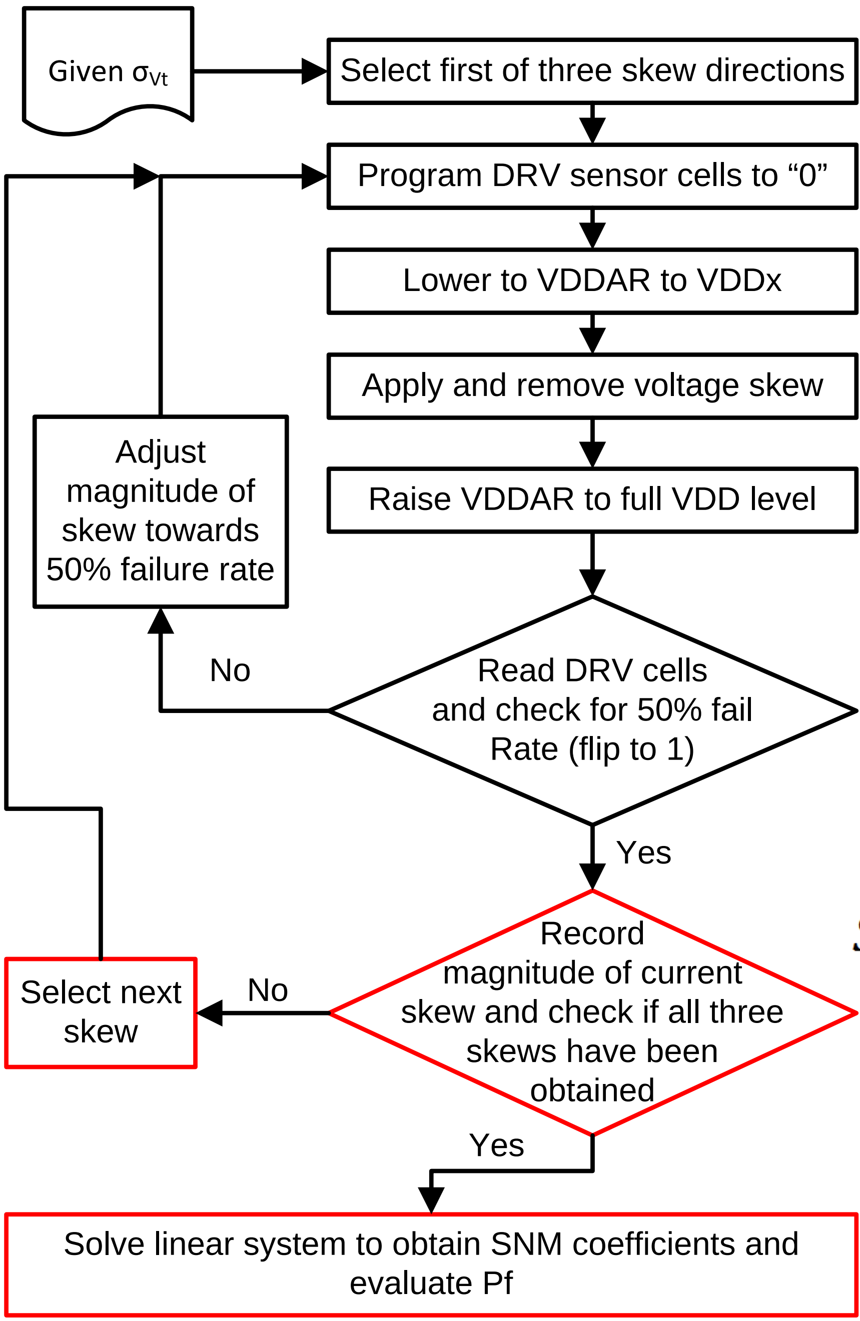
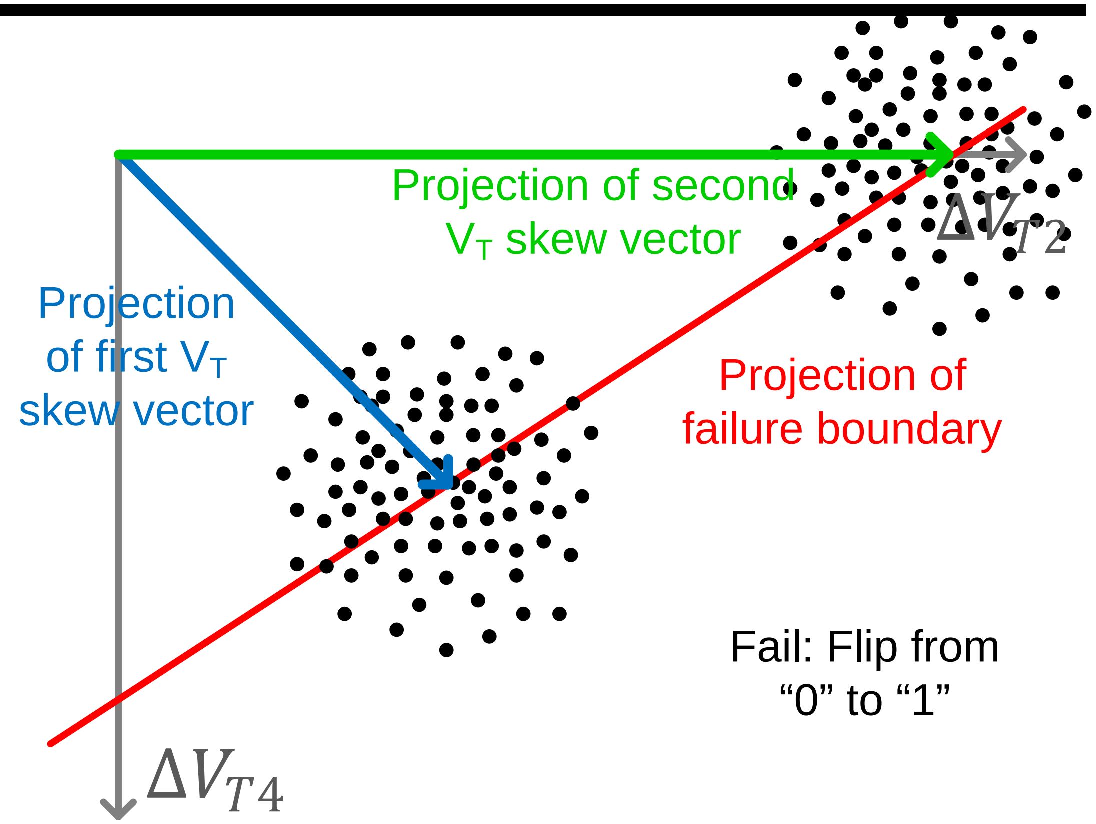
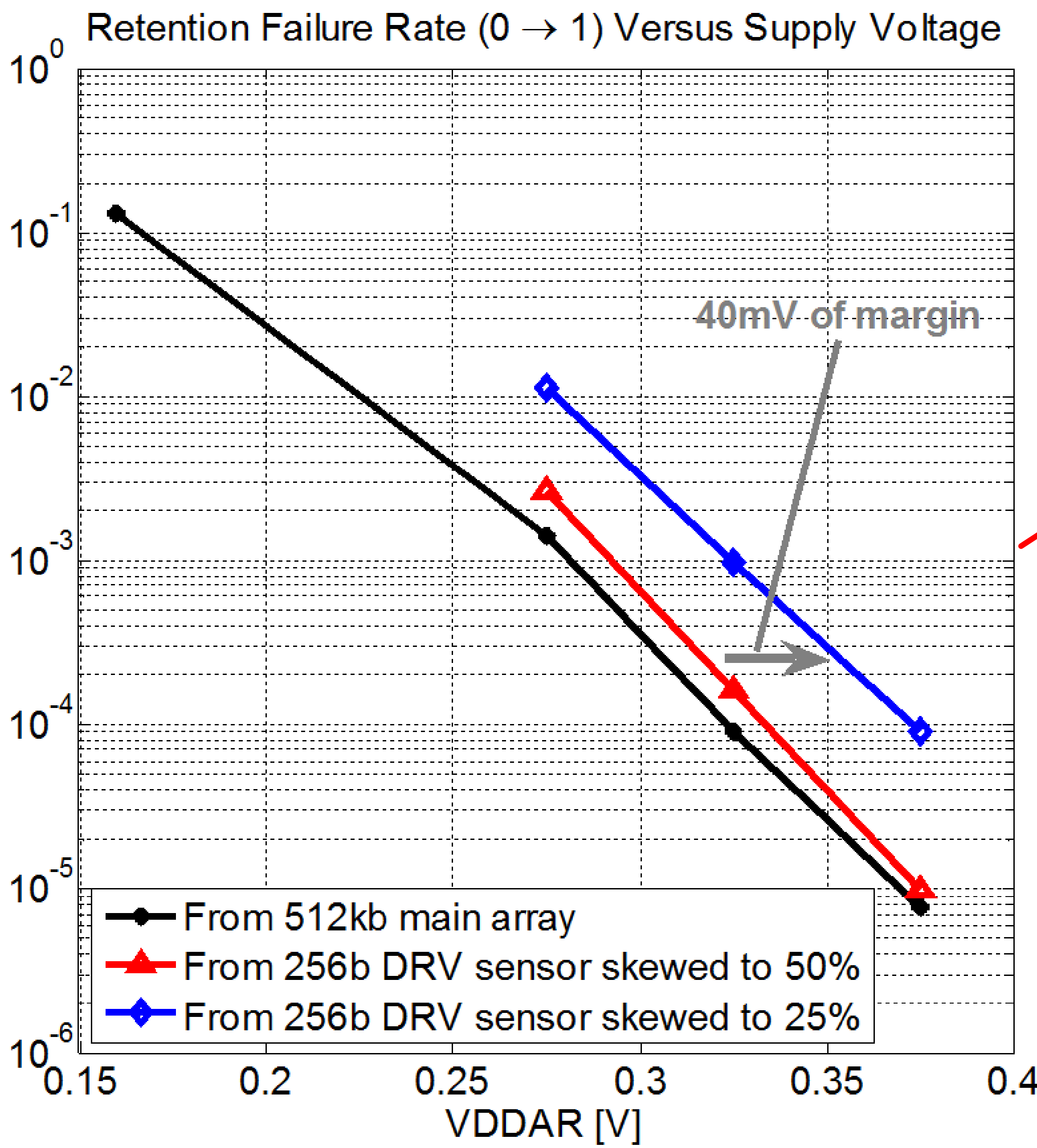


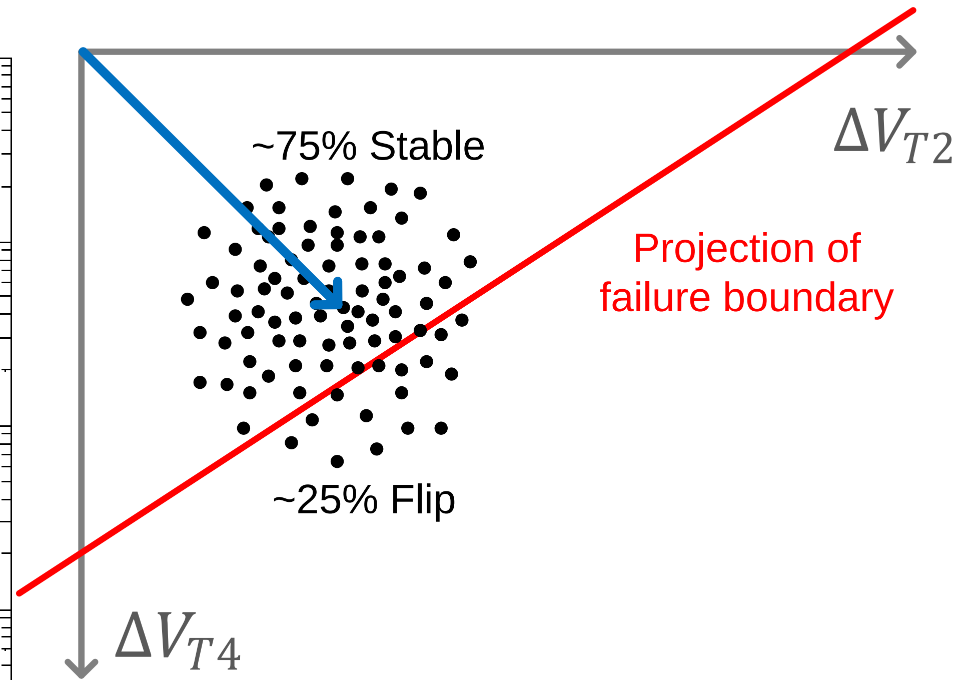


$$SNM = 1 + [c_1 \quad c_2 \quad c_4]\, R\, T_{0\to 1}\, [\boldsymbol{V}^1 \quad \boldsymbol{V}^2 \quad \boldsymbol{V}^3] = 0$$

$$P_f = \phi\left(-\frac{1}{\sqrt{(c_1\sigma_2)^2 + (c_2\sigma_2)^2 + \cdots + (c_6\sigma_6)^2}}\right)$$

DRV Sensor Measurement Results

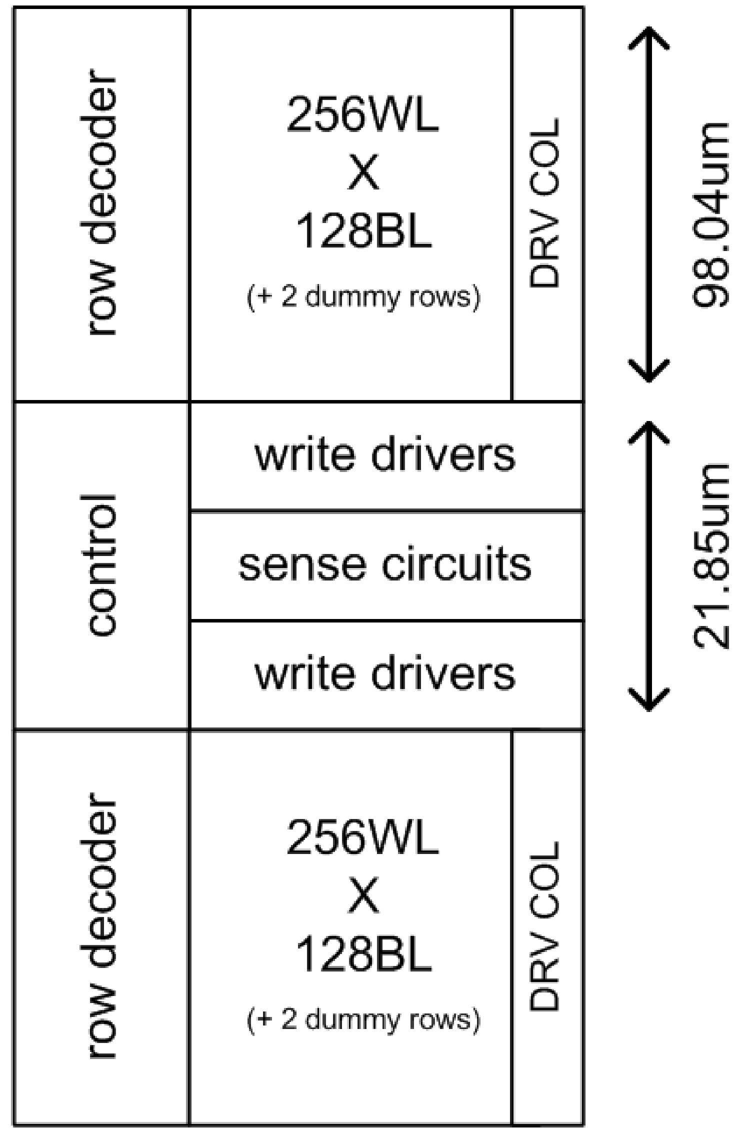




The spherically symmetric sampling of V_T mismatch enables the insertion of margin.

512kb Macro Summary

Organization	4096 words x 128b (in 8 banks of 64kb)
Technology	45nm High-Performance SOI
Cell area	$0.578um^2$
Sense Circuit Area Supporting 512b	$20.9um^2$
Access time at 1.2V	400ps
Access time at 0.57V	3.4ns
Active Power at 1.2V (extrapolated from 100MHz to 1.25GHz)	169mW
Leakage Power at 1.2V	338mW



64kb Bank

Conclusions

- AC-coupling is viable on a finer scale in advanced CMOS technology.
- Variation-tolerant sensing networks are needed to operate closer to the fundamental voltage scaling limits of the bitcell.
- Statistical fluctuation can be predicted on-chip by recovering the functional relation between variation parameter and performance metric.

Acknowledgement: FCRP Focus Center for Circuit & System Solutions (C2S2) for funding.