A 0.16mm^2 Completely On-Chip Switched-Capacitor DC-DC Converter using Digital Capacitance Modulation for LDO Replacement in 45nm CMOS

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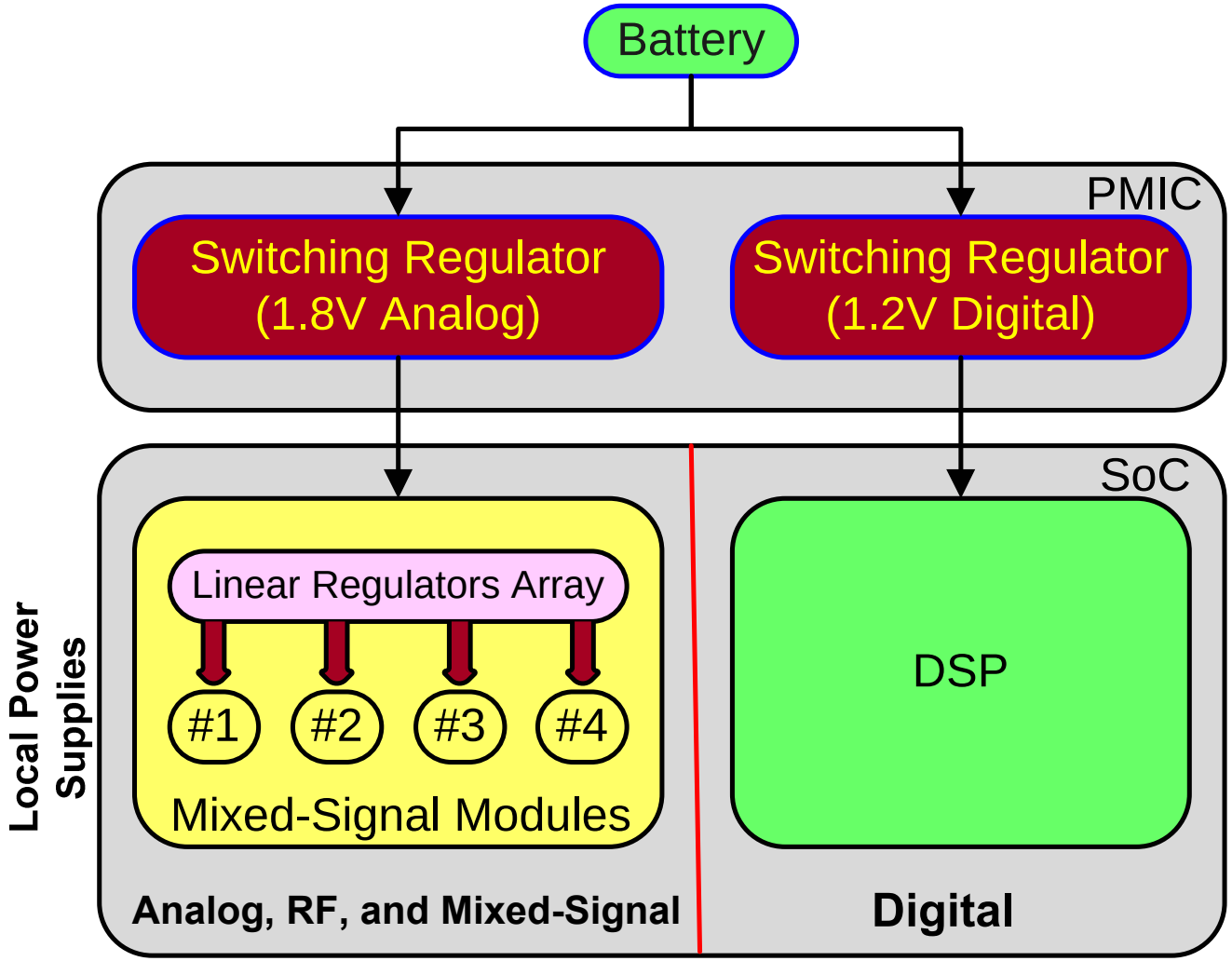
Power Domains in Wireless Systems

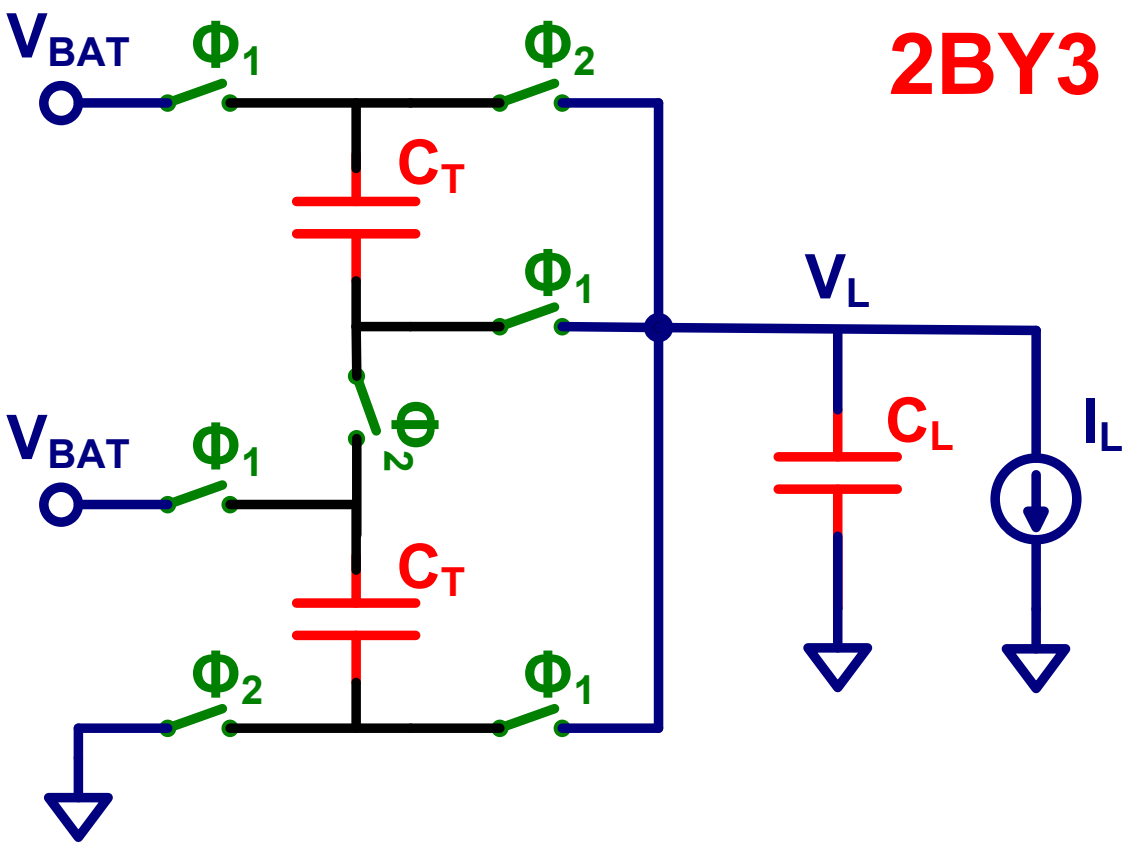


LDO Efficiency

$$\eta_{max} = \frac{V_L}{1.8}$$

Multiple low-efficiency local linear regulators

Switched Capacitor DC-DC Converter

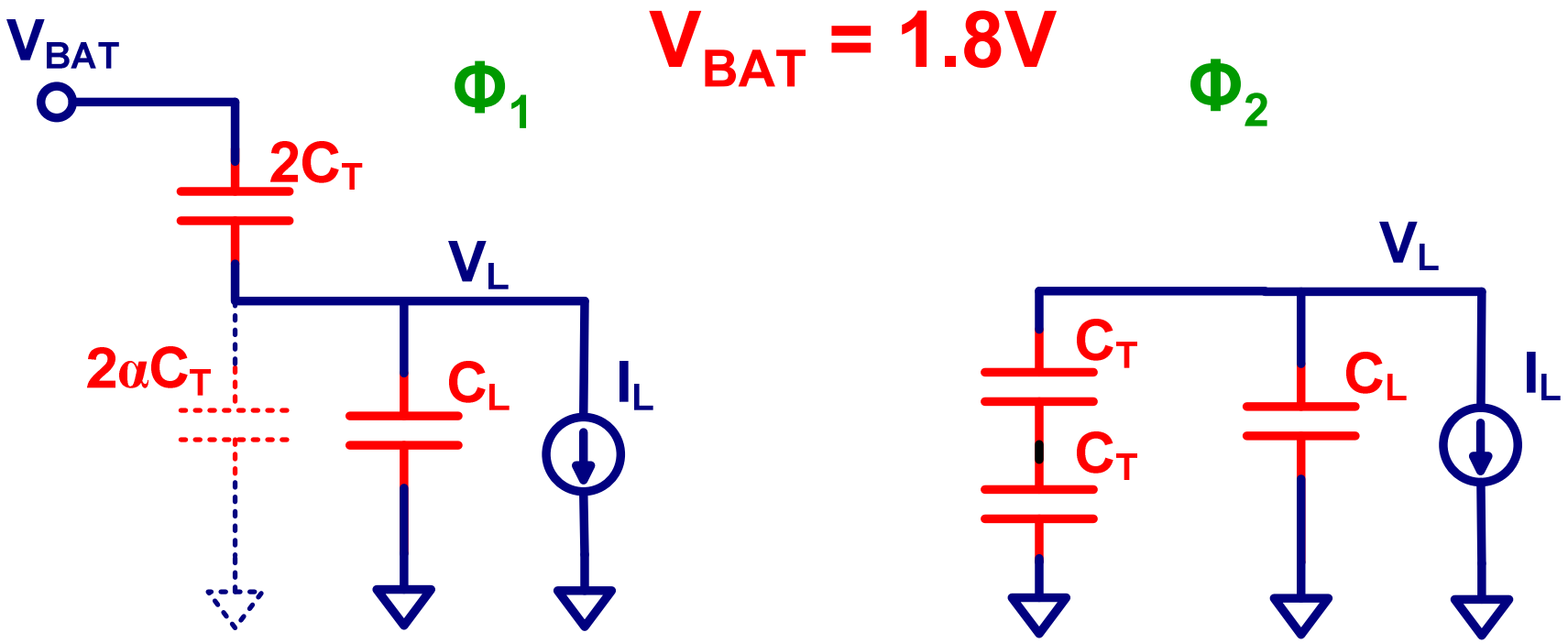


2BY3 Gain Setting

Provides voltages between 0.8V – 1V

On-chip, high efficiency alternative to linear regulators

Operation and Loss Mechanisms



- **Conduction Loss**
- **Bottom-plate Loss**
- **Switching and Control Loss**

$$\eta_{max} = \frac{V_L}{1.2}$$

Regulating the load voltage

$$I_L = Q_L f_s = 4.5 C_T \left(1.2 - V_L\right) f_s$$

Load voltage V_L needs to be regulated with change in load current I_L

- **Change f_s**
  - **Variable frequency control**
- **Problems:**
  - **Frequency of tones (spurs) cannot be controlled**

Fixed Frequency Control

$$I_L = Q_L f_s = 4.5 C_T \left(1.2 - V_L\right) f_s$$

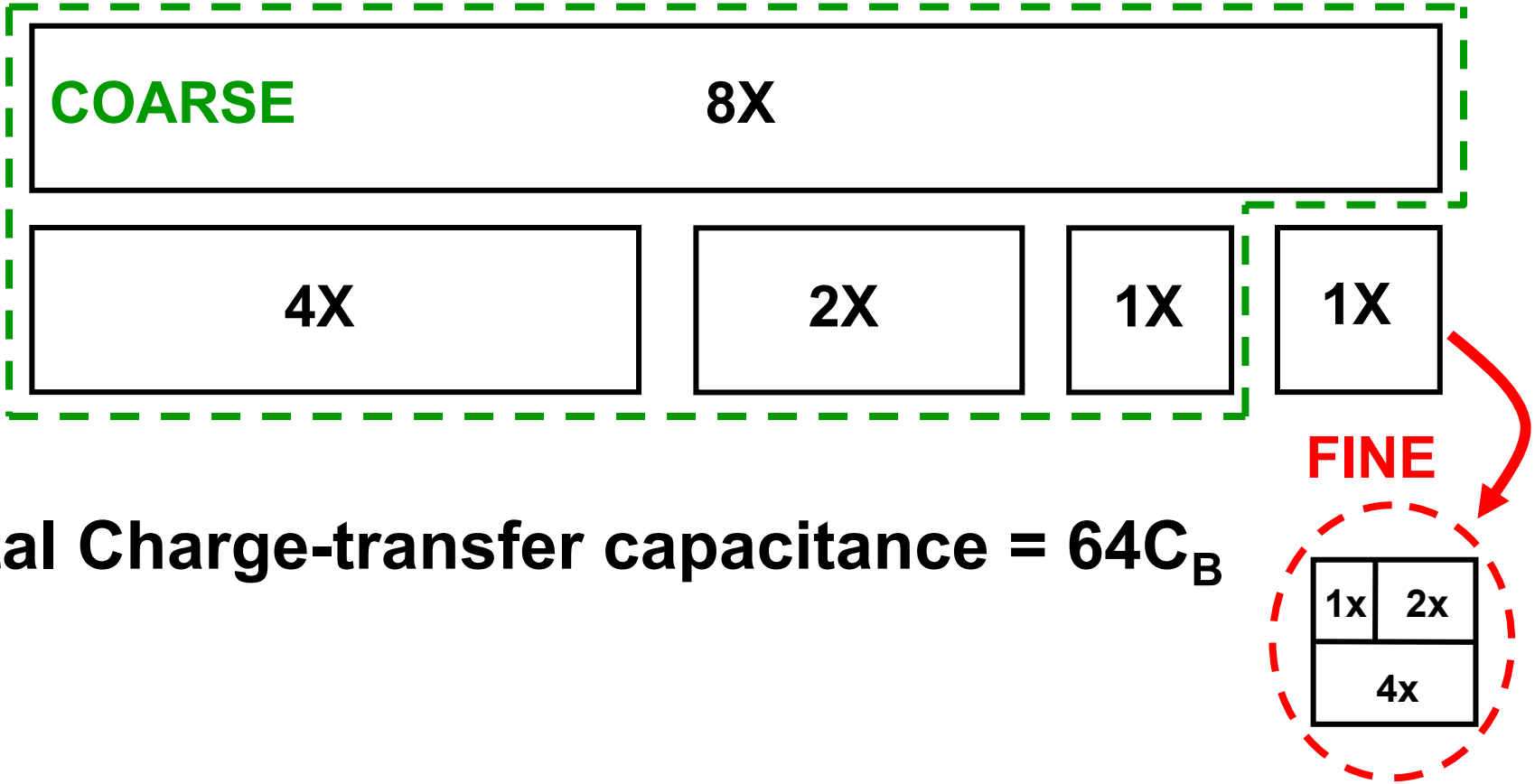
- **Change Q_L *(Charge Delivered to Load/Cycle)***
  - **Duty cycle control, segmented switch widths**
- **Problems:**
  - **Switching and bottom-plate losses do not scale**
  - **Process variations affect level of control**

Fixed Frequency Control

$$I_L = Q_L f_s = 4.5 C_T \left(1.2 - V_L\right) f_s$$

- **Change C_T *(Charge-Transfer Capacitance)***
  - **Segmented capacitive banks control**
  - **Losses scale well with load current**
  - **More immune to process variations**

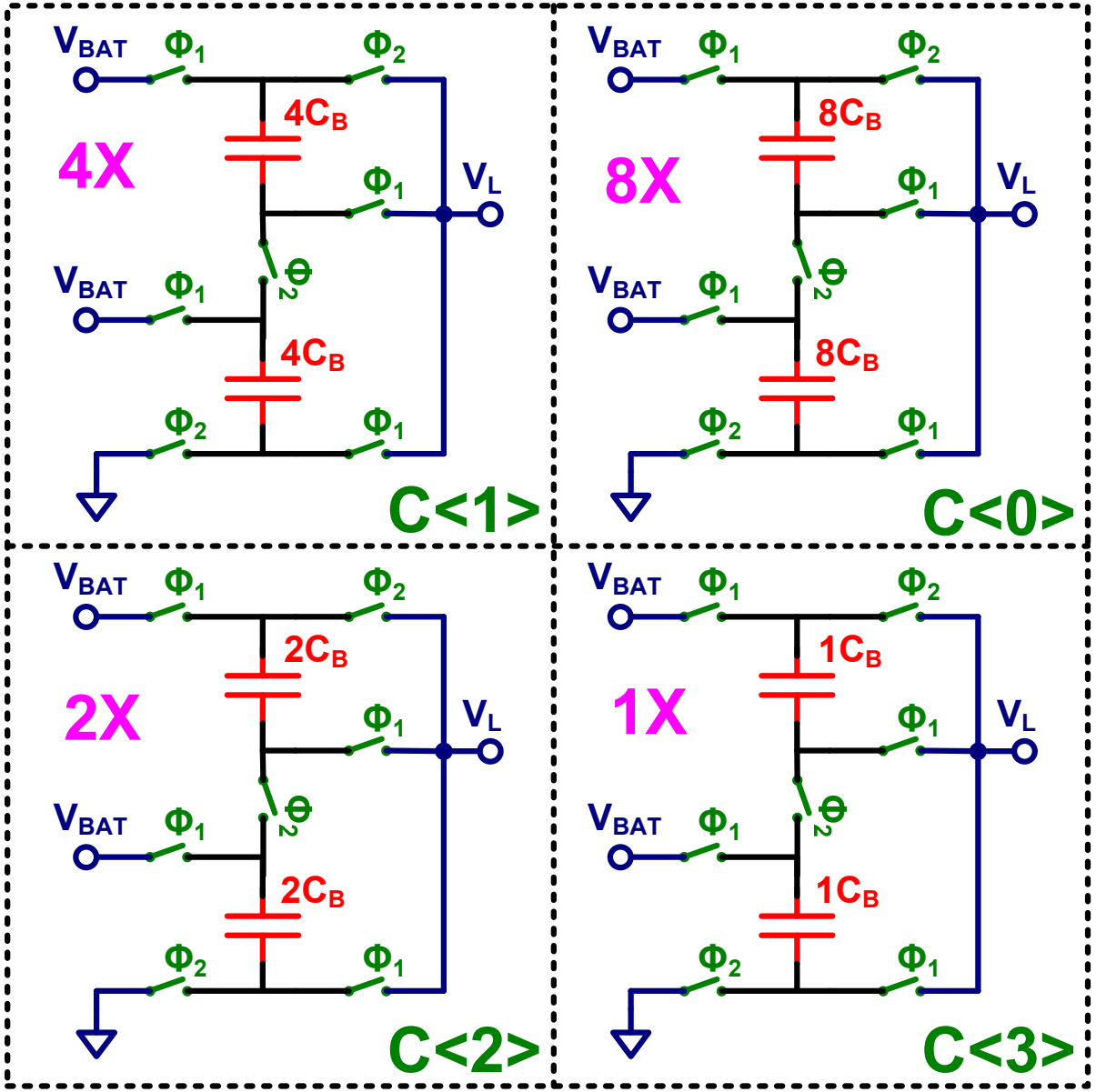
Digital Capacitance Modulation (DCM)



Total Charge-transfer capacitance = $64C_B$

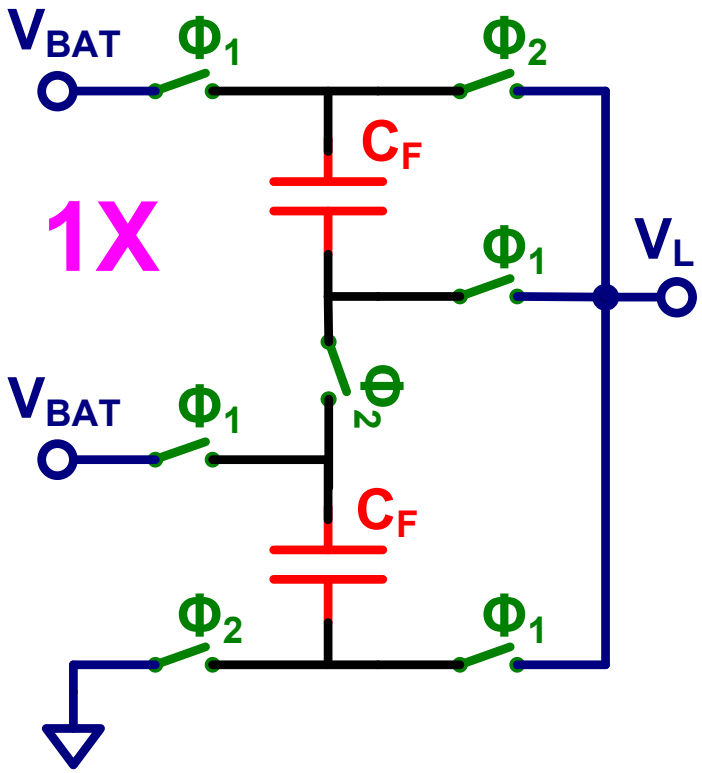
Charge-transfer capacitance split into binary-weighted banks

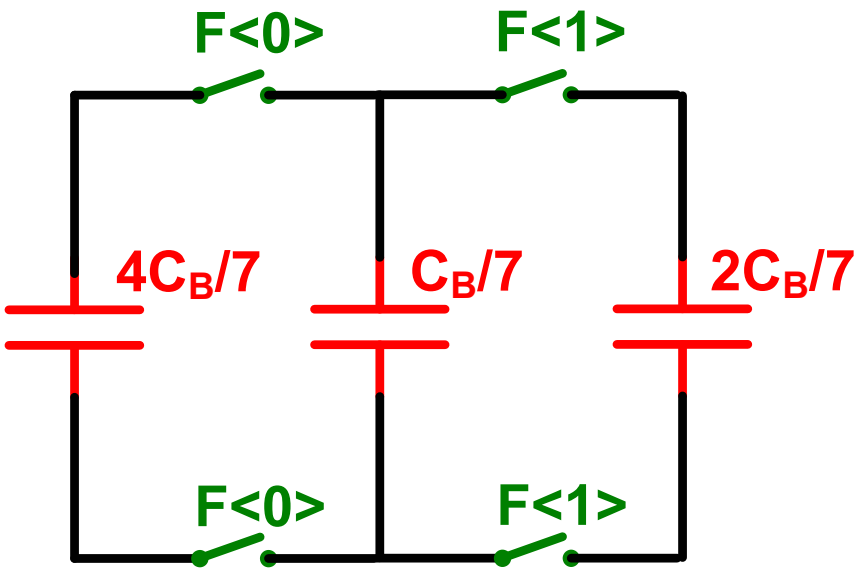
Coarse Splitting of Charge-Transfer Cap



Switch sizes scale with capacitance

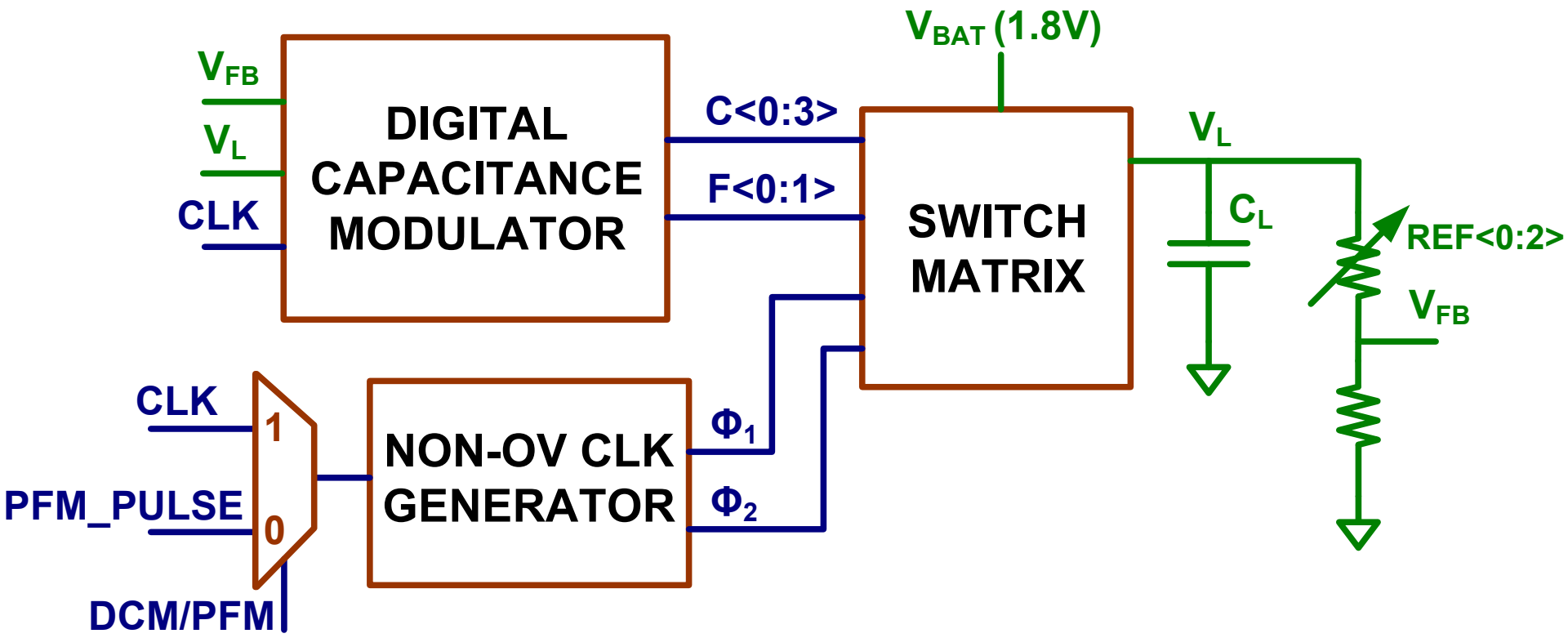
Fine Splitting of Charge-Transfer Cap





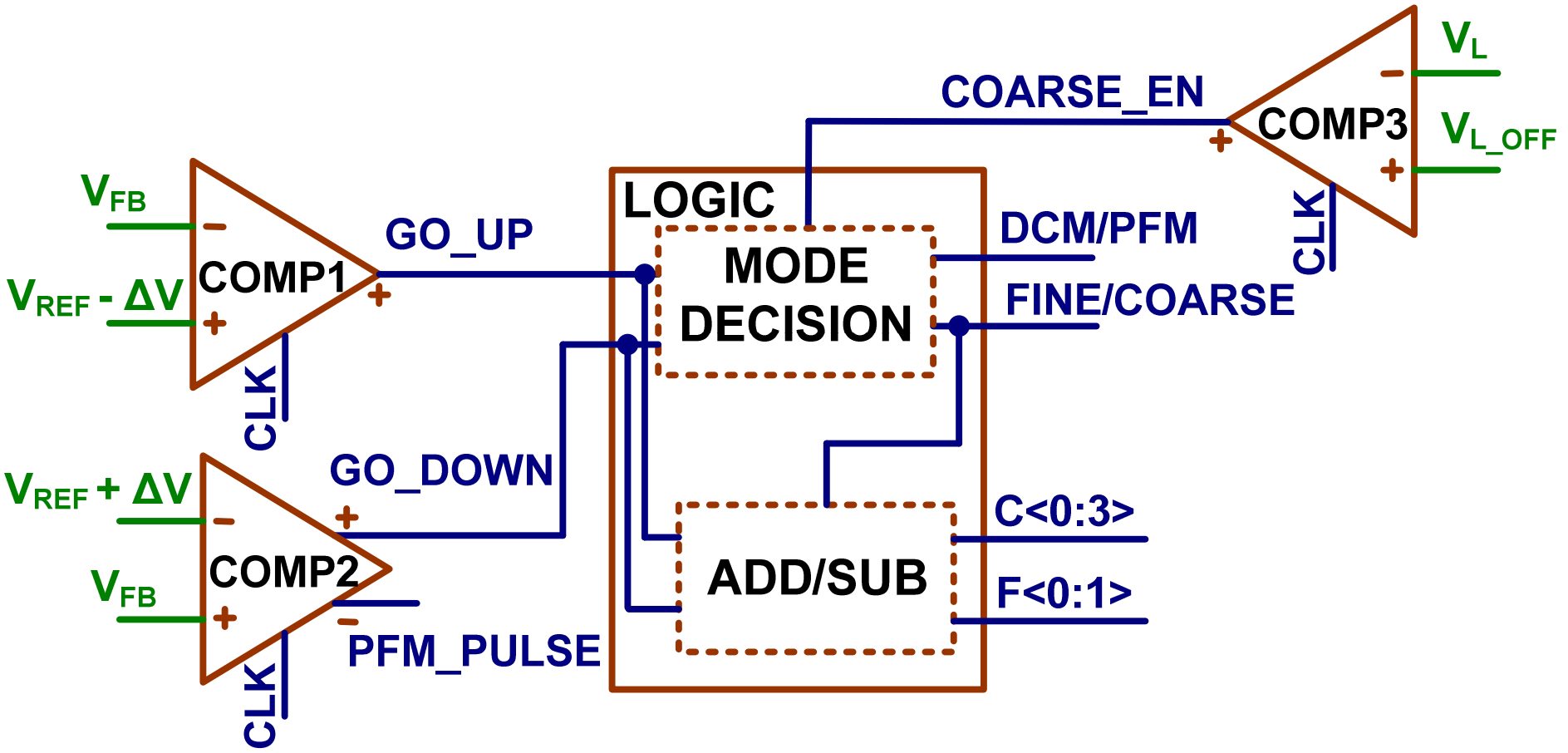
- FINE block is always ON
- C_F is split into three smaller capacitances

System Architecture



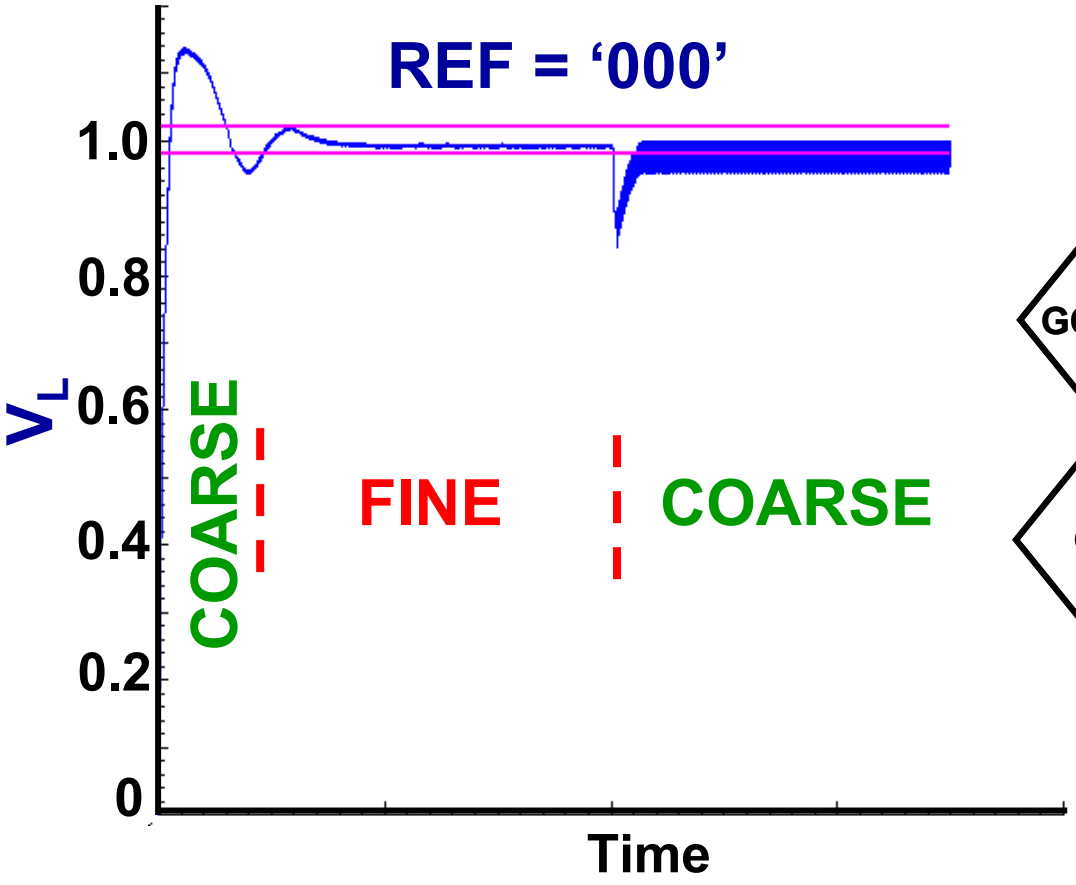
- All-digital multi-mode control
- Scalable output voltage (3 bits)

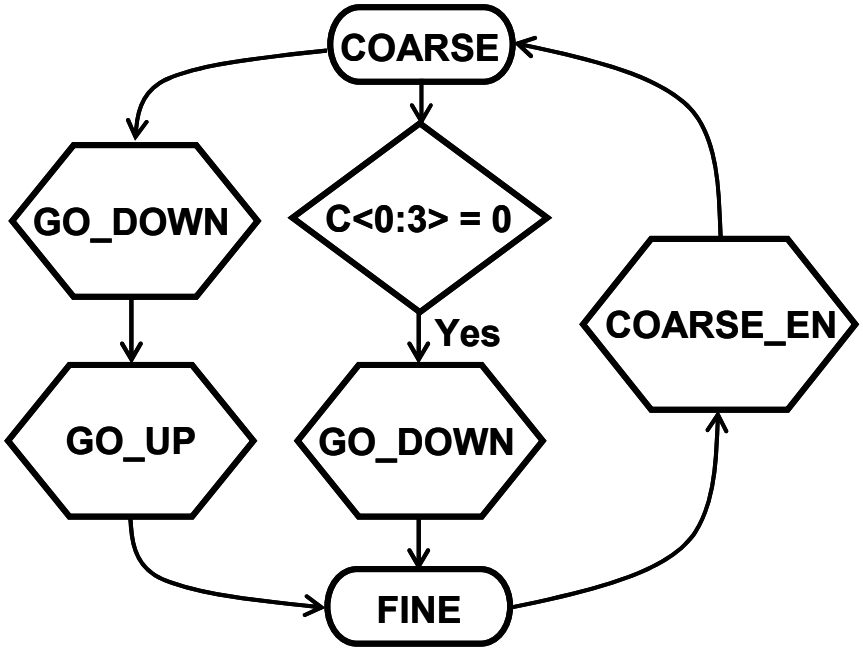
Digital Capacitance Modulator



- V_L regulated within a hysteretic band
- Determines the mode of operation

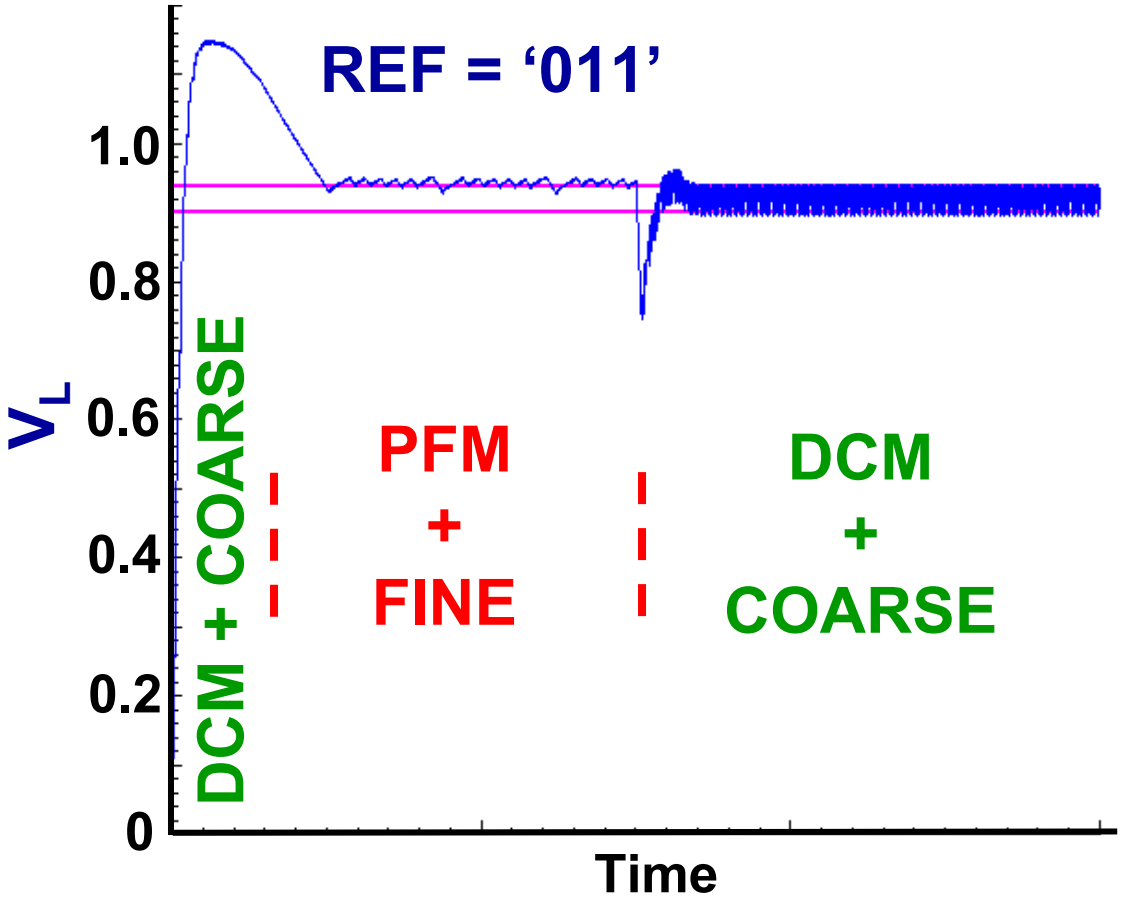
FINE/COARSE Control

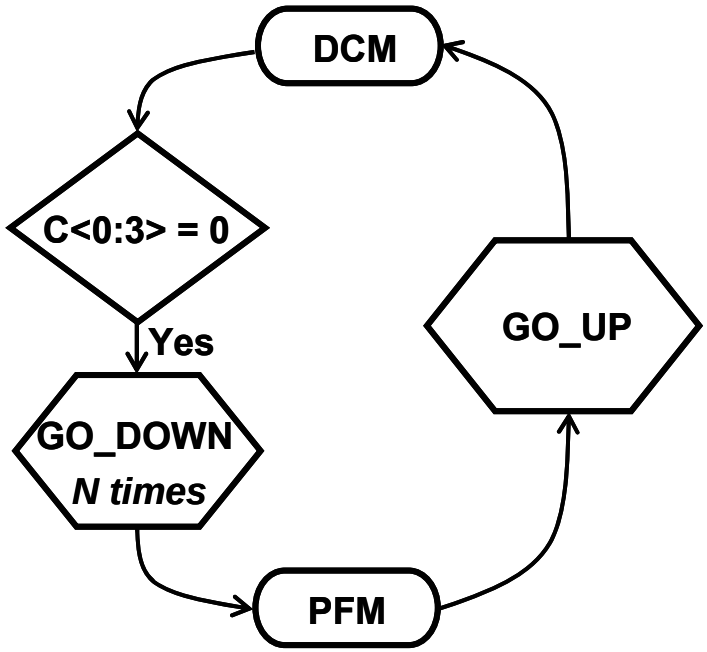




- COARSE Control - Faster Transient Response
- FINE Control - Better Settling, Prevents unwanted oscillations

DCM/PFM Control

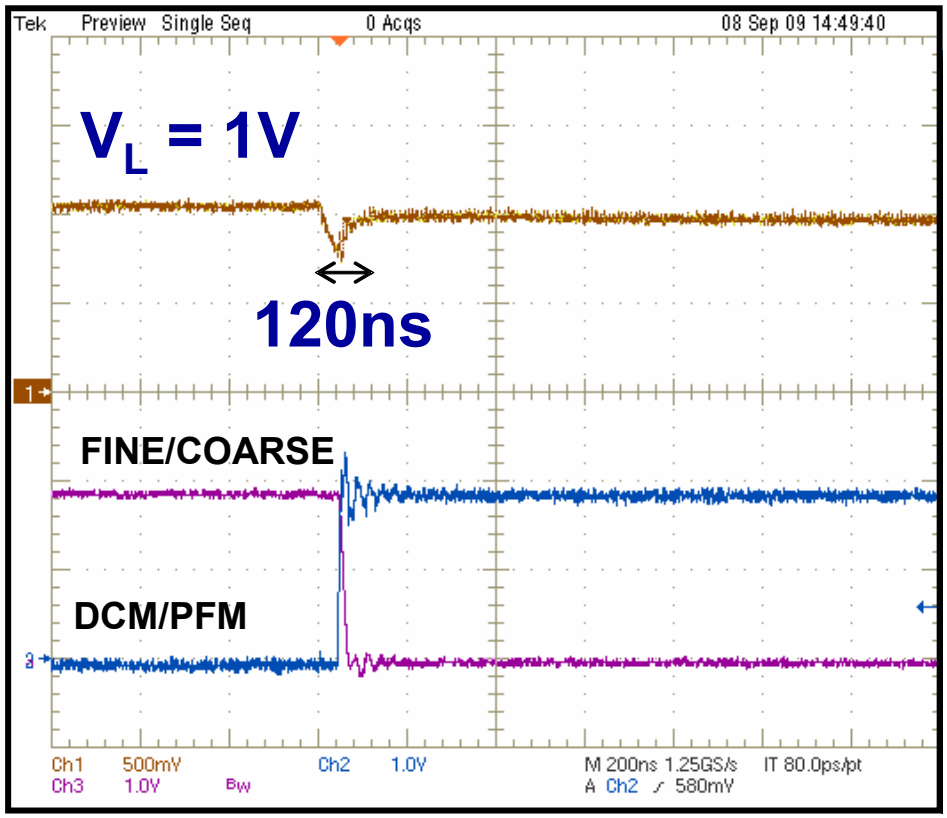


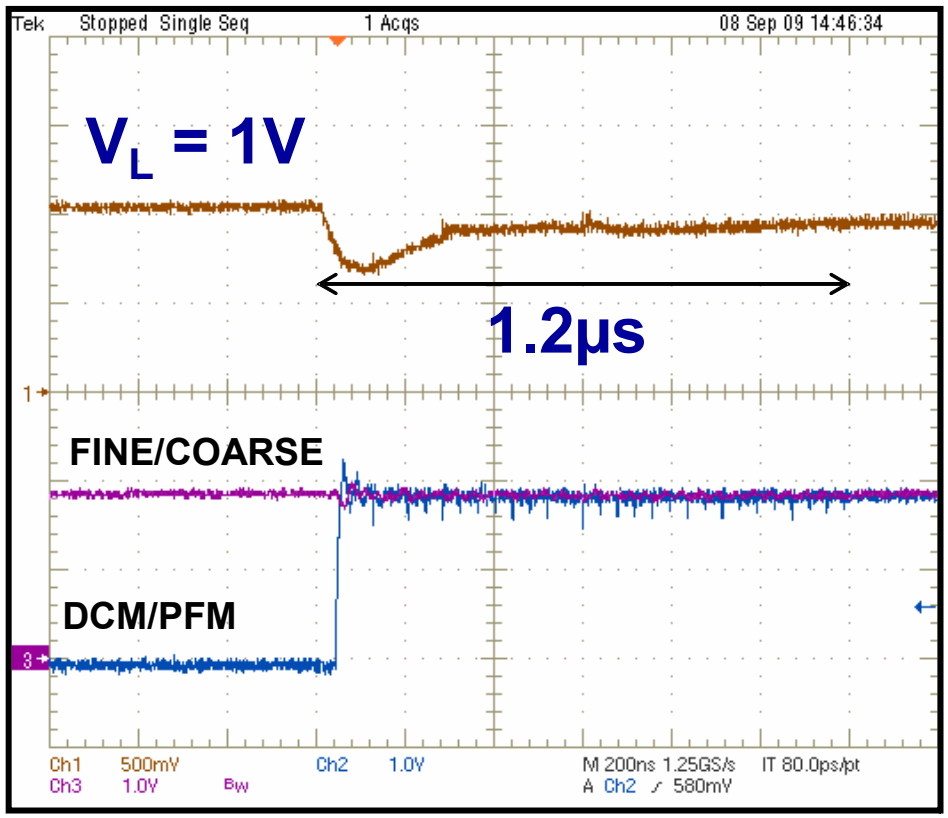


- DCM Control - Constant Frequency Control
  - Scalable Losses to maintain constant efficiency
- PFM Control - Improve efficiency at light load

Transient Performance

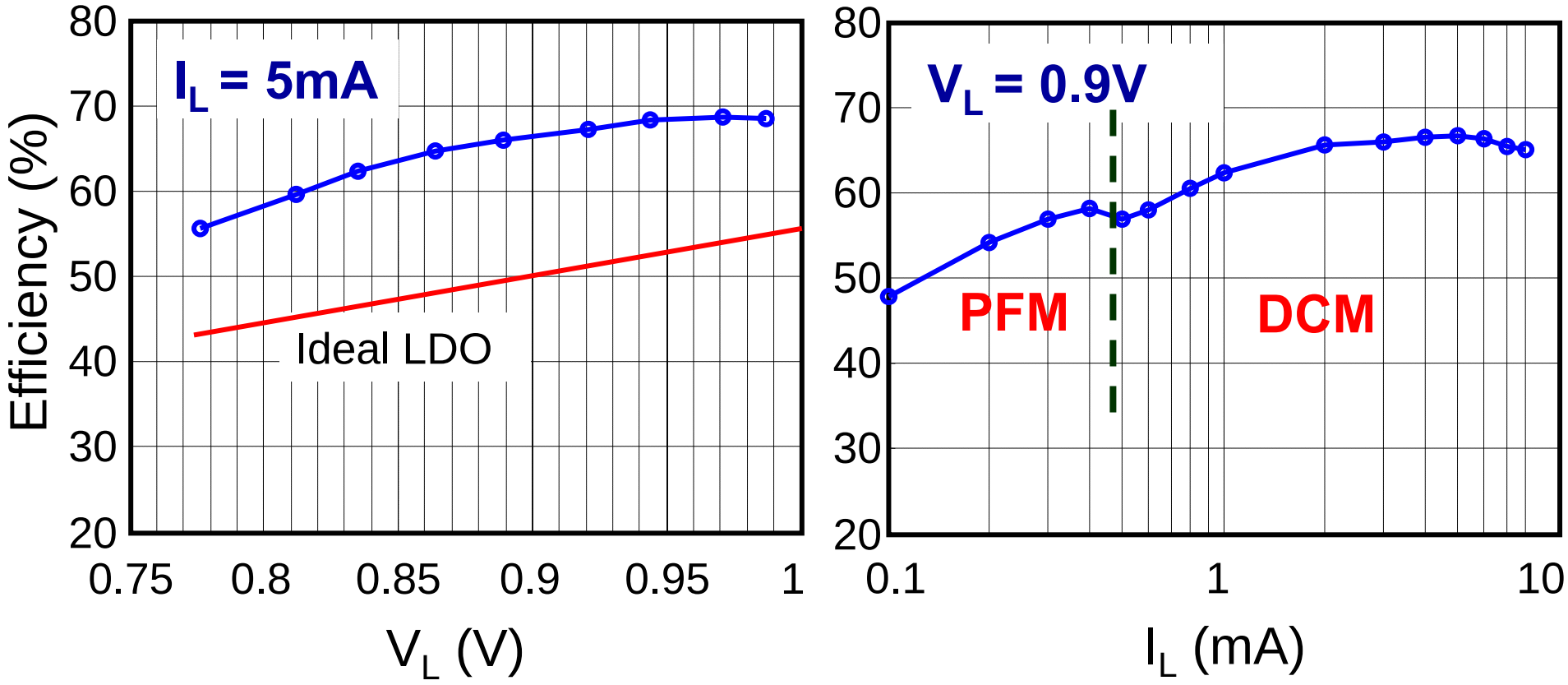
REF='000' : I_L = 270µA → 7.6mA





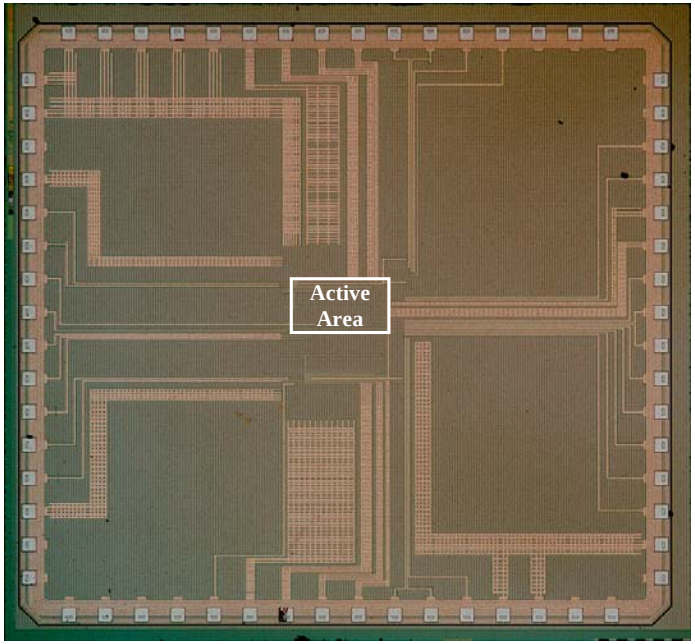
COARSE_EN enables faster settling

Efficiency



- **15-20% more efficiency than a linear regulator**
- **PFM mode control improves light load efficiency**

Summary



Technology	45nm CMOS
Active Area	0.16mm^2
Switching Frequency	30MHz
Input Voltage	1.8V
Maximum Load Current	8mA
Charge Transfer Cap.	534pF
Load Capacitance	700pF

- **Completely on-chip switched capacitor converter**
- **Digital Capacitance Modulation scheme provides scalable output voltages at high efficiencies**
- **Multi-mode control allows fast transients with fine settling**