# Non-Linear Operating Point Analysis for Local Variations in Logic Timing at Low-Voltage

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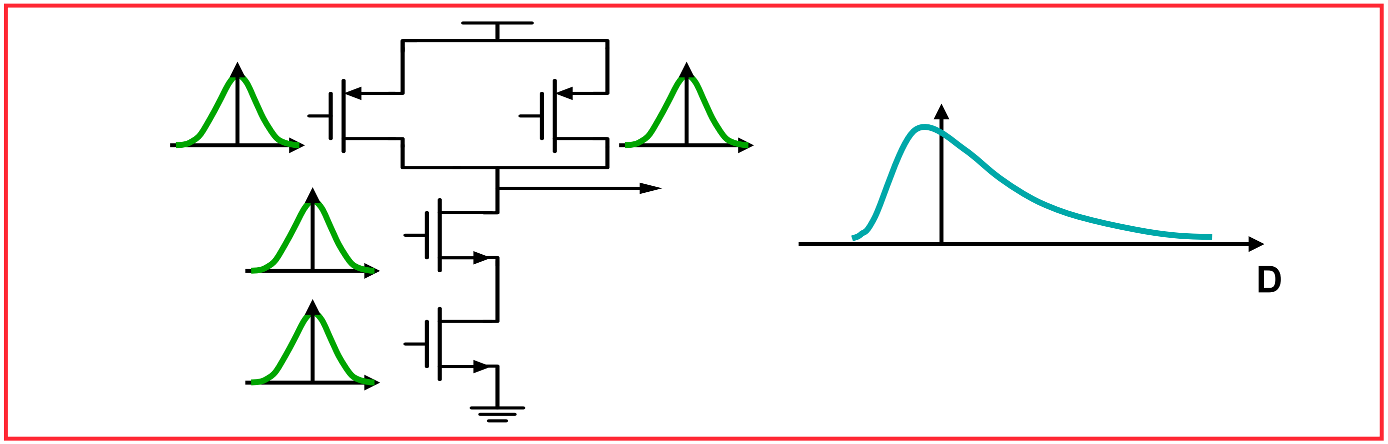
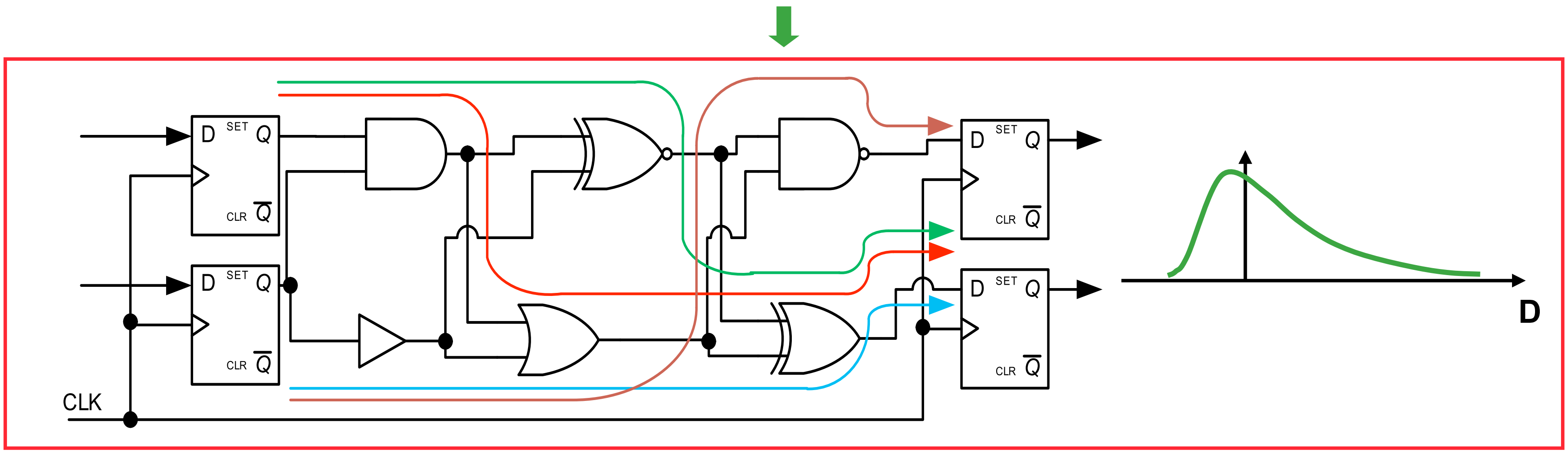
# Overview

- For technology nodes of 65nm and below, local transistor variations become increasingly significant for logic timing
- At nominal VDD:
  - delay varies linearly with local parameter variations
  - leads to Gaussian probability density function (PDF) for delay
- At ultra-low voltage (ULV) (VDD near threshold):
  - delay varies non-linearly with local transistor parameter variations
  - leads to non-Gaussian delay PDF
- This work addresses:
  - accurately predicting statistical circuit performance for ULV
  - developing computationally efficient methodology
  - integrating with commercially used timing analysis tools

# Motivation

**Goal: To determine statistical circuit performance, given by 3σ (in general, fσ) stochastic delay**



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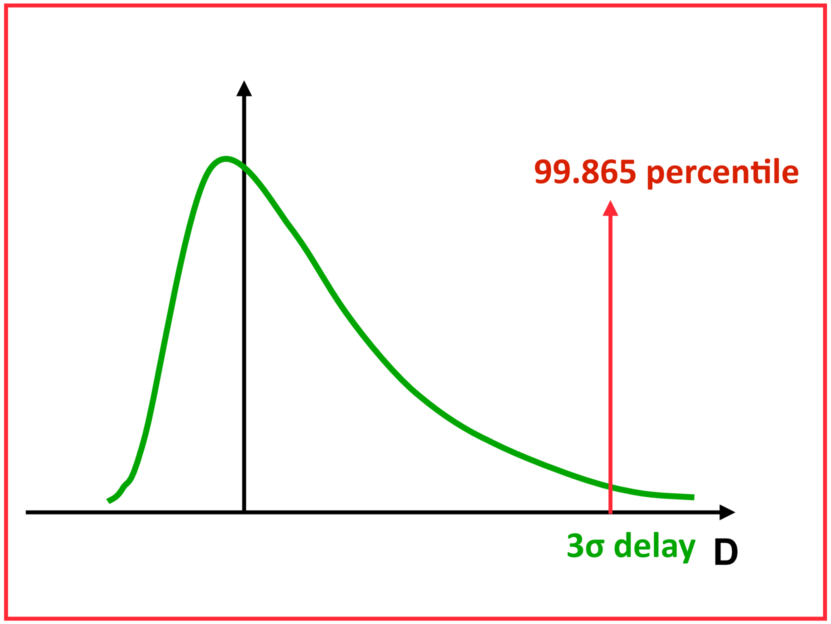
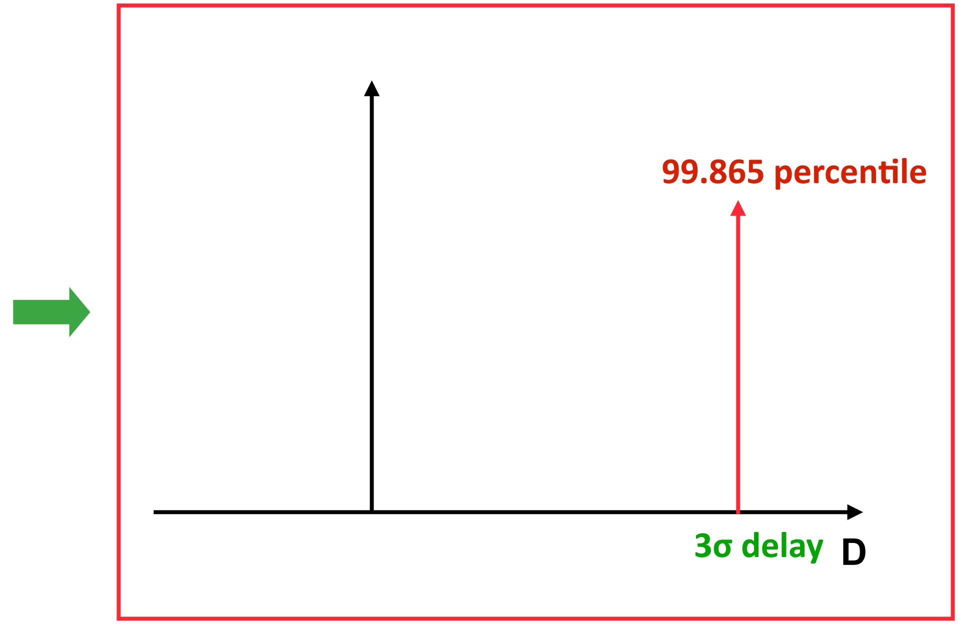
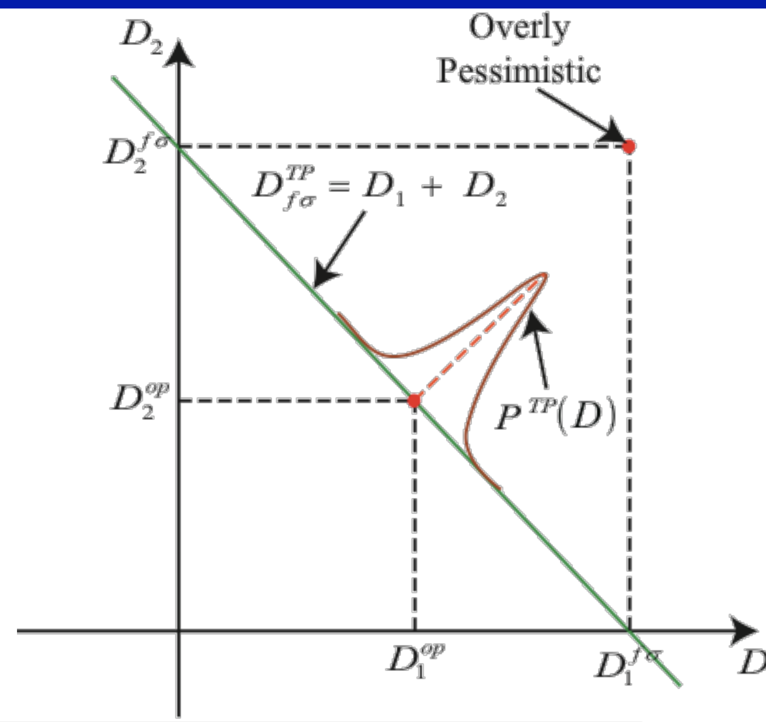



**Can we determine the 3σ-delay (in general, fσ-delay) without computing the entire delay PDF for the timing path?**

# Linear-Gaussian Theory

- **Consider a 2-stage timing path (TP)**
- **Assume that individual cell delay PDFs are Gaussian and TP delay is a linear function of cell delays**
- **Timing path delay PDF is the convolution of cell delay PDFs**




$$P^{TP}(D_{f\sigma}^{TP}) = \int_{-\infty}^{\infty} P_1(D)P_2(D_{f\sigma}^{TP} - D)dD$$

$$P^{TP}(D_{f\sigma}^{TP}) = k_1 \exp\left(\frac{-(D_{f\sigma}^{TP})^2}{2(\sigma_1^2+\sigma_2^2)}\right)\int_{-\infty}^{\infty} \exp\left(\frac{-(\sigma_1^2+\sigma_2^2)(D - \frac{\sigma_1^2}{\sigma_1^2+\sigma_2^2}D_{f\sigma}^{TP})^2}{2\sigma_1^2\sigma_2^2}\right)dD$$

$$= k_1 \exp\left(\frac{-(D_{f\sigma}^{TP})^2}{2(\sigma_1^2+\sigma_2^2)}\right)$$

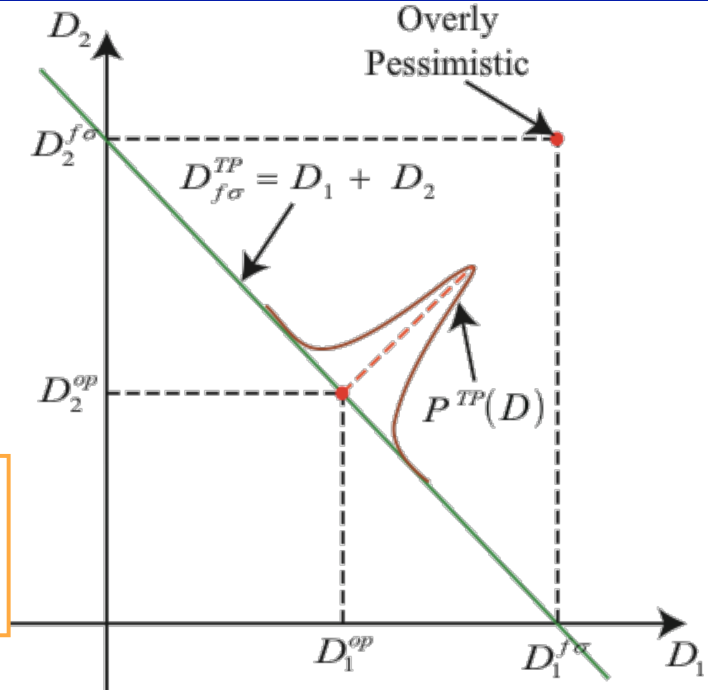
Gaussian with $\sigma = \sqrt{\sigma_1^2 + \sigma_2^2}$

# Linear-Gaussian Theory

$$\exp\left(\frac{-(\sigma_1^2+\sigma_2^2)(D-\frac{\sigma_1^2}{\sigma_1^2+\sigma_2^2}D_{f\sigma}^{TP})^2}{2\sigma_1^2\sigma_2^2}\right)$$

Integrand of the convolution integral has a point of maxima at:

$$D_1^{op}=\frac{\sigma_1^2}{\sigma_1^2+\sigma_2^2}D_{f\sigma}^{TP} \quad \text{and} \quad D_2^{op}=\frac{\sigma_2^2}{\sigma_1^2+\sigma_2^2}D_{f\sigma}^{TP}$$




**The point of maxima is called the operating point**

**In the vicinity of the operating point:**

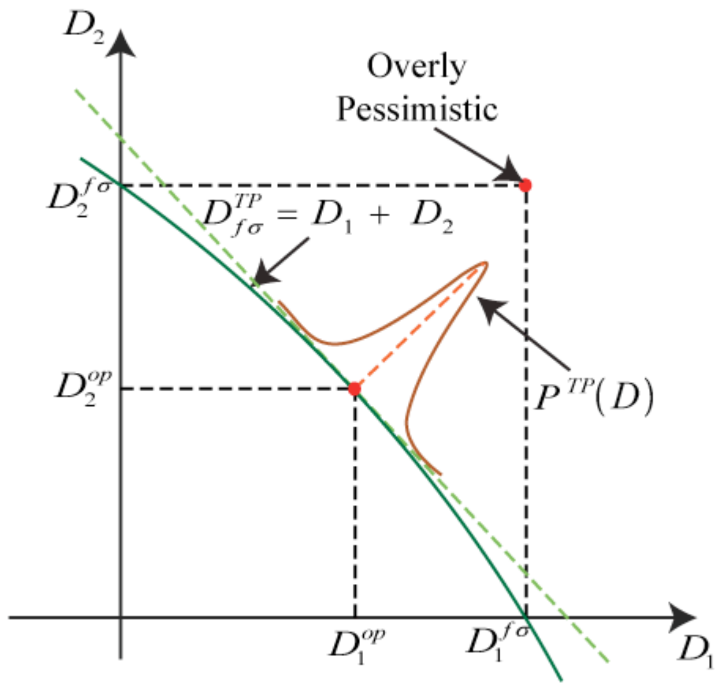
- **The integrand falls-off sharply**
- **Only points in the immediate vicinity of the operating point contribute significantly towards convolution**

# Non-Linear – Non-Gaussian Case

- Cell delays are non-Gaussian
- TP delay is a non-linear function of cell delays

In the vicinity of the operating point:

- Non-linear delay curve can be linearized
- Cell delay PDFs can be approximated as Gaussian with an 'effective' sigma




**Linear-Gaussian Theory applies in the vicinity of the Operating Point**

# Gaussian Mapping: D-space to ξ-space

- **Non-linear delay PDF mapped on a Gaussian parameter ξ**
- **Mapping through a non-linear Cell/Arc Delay Function (CADF)**
- **Mapping based on:**

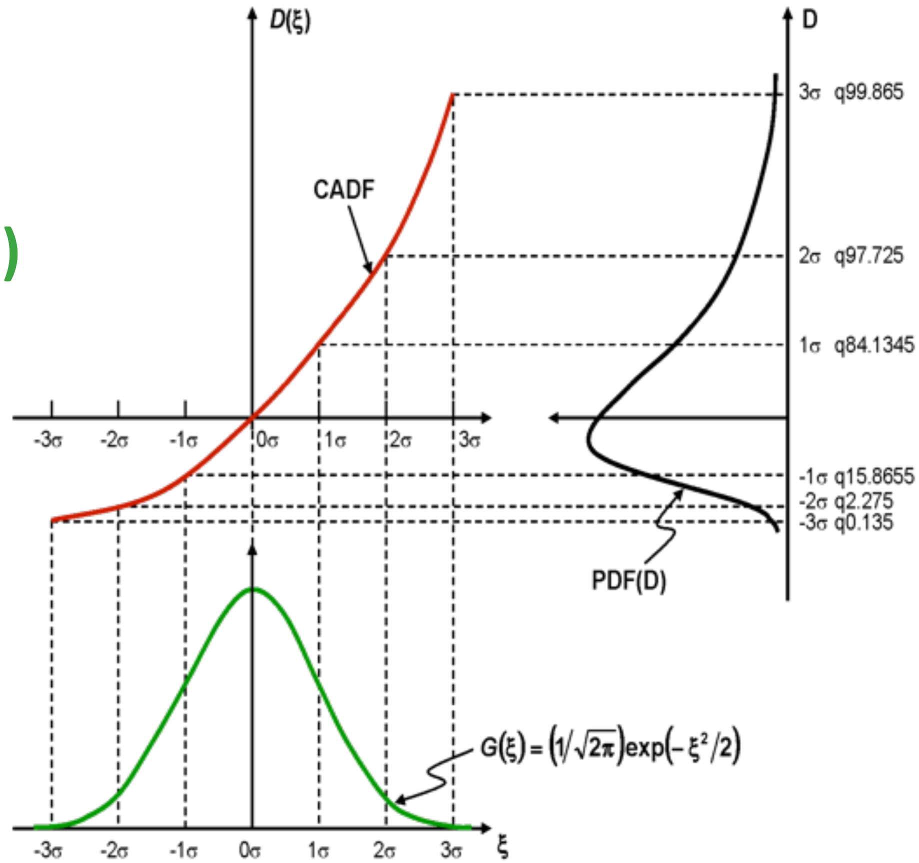
$$\int_{-\infty}^{f} G(\xi)d\xi = \int_{-\infty}^{D_{f\sigma}} P(D)dD$$

- **If the PDF is Gaussian:**

$$D(\xi) = \sigma\xi$$

- **If the PDF is non-Gaussian:**

$\frac{\partial D}{\partial \xi}\Big|_{\xi_0}$ **is the 'effective' sigma**



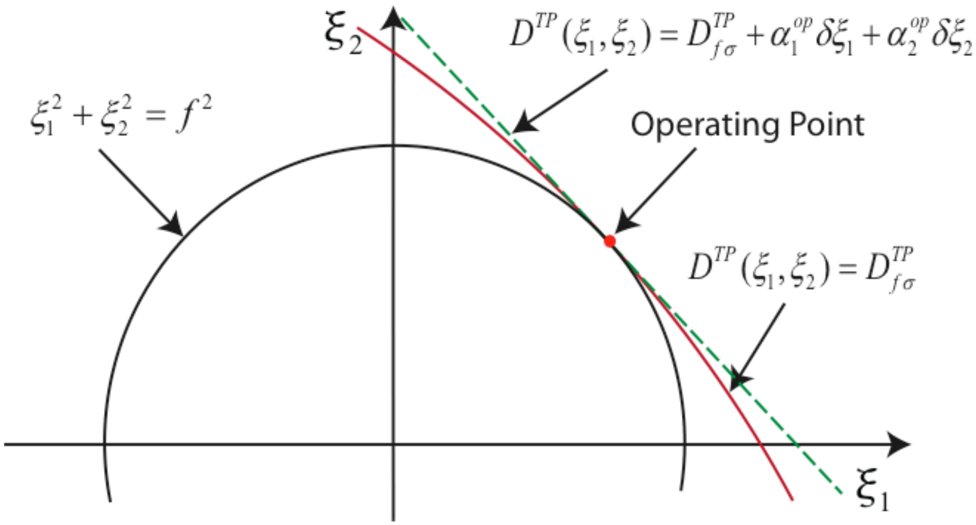
# Operating point in ξ-space

- In ξ-space, **lines of constant probability:** hyper-spheres
- **Operating point becomes the point of tangency of the hyper-plane:**

$$D^{TP}(\xi_1, \xi_2, \ldots \xi_N) = D^{TP}_{f\sigma}$$

**and the hyper-sphere:**

$$\sum_{i=1}^{N} \xi_i^2 = f^2$$




The operating point can be determined by solving the self-consistent equation:

$$\xi_i^{op} = \frac{f\alpha_i^{op}}{\sqrt{\sum_{j=1}^{N}(\alpha_j^{op})^2}}$$

**where,**

$$\alpha_i^{op} = \left(\frac{dD^{TP}}{d\xi_i}\right)_{op} = \left(\frac{\partial D^{TP}}{\partial D_i}\right)_{op}\left(\frac{\partial D_i}{\partial \xi_i}\right)_{op}$$

# Timing Path Analysis

- **Once the operating point is determined, the *f*-sigma timing path delay can be computed as:**

$$D_{f\sigma}^{TP} = D^{TP}(\xi_1, \xi_2, \ldots.\xi_N) \approx \sum_{i=1}^{N} D_i(\xi_i^{op})$$

- **However, in real timing paths the delay and slew are highly correlated**
  - **Output slew of one stage is the input slew to the next stage**
  - **The delay and output slew of a stage depends on all the previous stages**
  - **Makes all the stages in the design correlated**

# Effect of correlation

**Taking into account the correlations between cell delays in the TP, the modified operating point can be given as:**

$$\xi_i^{op} = \frac{f(\alpha_i + \eta_i + \lambda_i)}{\sqrt{\sum_{i=1}^{N} (\alpha_i + \eta_i + \lambda_i)^2}}$$

where,

$$\alpha_i = \frac{dD_i}{d\xi_i}$$

$$\eta_i = \frac{dD_{i+1}}{d\xi_i} = \left(\frac{dD_{i+1}}{dS_i}\right)_{op} \left(\frac{dS_i}{d\xi_i}\right)_{op}$$

$$\lambda_i = \frac{dD_{i+2}}{d\xi_i} = \left(\frac{dD_{i+2}}{dS_{i+1}}\right)_{op} \left(\frac{dS_{i+1}}{dS_i}\right)_{op} \left(\frac{dS_i}{d\xi_i}\right)_{op}$$

**The fσ TP delay can be given as:**

$$D_{TP}^{f\sigma}(\xi_1,..\xi_N) = \sum_{i=1}^{N} D_i(\xi_i^{op}) + \sum_{i=1}^{N-1} \left(\frac{dD_{i+1}}{dS_i}\right)_{op} S_i(\xi_i^{op}) + \sum_{i=1}^{N-2} \left(\frac{dD_{i+2}}{dS_{i+1}}\right)_{op} \left(\frac{dS_{i+1}}{dS_i}\right)_{op} S_i(\xi_i^{op})$$

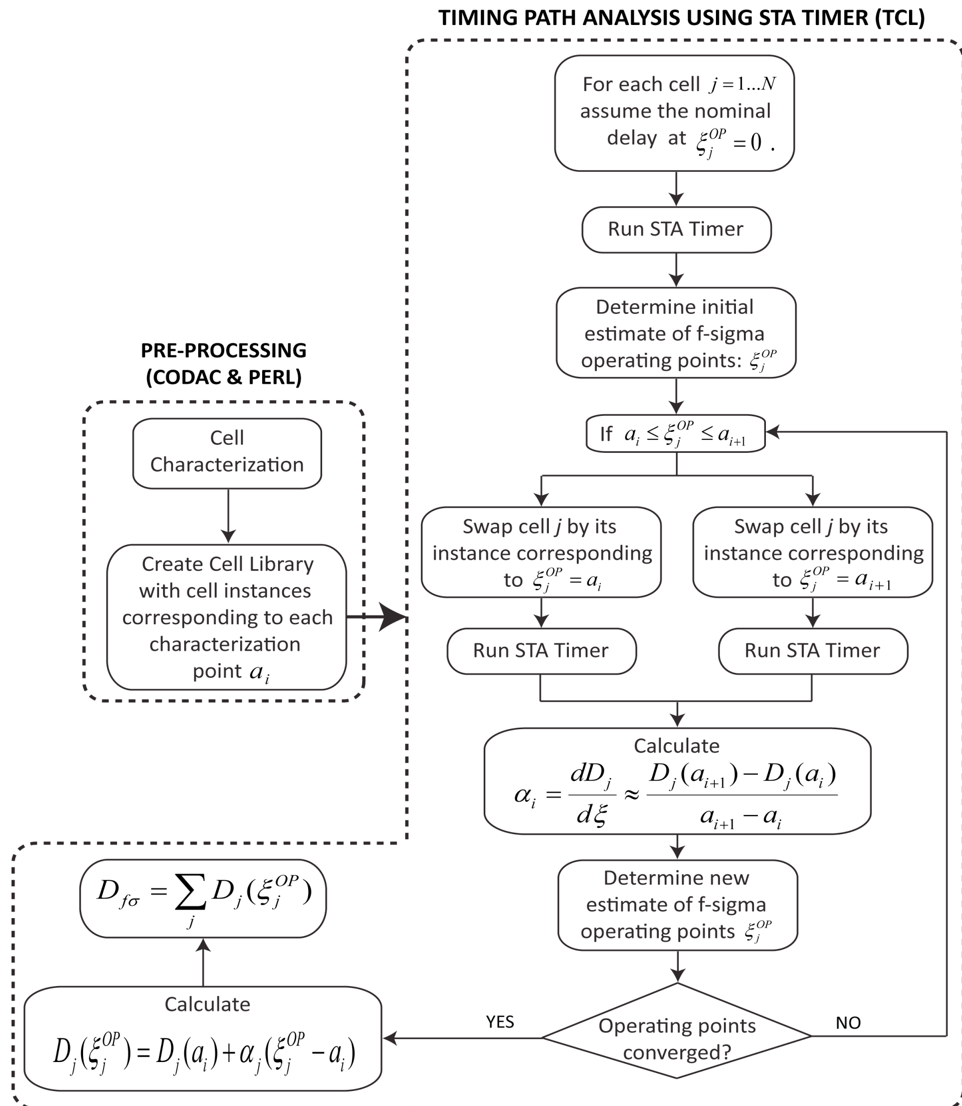
# Integration with CAD Flow

- **NLOPALV approach implemented using commercial CAD tools**
- **Integrated into standard design flow**
- **Single script operating around the STA timer performs entire analysis**

**Library Characterization: One-time effort**

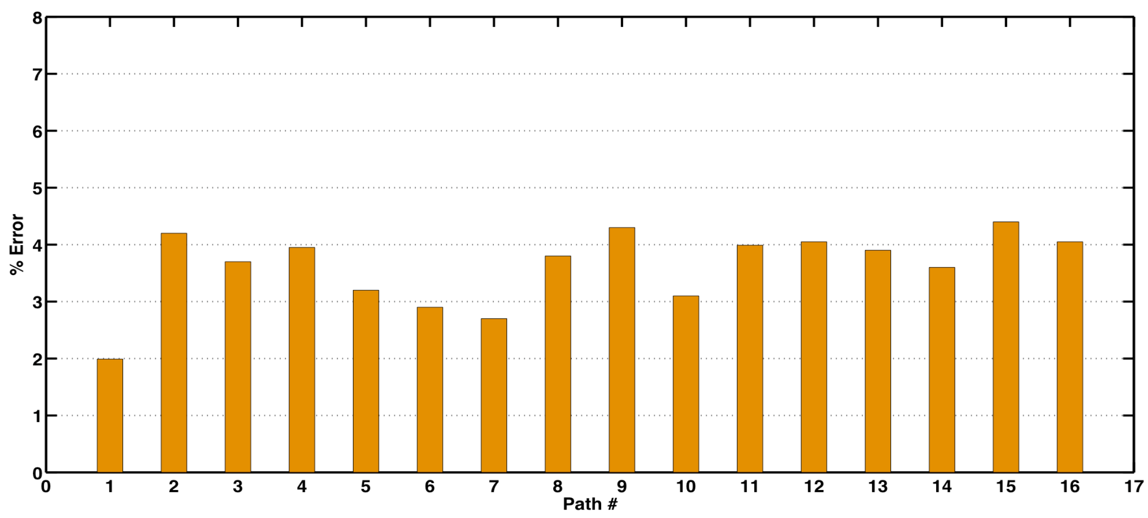
**TP analysis: 50 stage TP**

| | NLOPALV | Monte-Carlo |
|---|---|---|
| SPICE sims. | None | 10,000 |
| Run time | 10 sec | 3 hours |



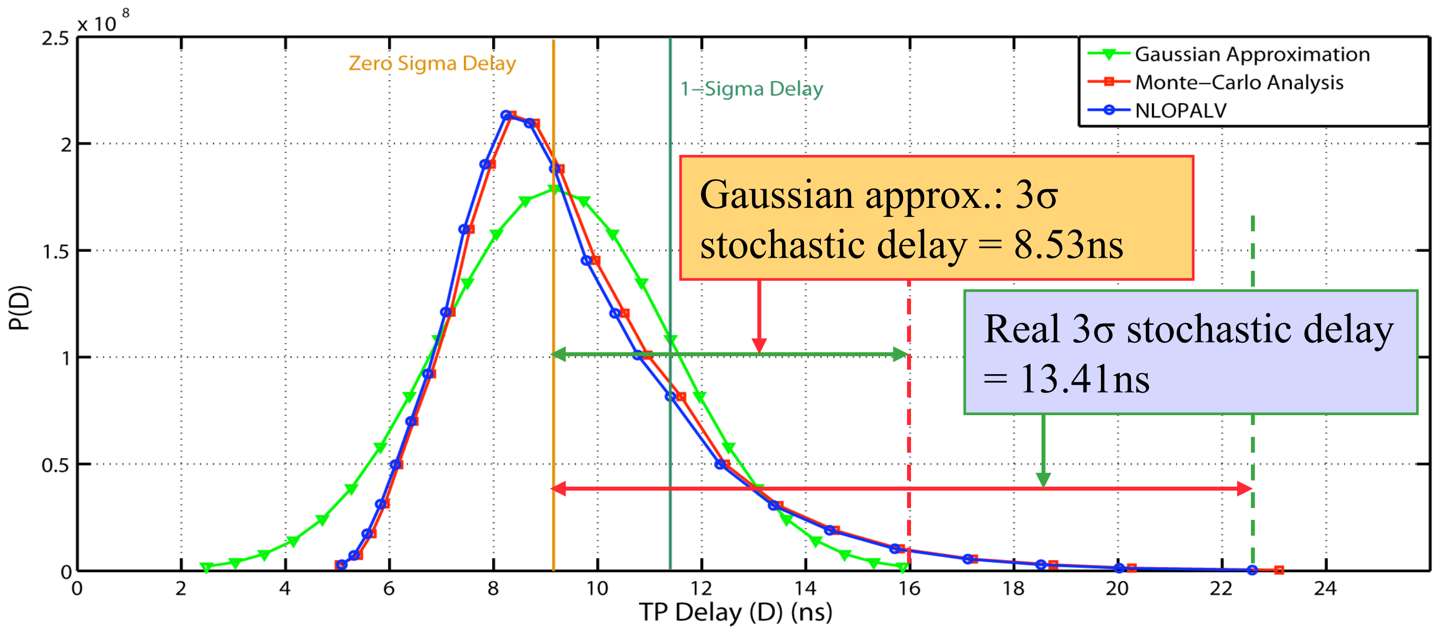
# TP analysis: Validation

- **Validation:** **logic paths taken from a commercial DSP implemented in 28nm CMOS technology operating at 0.5V**
- **3σ delay from the TP analysis flow is compared with 10k point Spice based Monte-Carlo simulations**




**Accuracy:** within 5% compared to Monte-Carlo

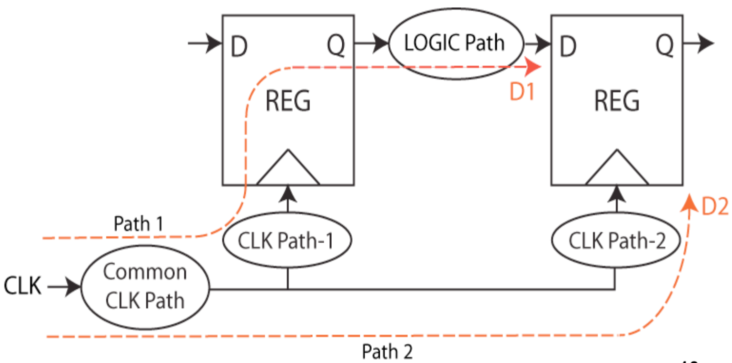
# TP analysis: Validation (cont..)




- **Excellent agreement between TP analysis and Monte-Carlo**
- **The 3σ stochastic delay: 13.41ns, nominal delay: 9.17ns**
- **Variations can be higher than the nominal delay at low voltage**
- **The 3σ stochastic delay with Gaussian approximation: 8.53ns**
- **Gaussian approximation can lead to huge errors at low voltage**

# Setup/hold analysis

- 3σ setup/hold slack computed using TP analysis is compared with 10k point Monte-Carlo simulations

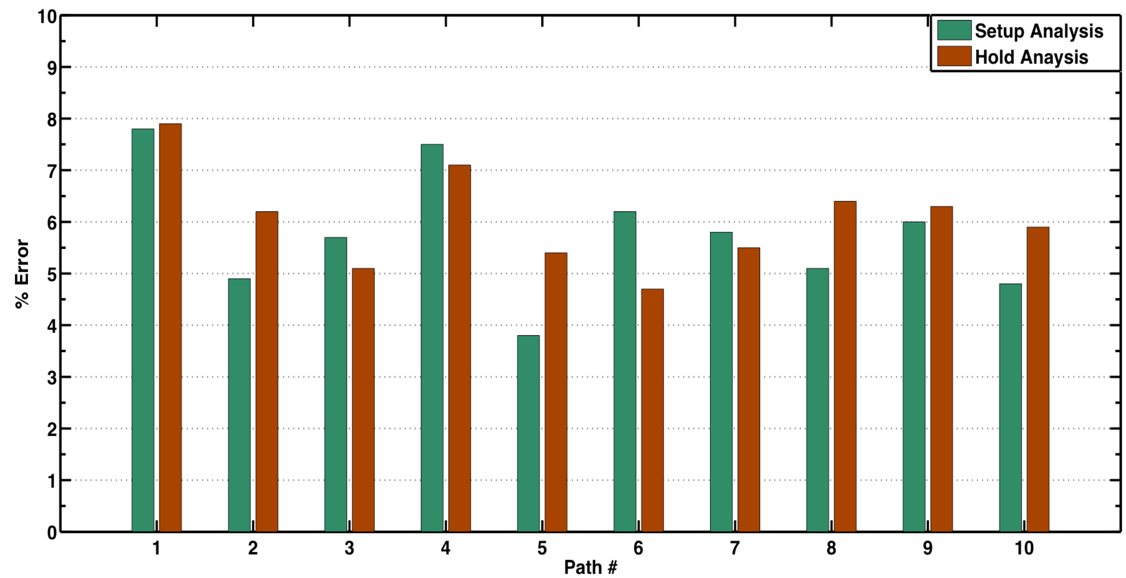



**Setup/hold constraints:**

$$(D_1 - D_2)_{-3\sigma} - T_{hold}^{3\sigma} > 0$$

$$(D_1 - D_2)_{3\sigma} + T_{setup}^{3\sigma} < T_{CLK}$$

**Accuracy: within 8% compared to Monte-Carlo**



# Conclusions

- **Computationally efficient approach** to calculate the stochastic delay in logic timing at low voltage
- Implemented using commercial STA tools and **integrated in the standard CAD flow**
- Verification on logic paths from a 28nm commercial DSP @ 0.5V demonstrates **high accuracy**
- **No expensive Monte-Carlo** simulations are required
- Approach can handle **non-Gaussian delay PDFs**
- Concept of **operating point** greatly **simplifies computations** for non-Gaussian statistics **without sacrificing accuracy**