A Resolution-Reconfigurable 5-to-10b 0.4-to-1V Power Scalable SAR ADC

Marcus Yip and Anantha P. Chandrakasan

Massachusetts Institute of Technology

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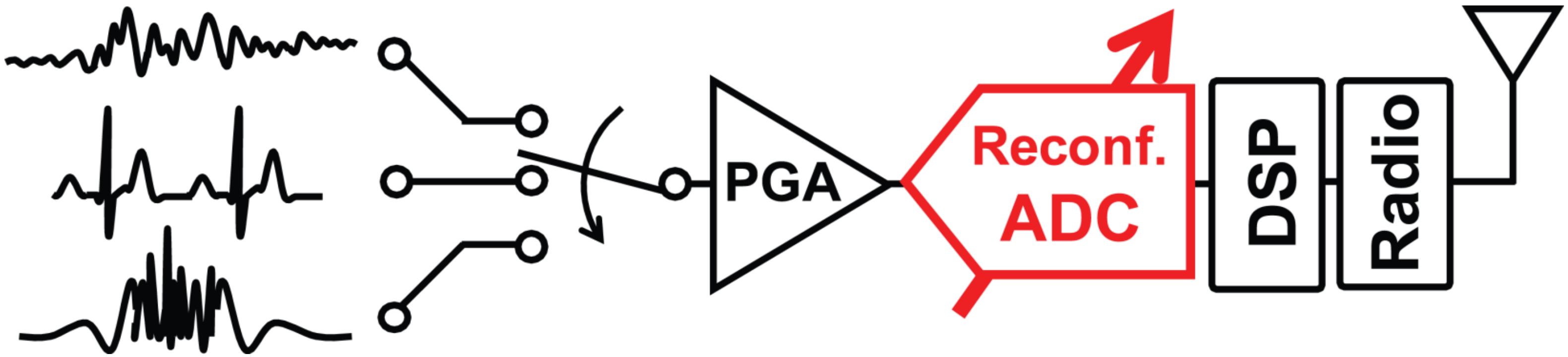
Motivation for Scalable ADC

- Bio-potentials vary in bandwidth and dynamic range
- DSP algorithms have varying resolution requirements



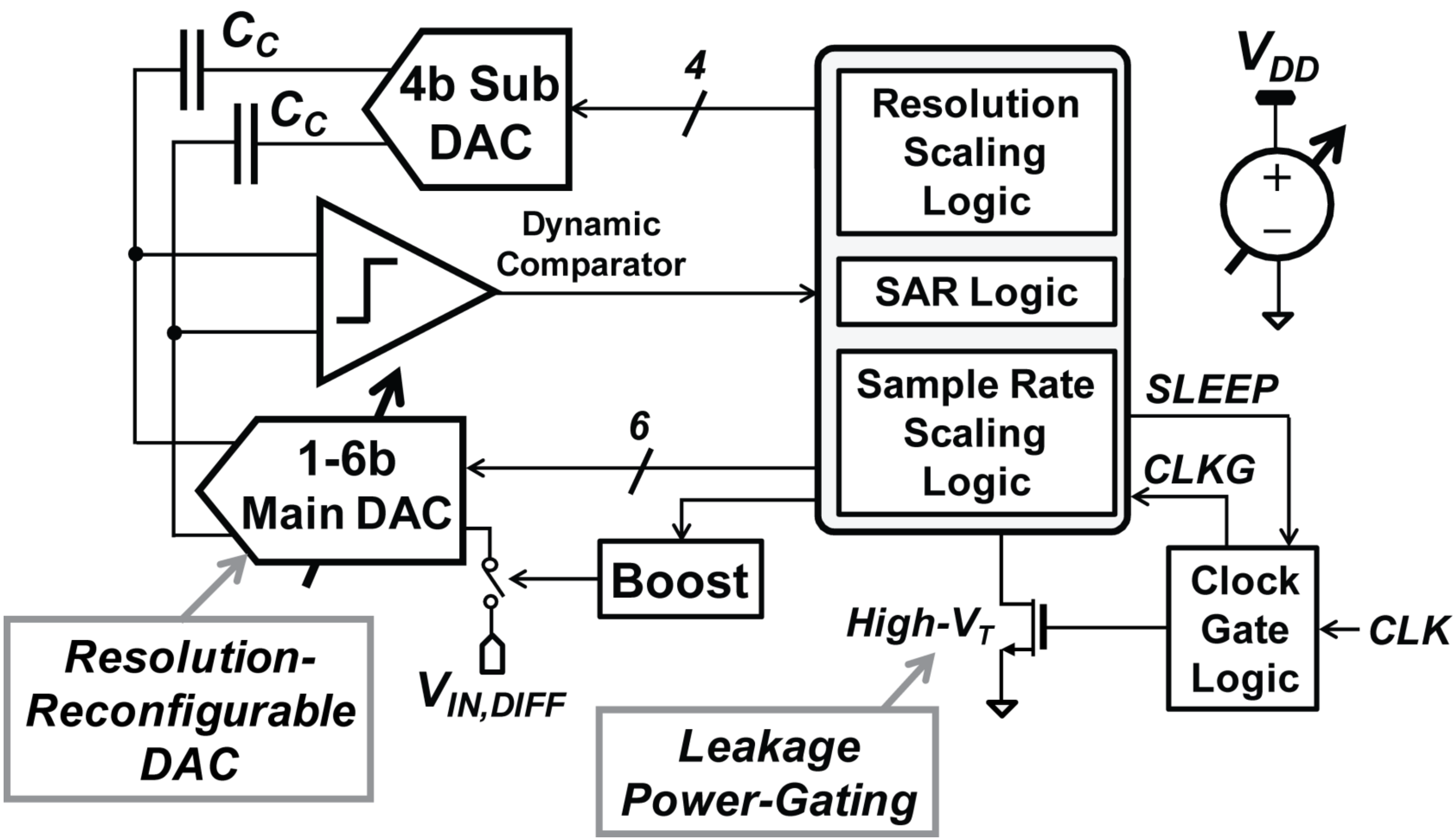
Bio-potential	Bandwidth
EEG (electroencephalography)	0.5 to 40 Hz
ECG (electrocardiography)	0.05 to 100 Hz
EMG (electromyography)	20 Hz to 2 kHz

Energy-efficient, scalable and reconfigurable ADC is beneficial

Power Scalable SAR ADC

ADC specifications:

Resolution	5b to 10b
Sample Rate	0 to 2MS/s



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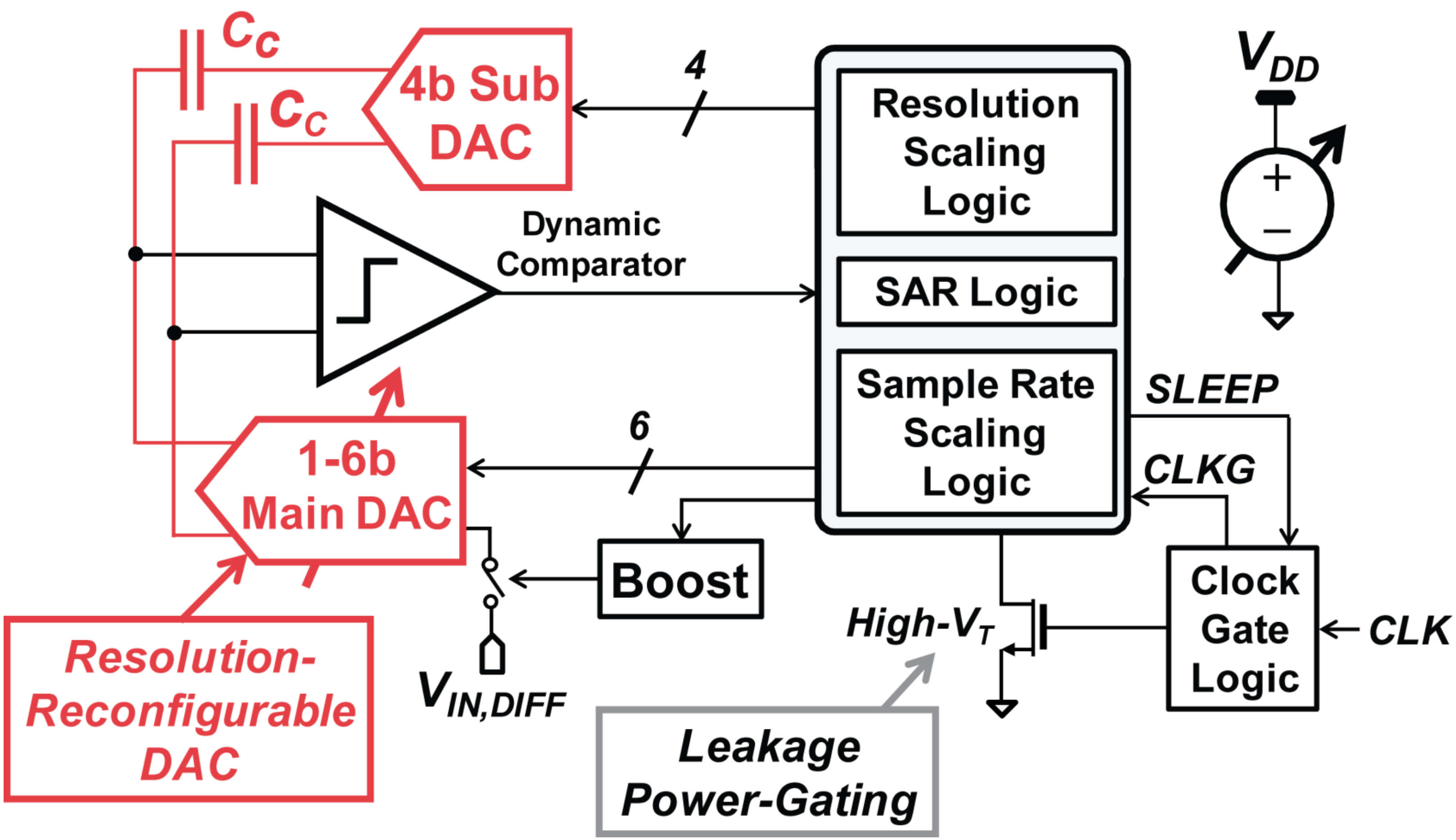

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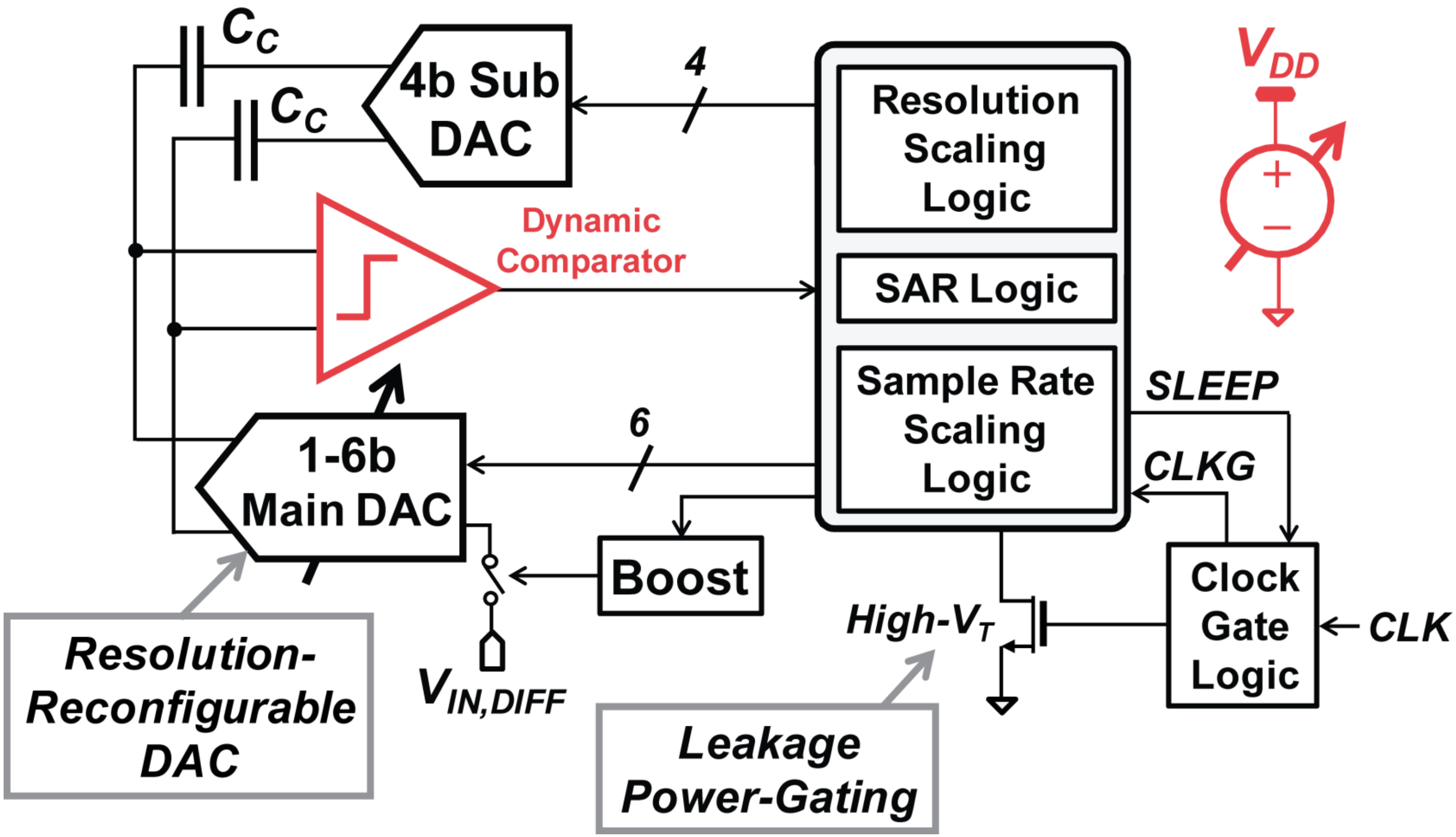

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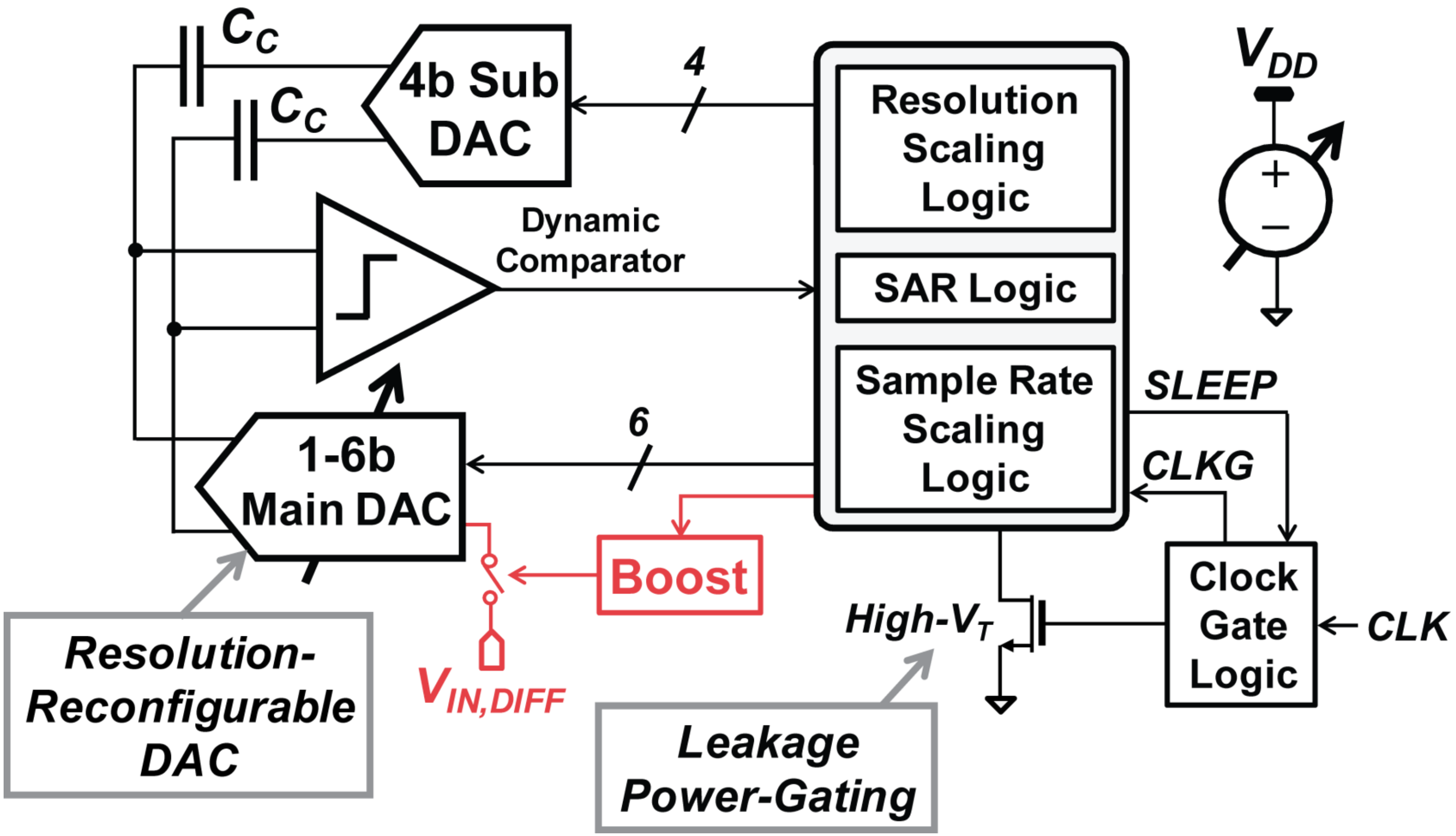

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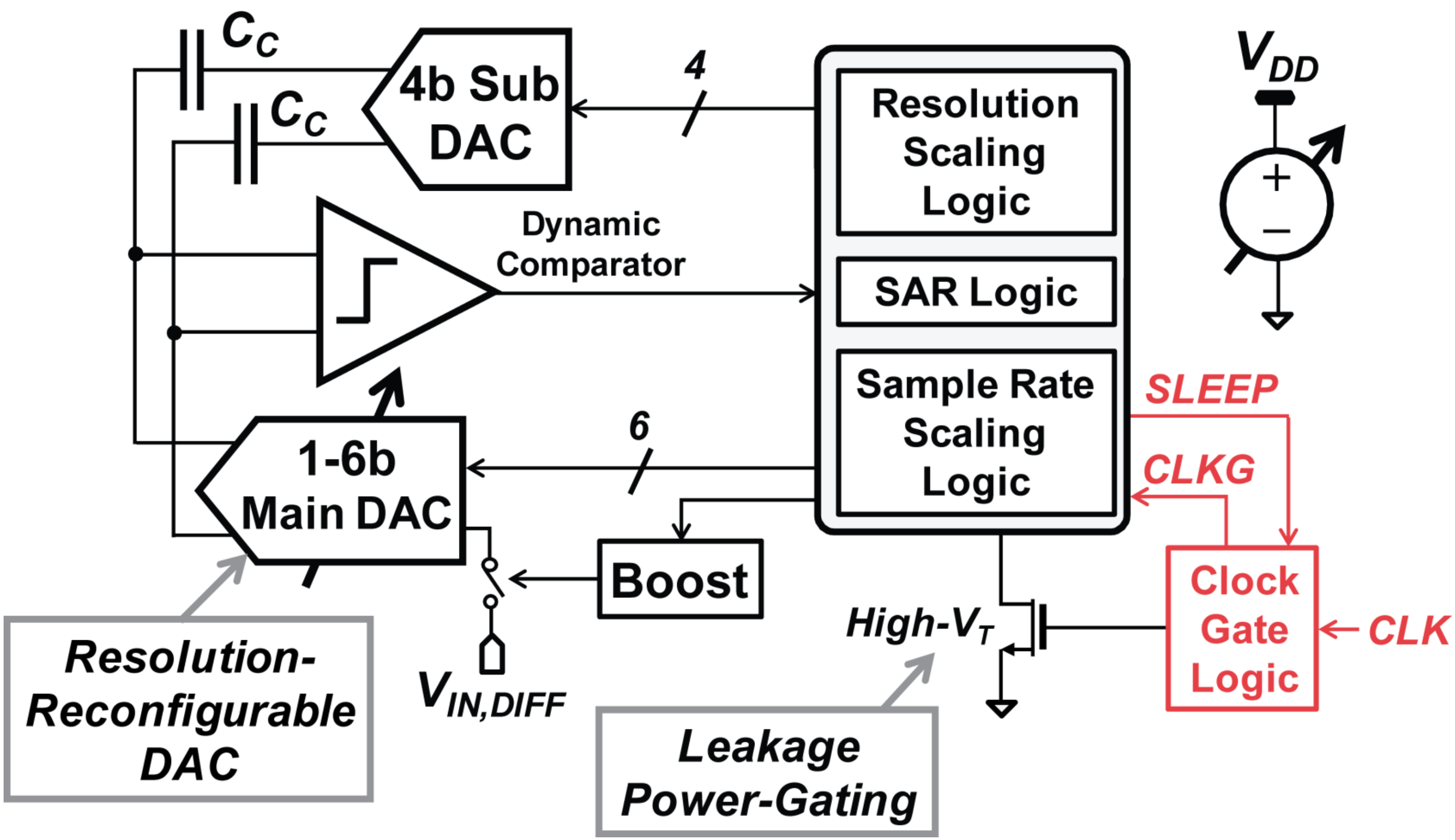

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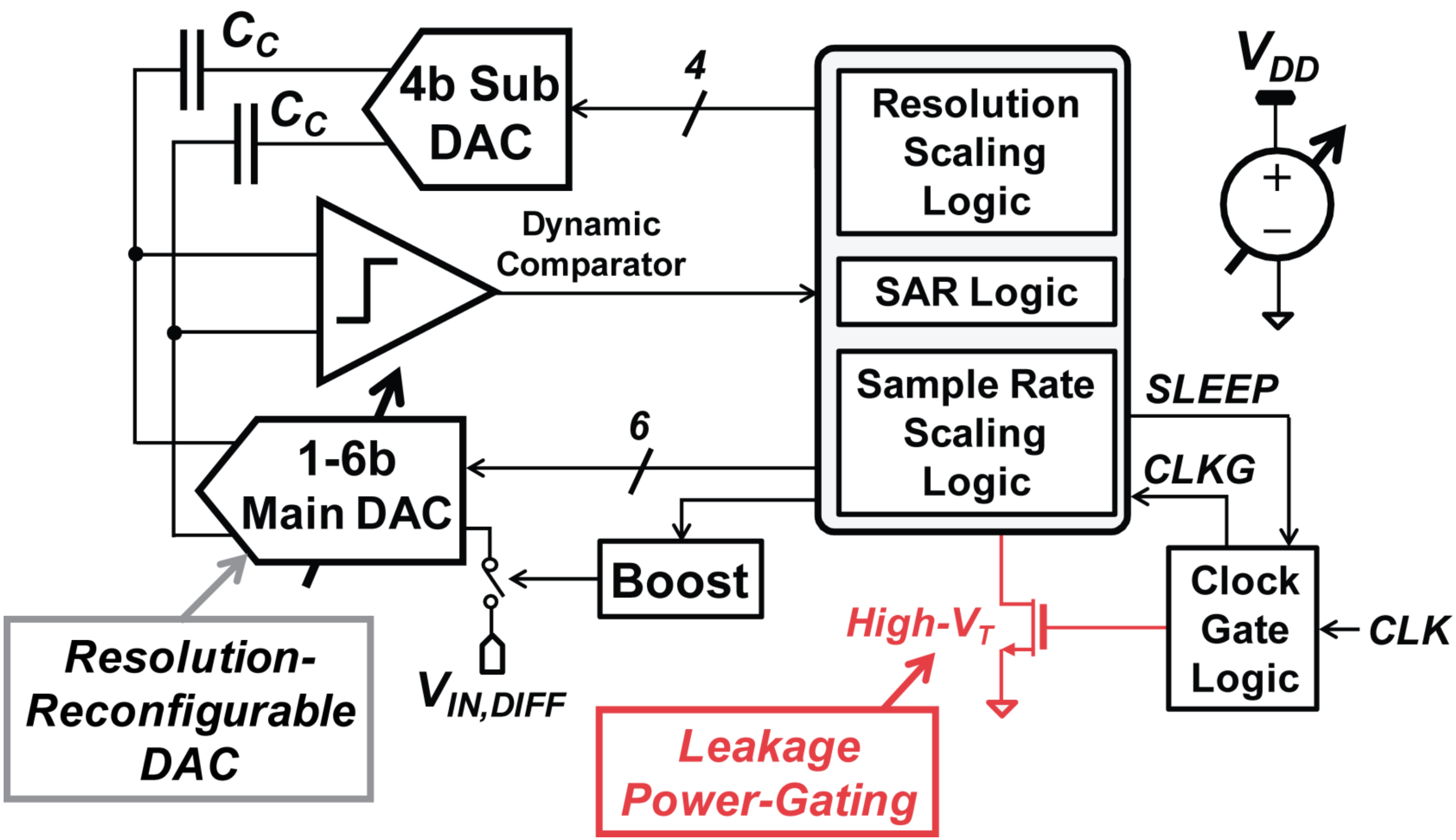
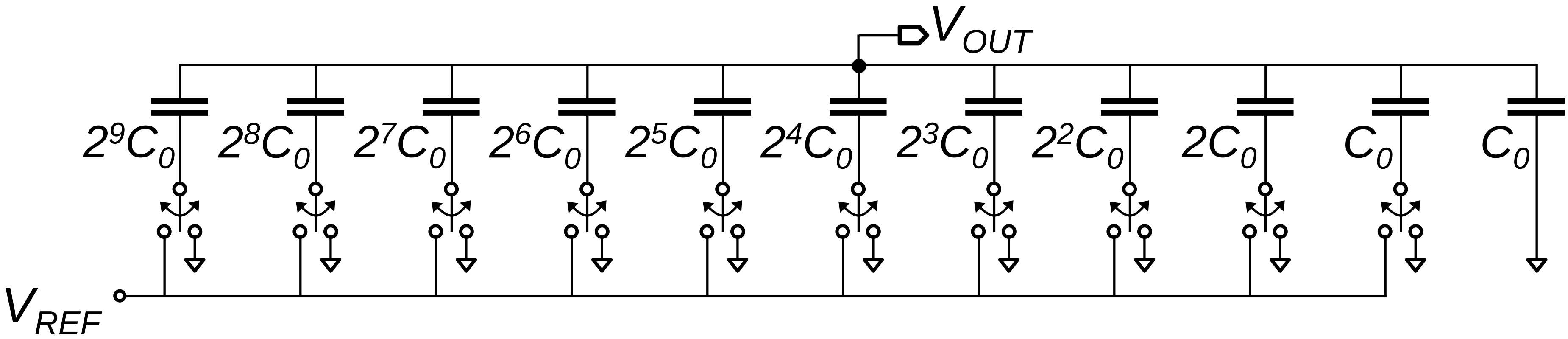


Outline

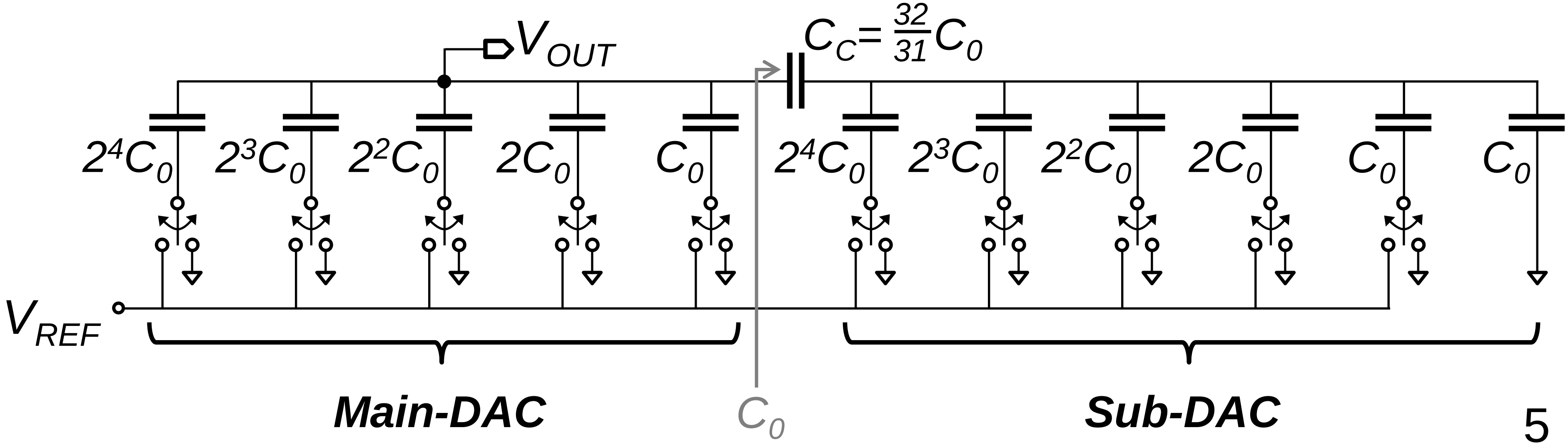
- Reconfigurable DAC Architecture
- Voltage Scaling
- Leakage Power-Gating
- Measured Results
- Conclusion

Review: Sub-DAC

Conventional Binary-Weighted Array → Large MSB to LSB ratio



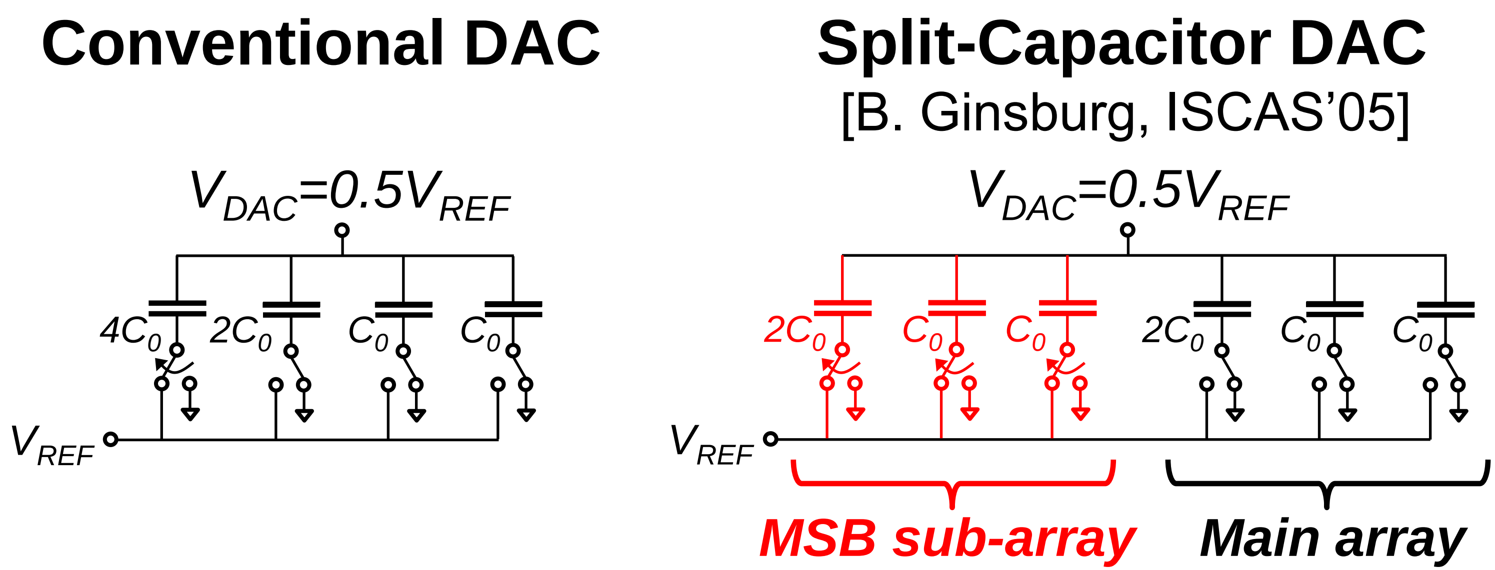
Main-DAC/Sub-DAC Array → Reduces ratio, saves area/power



Review: Split-Capacitor Array

Example: V_{REF} = 1V, V_{IN} = 0.4V

Bit Cycle 1 (Up)



$$E_{U,CONV,1} = E_{U,SPLIT,1} = 2C_0V_{REF}^2$$

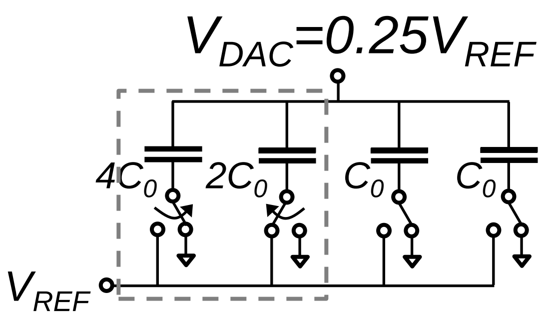
Up transitions require the same energy for both arrays

Review: Split-Capacitor Array

Example: $V_{REF} = 1V, V_{IN} = 0.4V$

Bit Cycle 2 (Down)

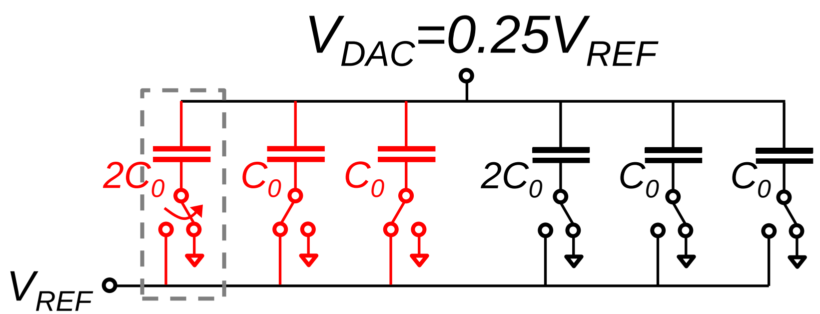
Conventional DAC



$$E_{D,CONV,2} = \frac{5}{2} C_0 V_{REF}^2$$

Split-Capacitor DAC

[B. Ginsburg, ISCAS'05]

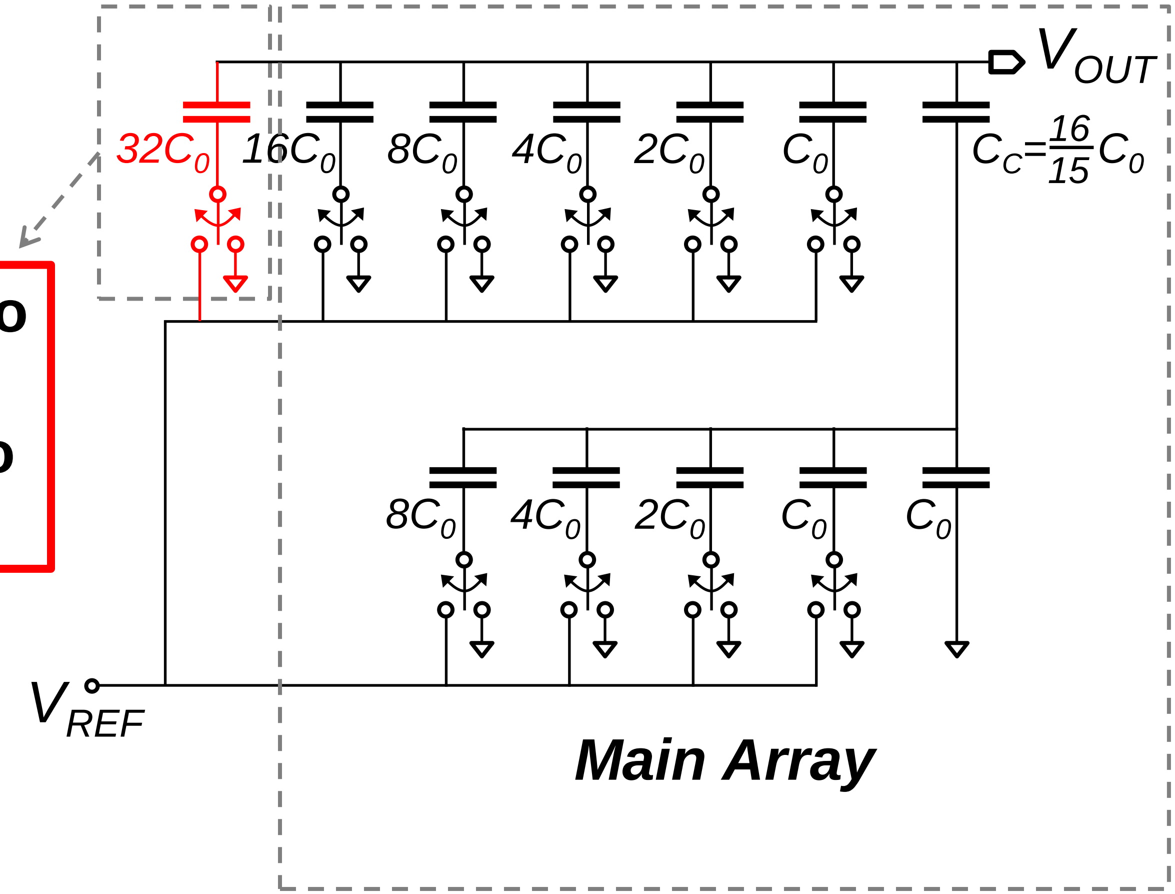


$$E_{D,SPLIT,2} = \frac{1}{2} C_0 V_{REF}^2$$

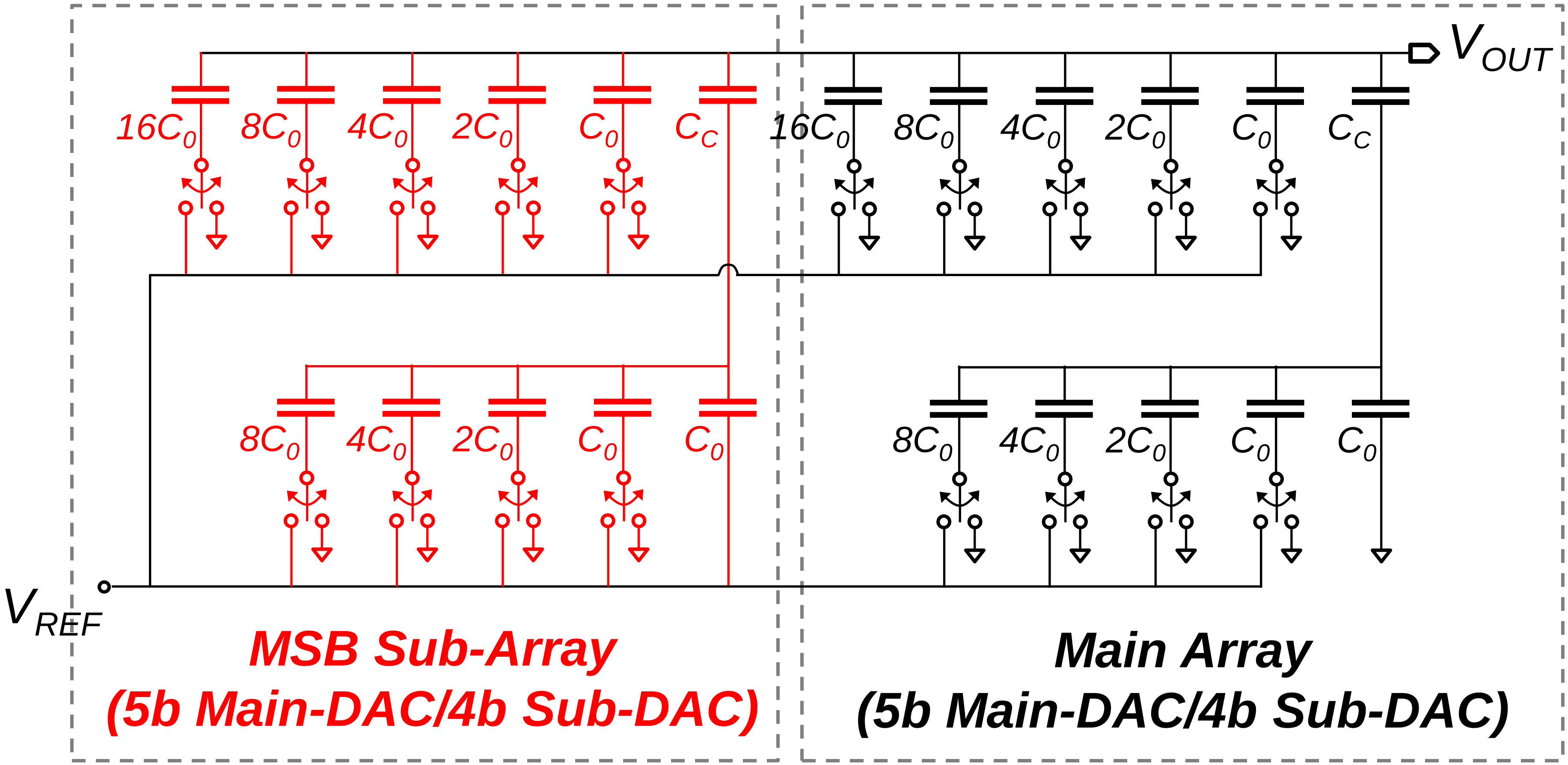
Split-Capacitor approach avoids charging capacitors to V_{REF} during down transitions

Split-Capacitor Array DAC with Sub-DAC

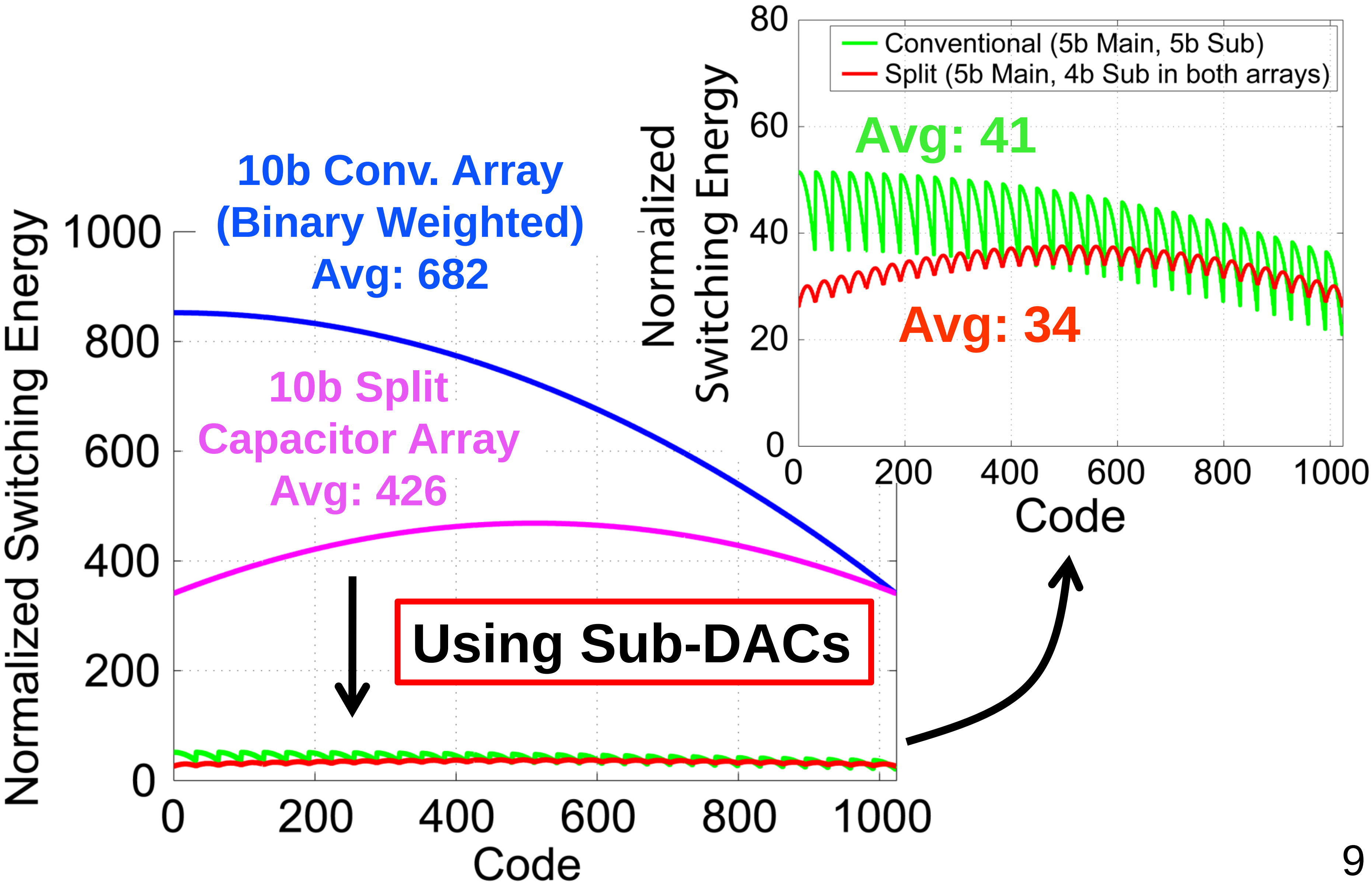
Split MSB capacitor into the MSB Sub-Array, identical in structure to the Main Array.



Split-Capacitor Array DAC with Sub-DAC

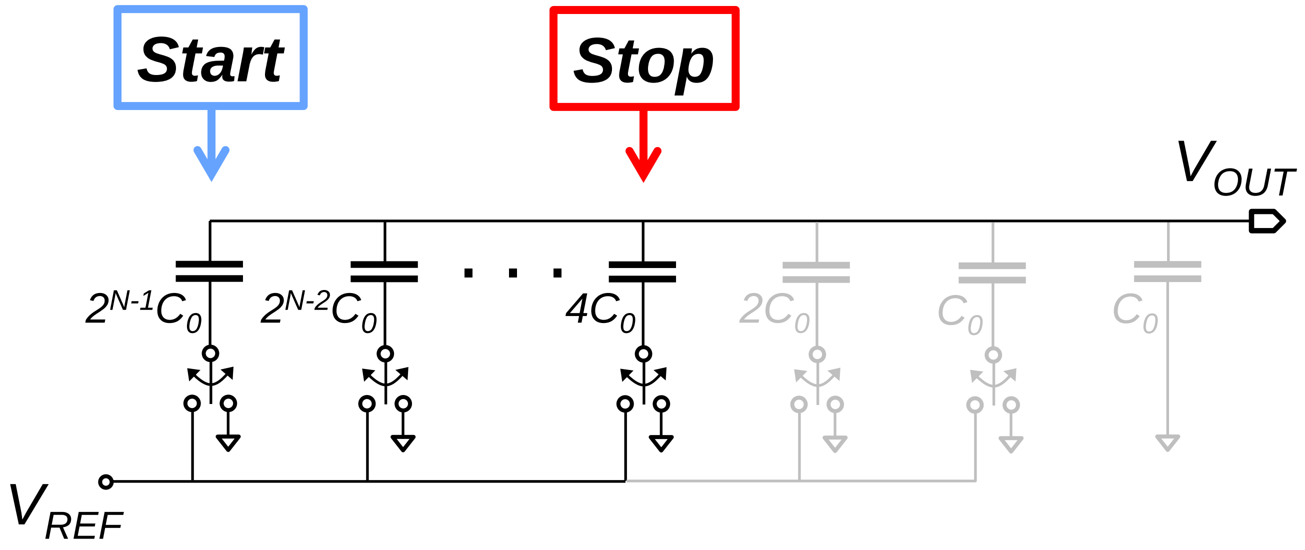


10b DAC Switching Energy



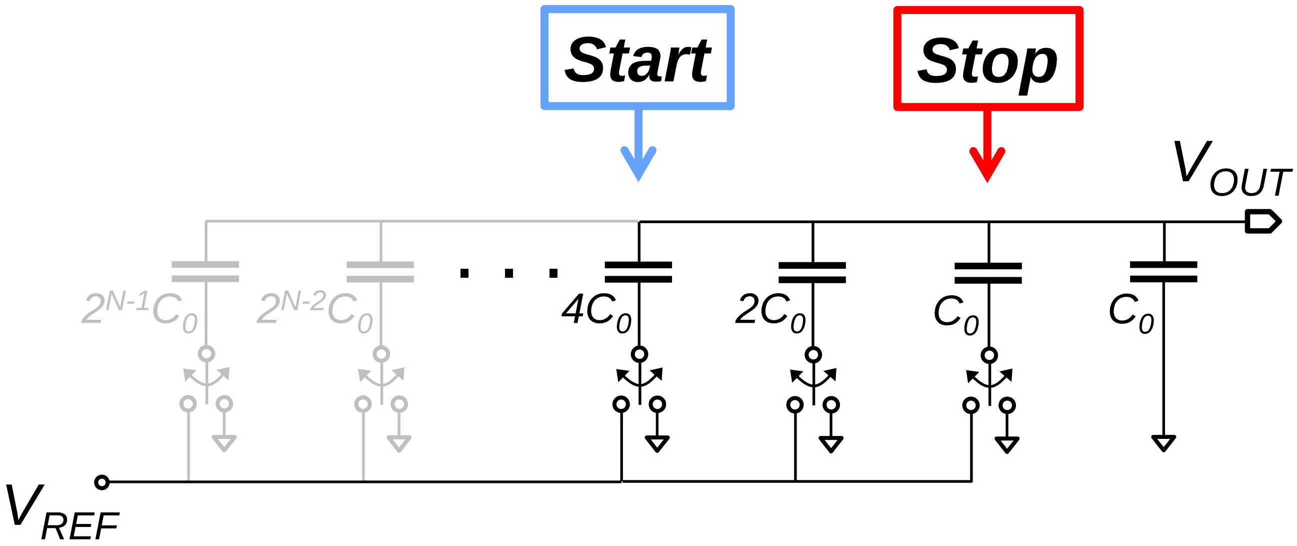
Adding Reconfigurability

- No power reduction by truncation of bits
- Resolution scaling:
  1. Start at MSB → power consumption



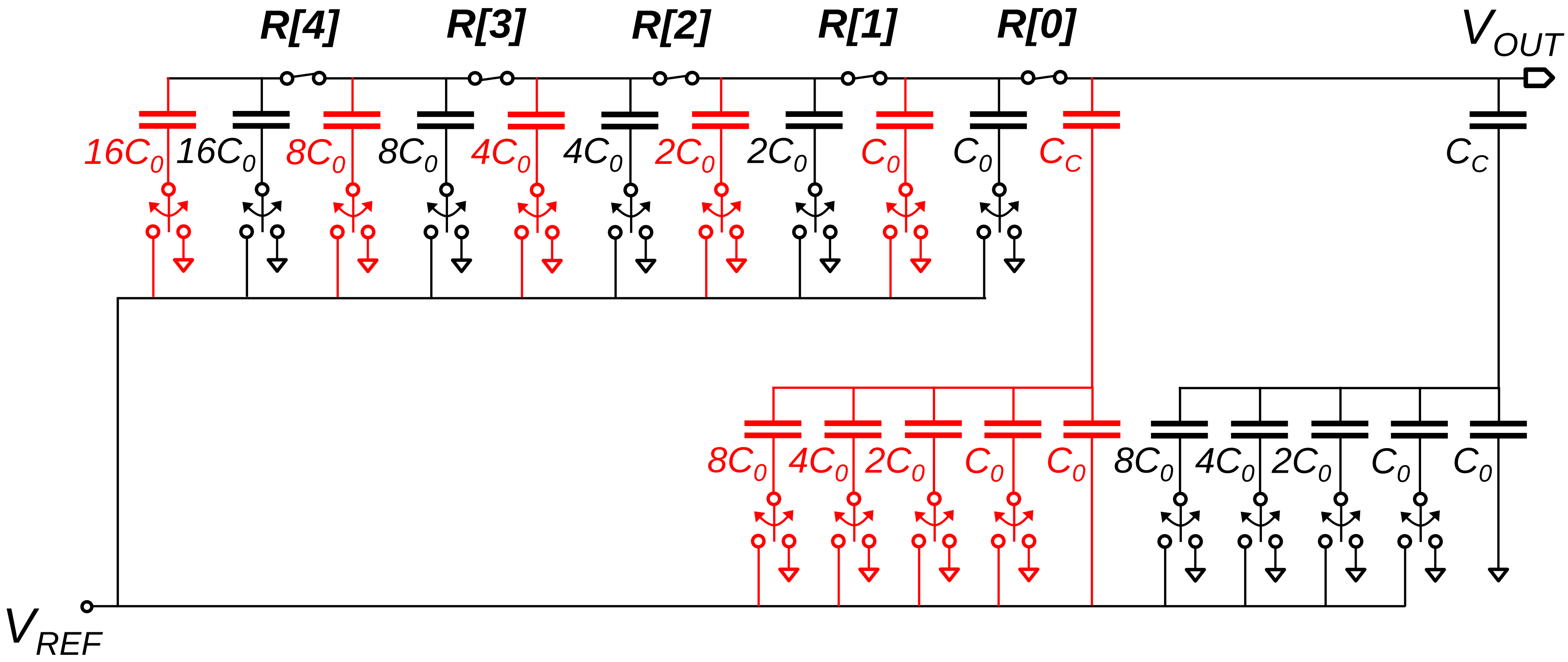
Adding Reconfigurability

- No power reduction by truncation of bits
- Resolution scaling:
  1. Start at MSB → power consumption
  2. Cycle through to LSB → attenuation of DAC output



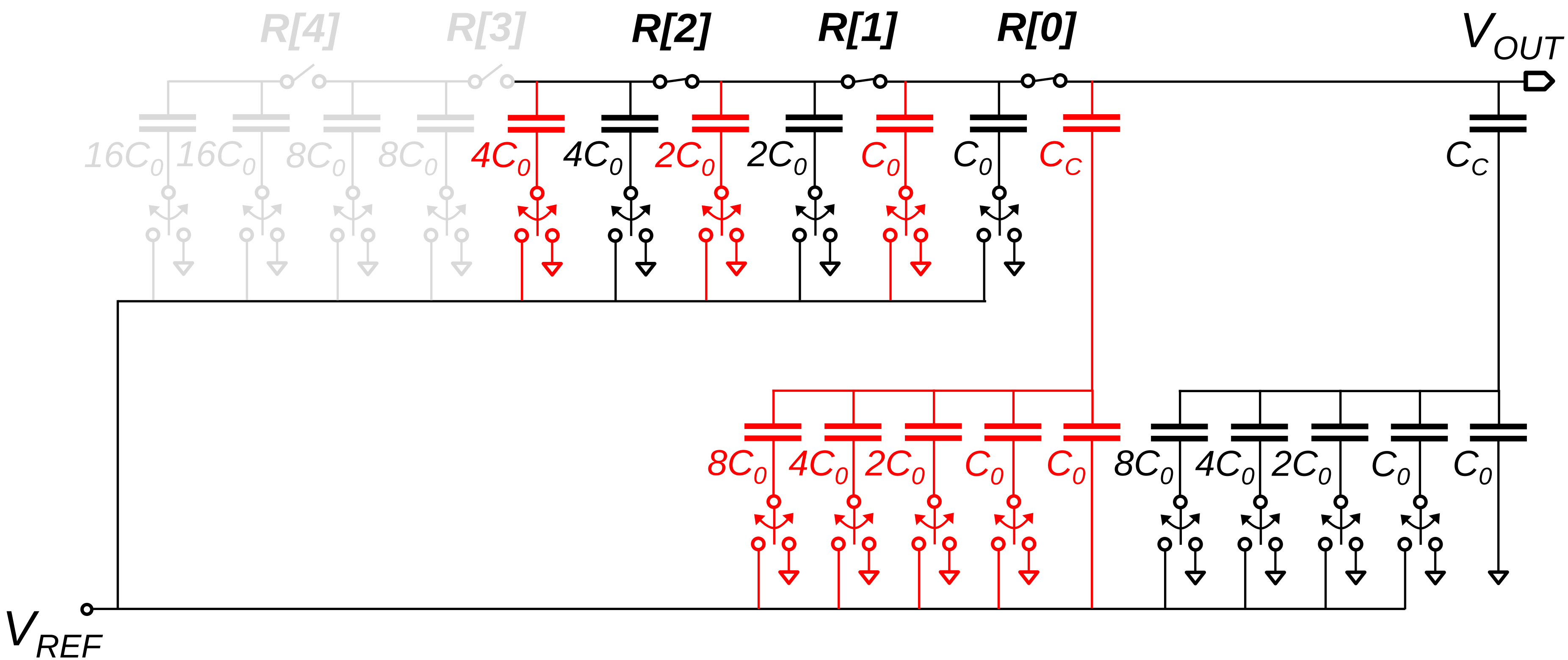
Reconfigurable DAC

- Interleave **MSB Sub-Array** with **Main Array**
- Insert switches to decouple capacitors as resolution is scaled

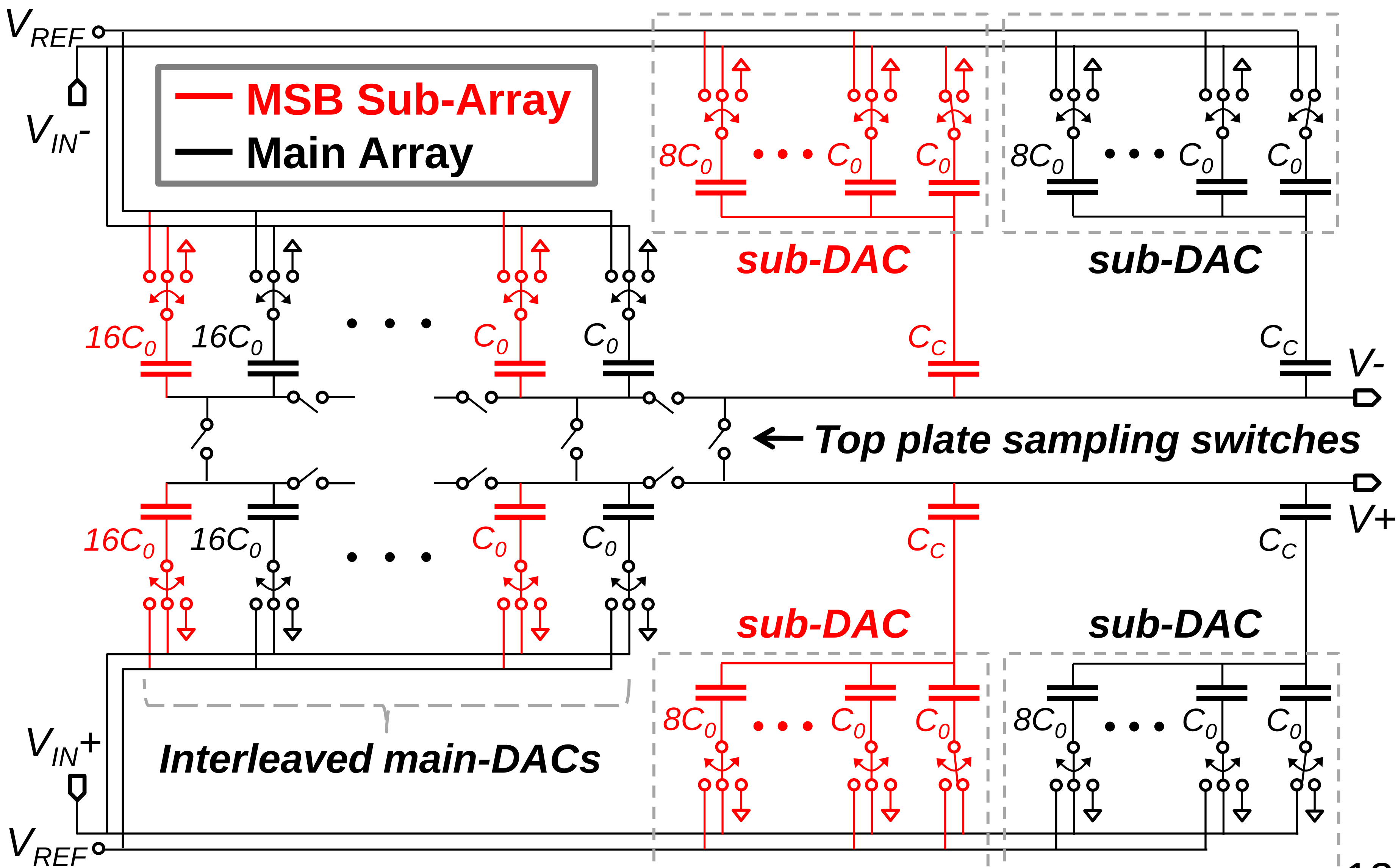


Reconfigurable DAC – 8b Mode

R[4:0]	00111
DAC Configuration	4b Main-DAC, 4b Sub-DAC
MSB Sub-Array	Split $8C_0$ (in red)



Differential DAC Schematic



Voltage Scaling

$$E_{ADC} \approx E_{DAC} + E_{COMP} + E_{DIG} + E_{LEAK}$$

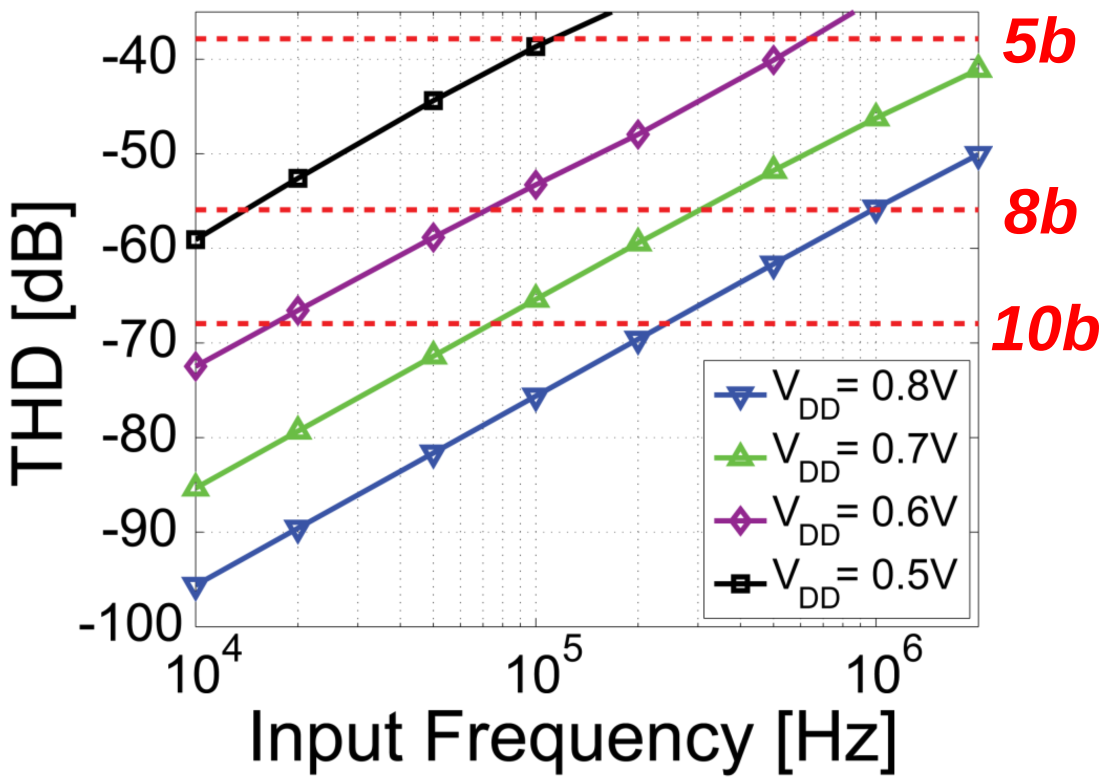
Block	Energy/Conversion	Voltage Dependence
DAC*	$C_{DAC}(2^N, V_{IN}) \cdot V_{DD}^2$	V_{DD}^2
Comparator	$N \cdot C_L \cdot V_{DD}^2$	V_{DD}^2
Digital	$C_{EFF}(N, V_{IN}) \cdot V_{DD}^2$	V_{DD}^2
Leakage**	$V_{DD} \cdot I_{LEAK} \cdot T_s$	$V_{DD} \cdot e^{kV_{DD}}$

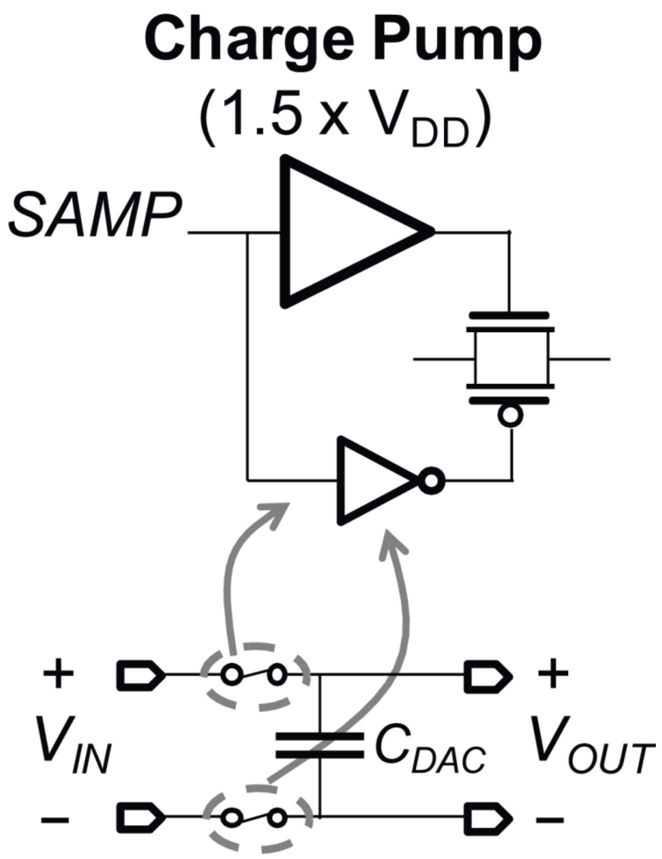
* $V_{REF} = V_{DD}$

** I_{LEAK} is exponential with V_{DD} due to DIBL

ADC Energy-Per-Conversion benefits from voltage scaling

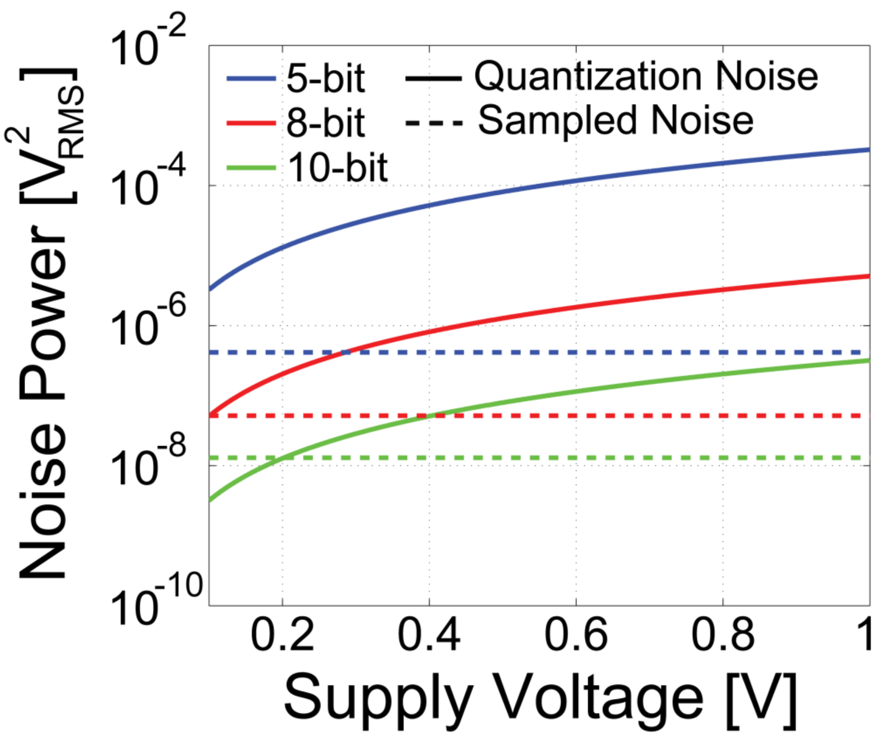
Voltage Scaling and Linearity

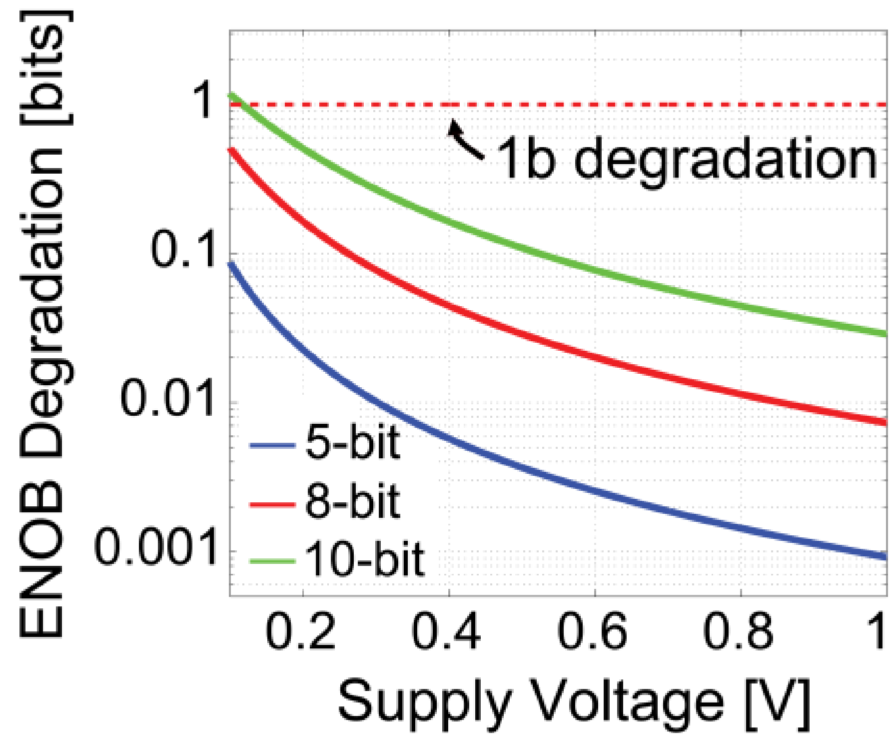




- Linearity requirements decrease with resolution

Voltage Scaling and Noise

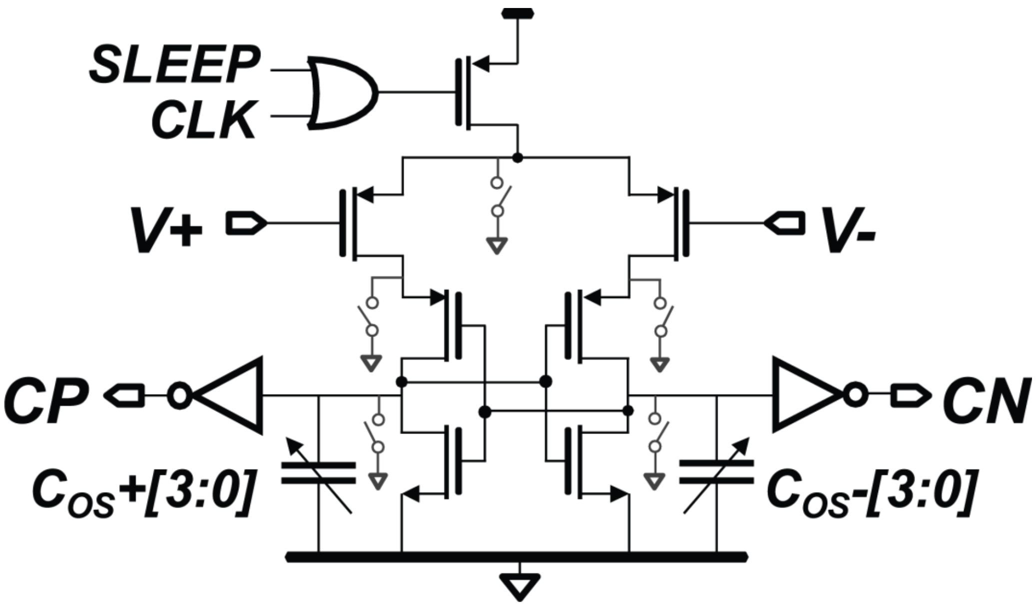


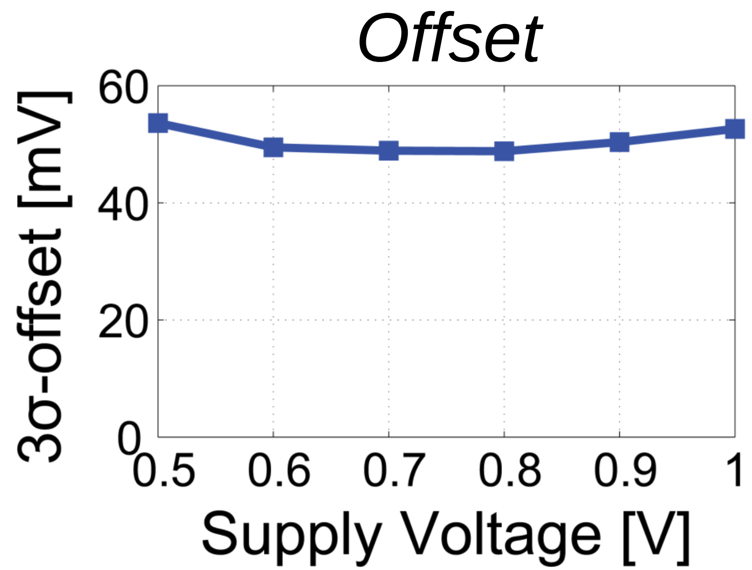


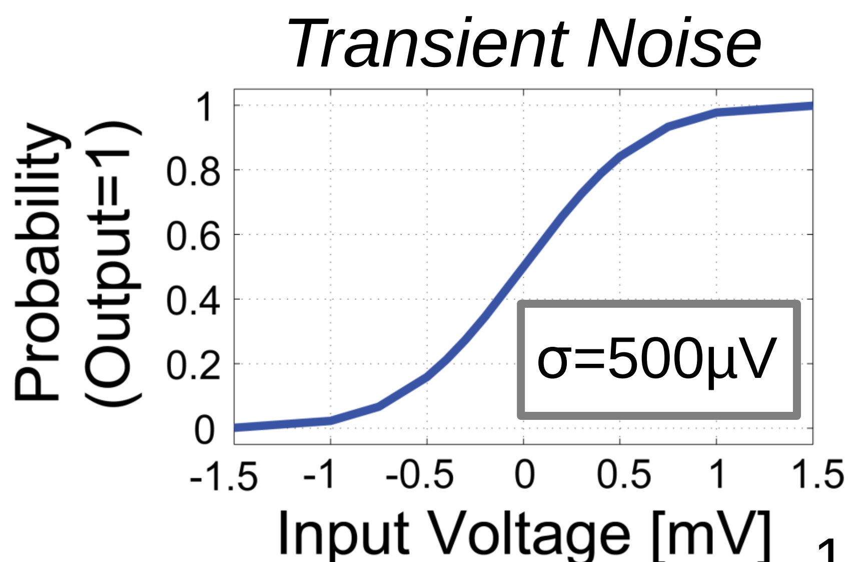
- Noise requirements decrease with resolution

Leverage voltage scaling with resolution for CV^2 savings

Regenerative Comparator





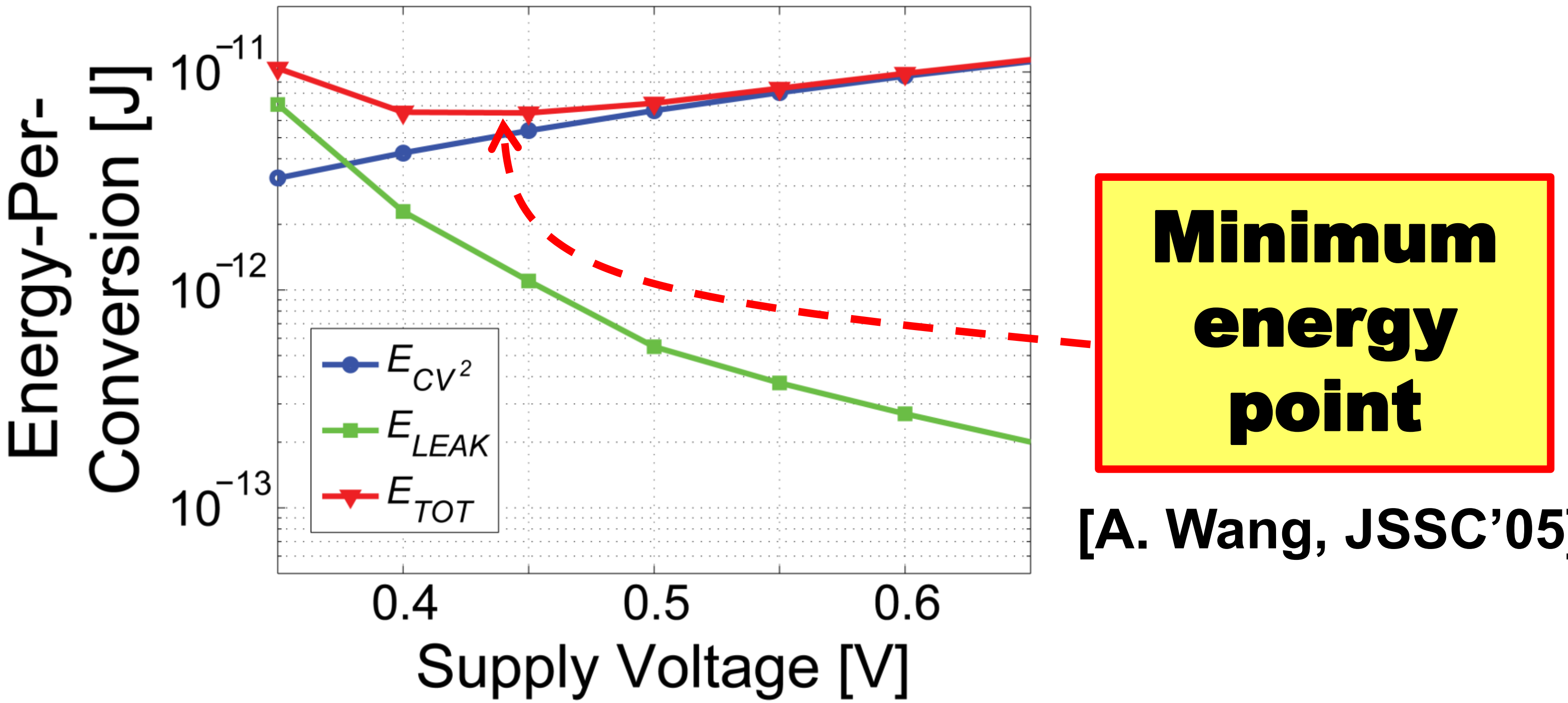


- 4-bit switched capacitors for 3-σ offset compensation
- Noise degrades ENOB by 1b at 0.5V in 10b mode

Minimum Energy Point

$$E/conversion \sim C_{EFF}V_{DD}^2 + V_{DD}I_{LEAK}T_S$$

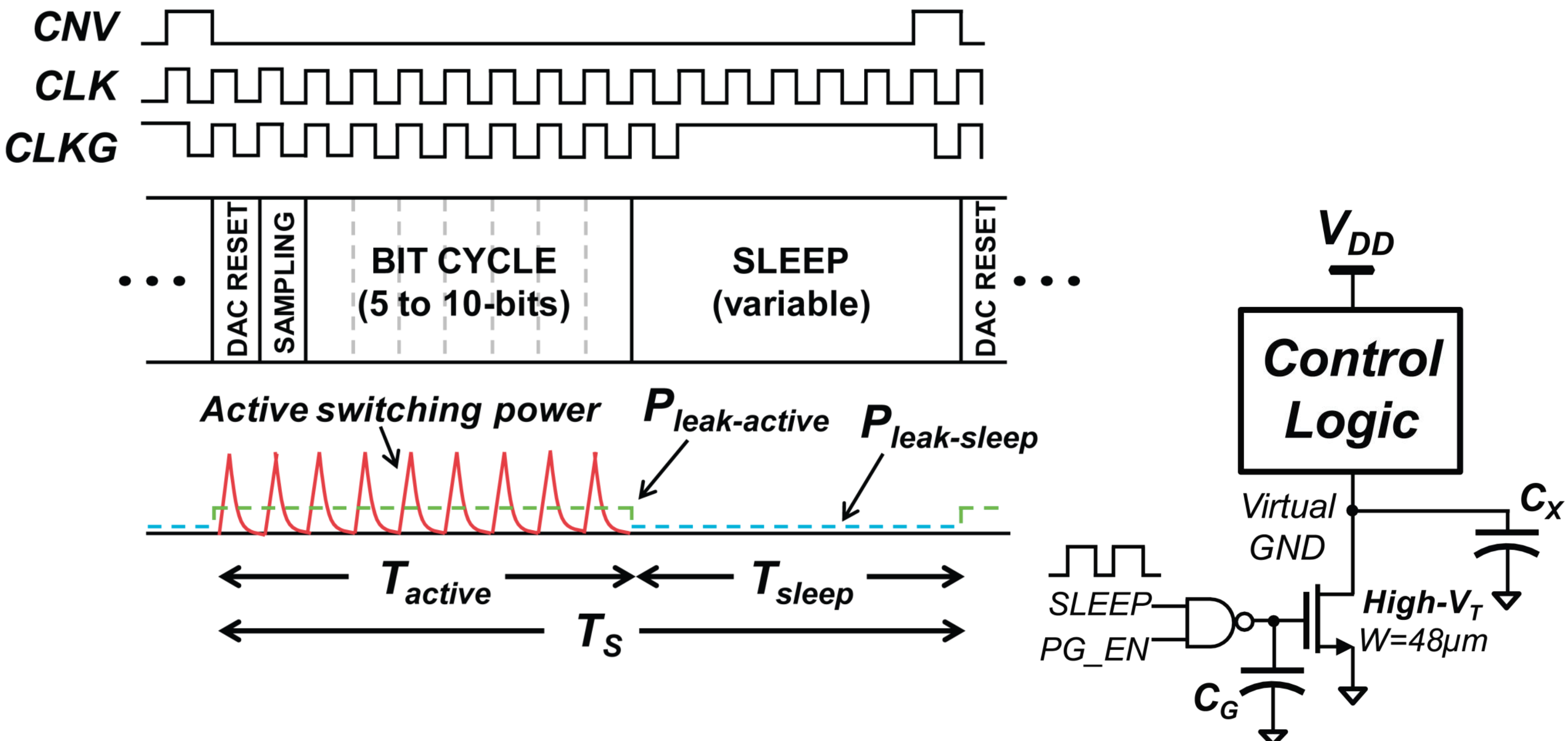
- Minimum conversion time (T_S) can be limited by:
  - Sampling bandwidth, reference settling, comparator



[A. Wang, JSSC'05]

Leakage Reduction

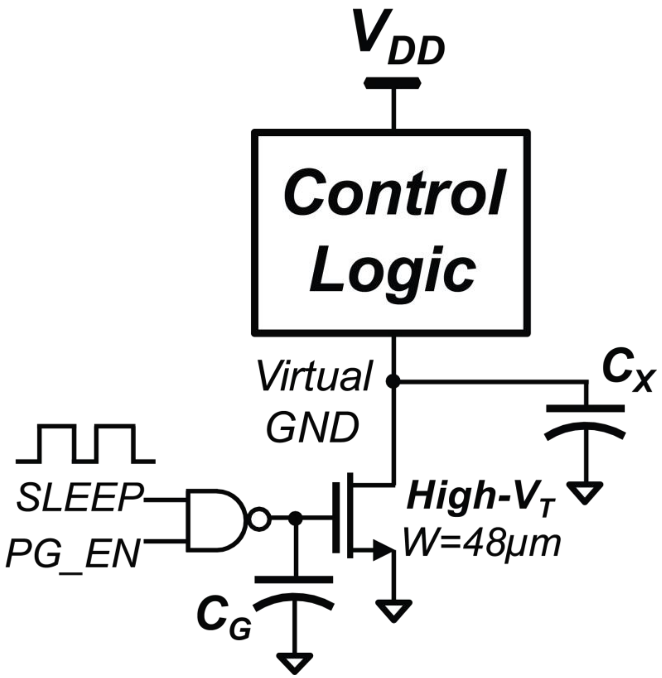
- *SLEEP* mode enables sample rate scaling
- Leakage power-gating applied during *SLEEP*

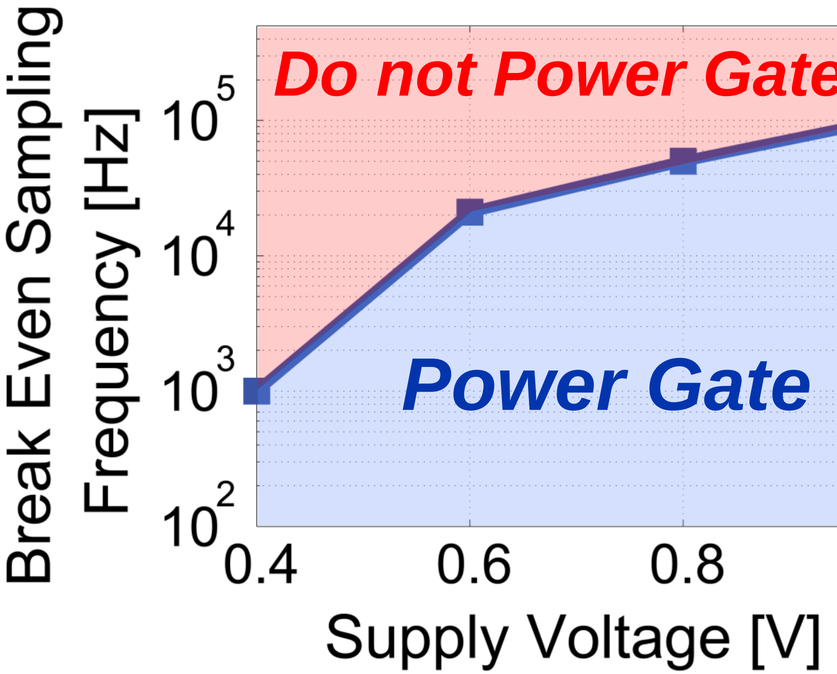


Power Gating Break-Even Point

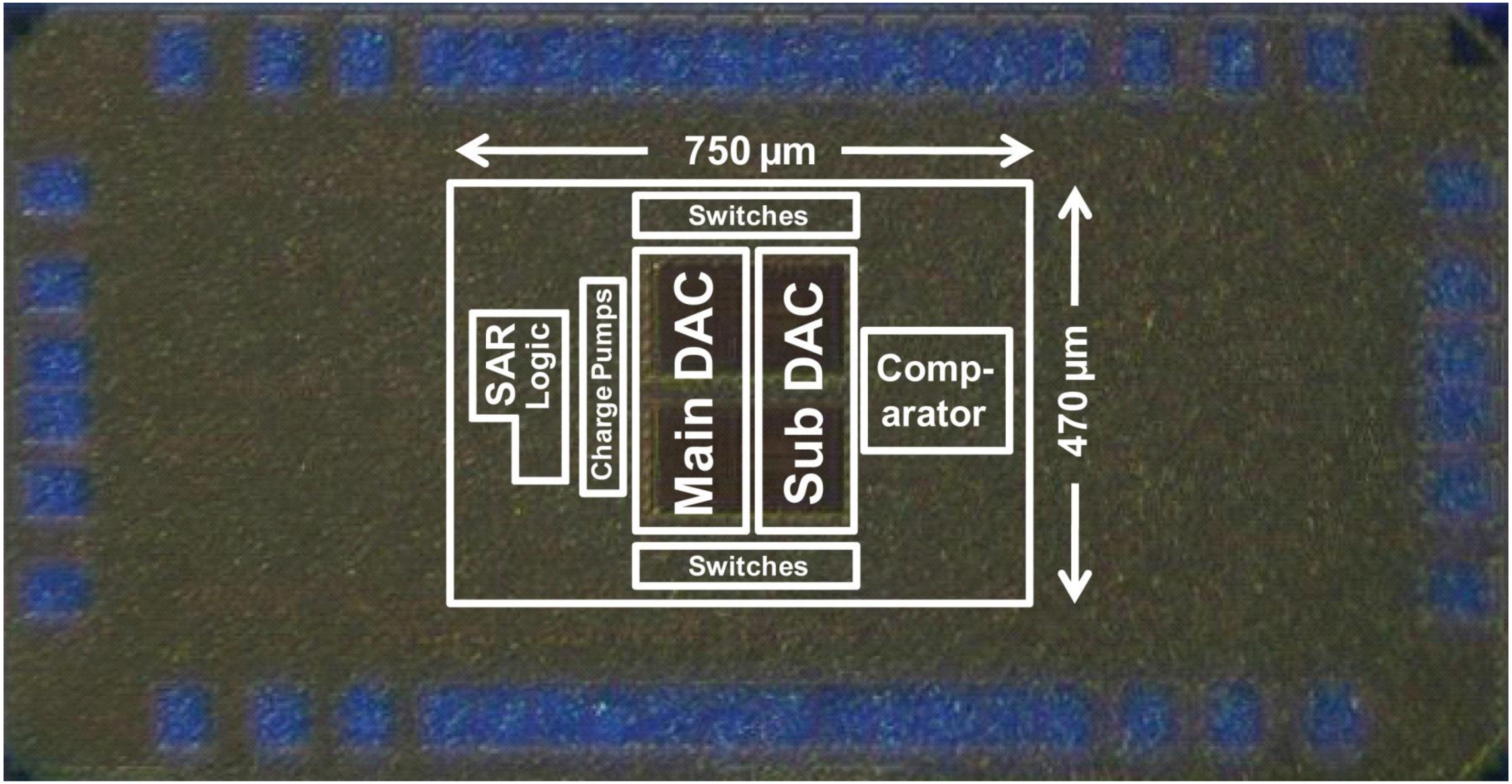
- Energy overhead:
  - Switching gate capacitance: $E_{SW}=C_G V_{DD}^2$
  - Recovery of virtual ground: $E_{REC}=C_X V_{DD} \Delta V$

Require: $E_{REC} + E_{SW} < (P_{leak\text{-}active} - P_{leak\text{-}sleep})T_{sleep}$



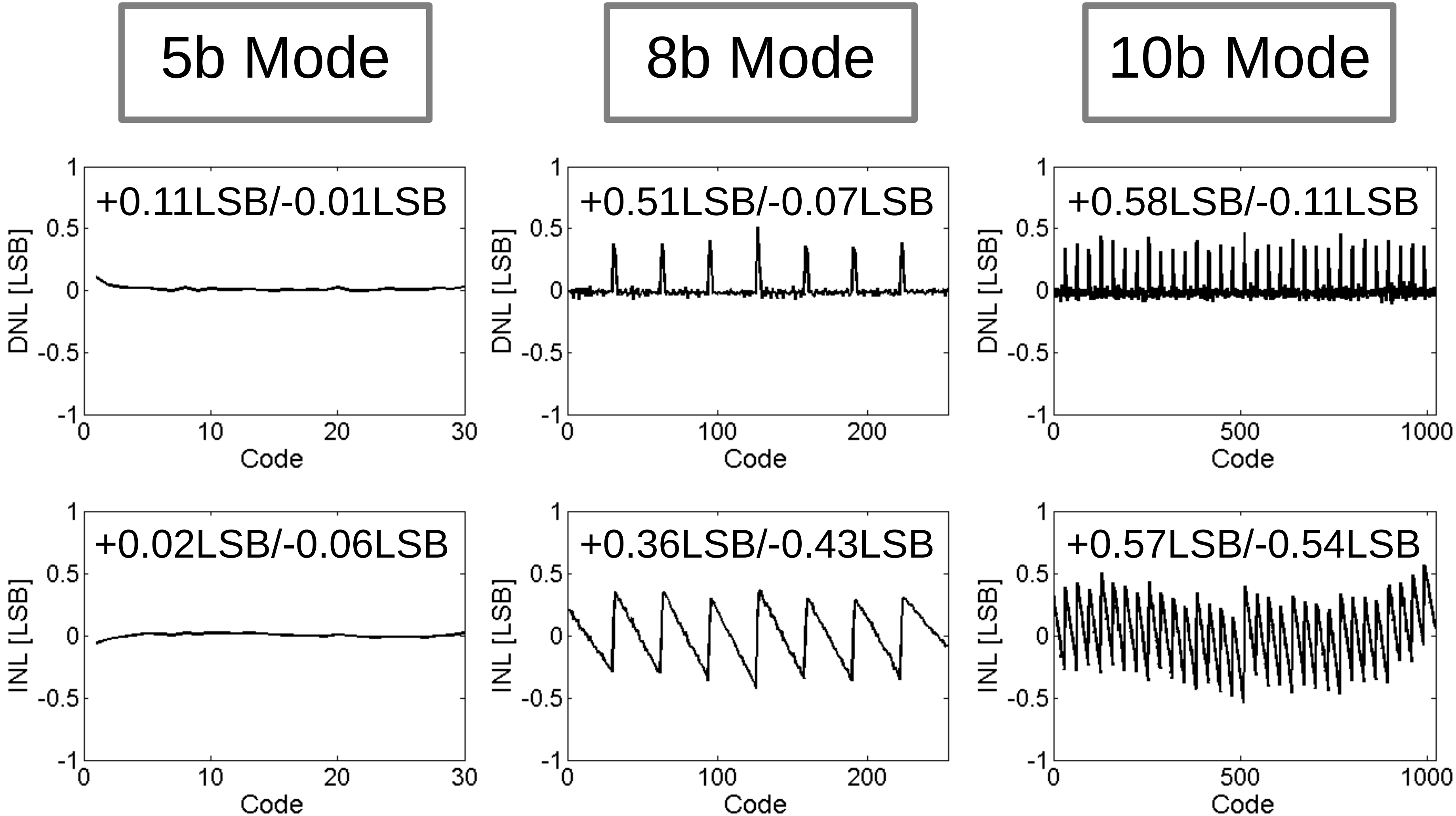


ADC Prototype



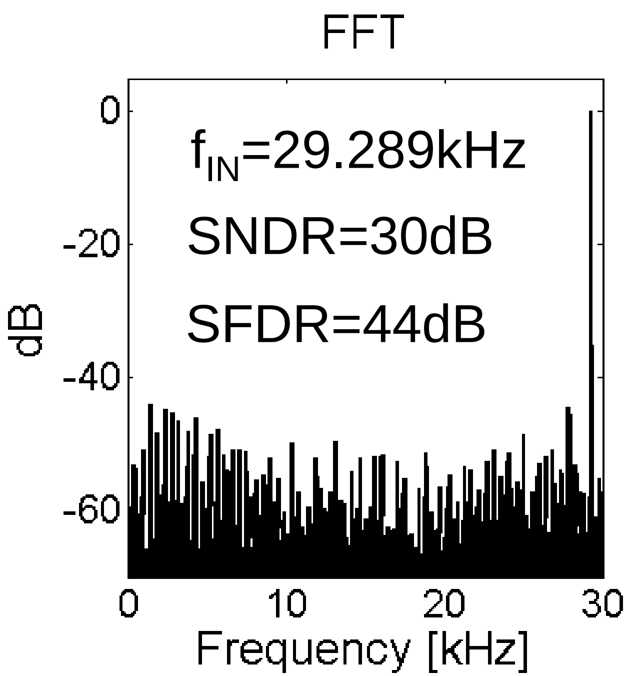
65nm Low-Leakage Digital CMOS

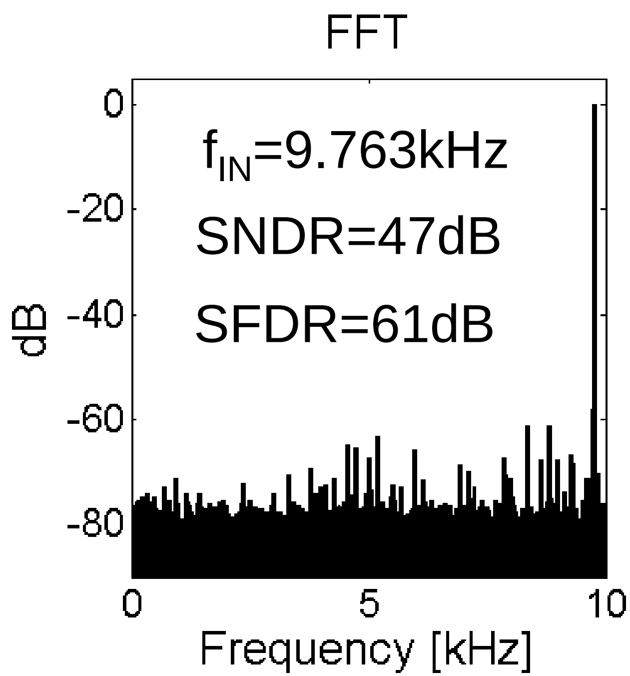
Measured INL and DNL (V_{DD}=0.6V, f_S=100kS/s)

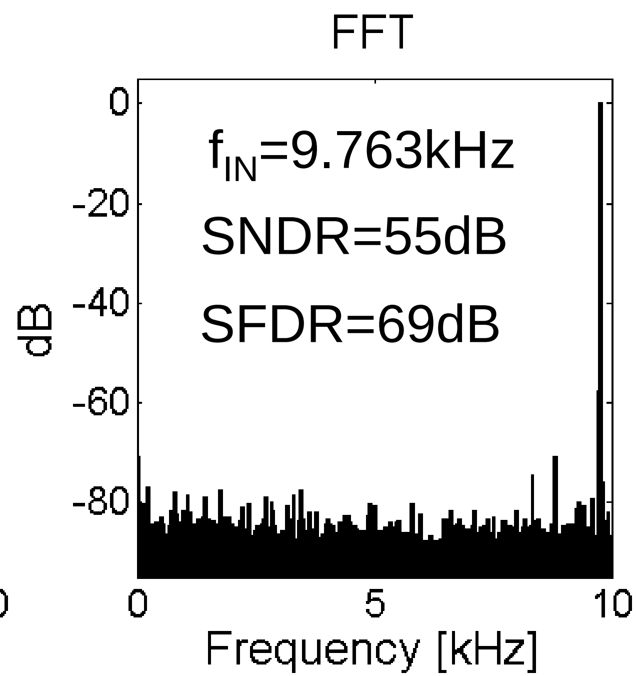


Measured FFT

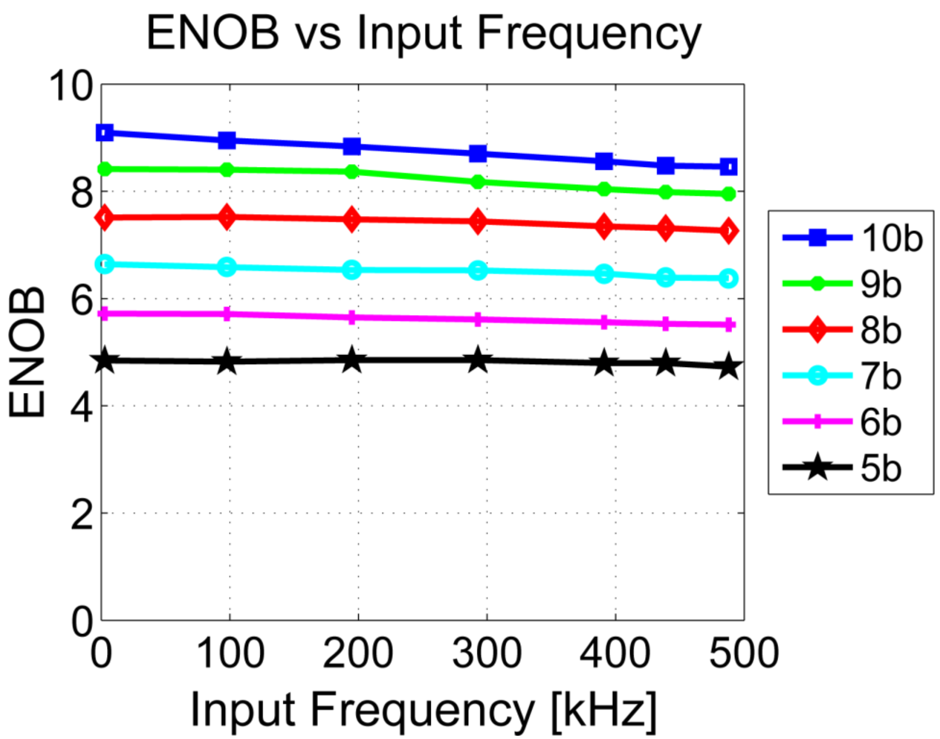
5b Mode	**8b Mode**	**10b Mode**
V_{DD}=0.5V	V_{DD}=0.55V	V_{DD}=0.55V
f_S=60kS/s	f_S=20kS/s	f_S=20kS/s

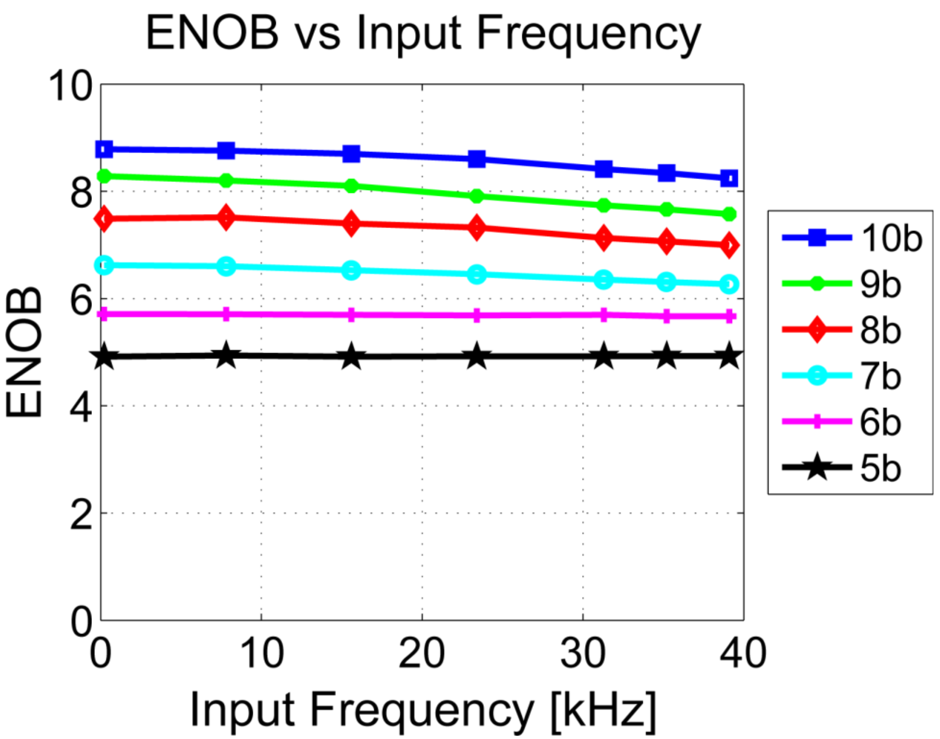






Measured ENOB

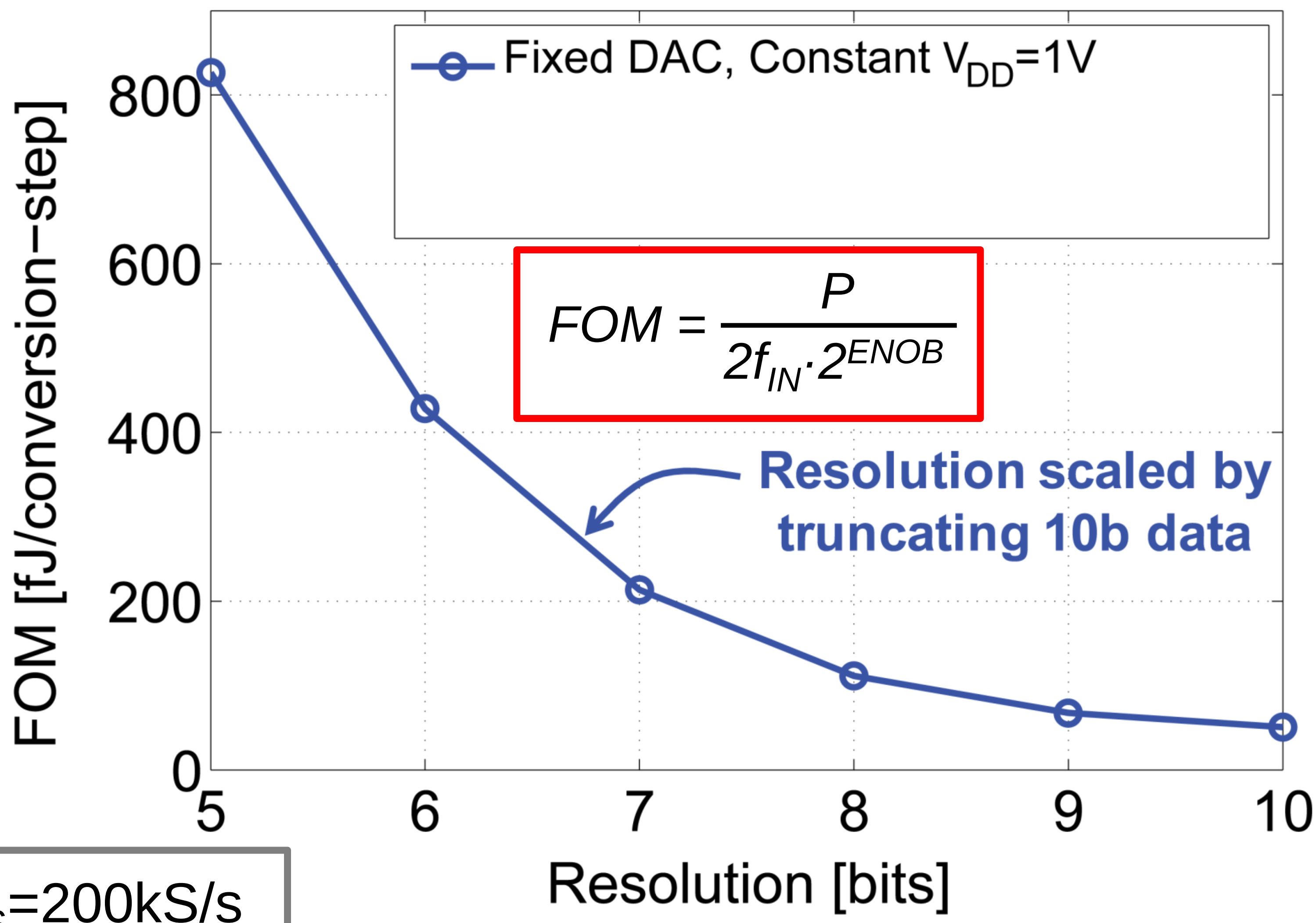




f_S=1MS/s
V_{DD}=1V

f_S=80kS/s
V_{DD}=0.55V

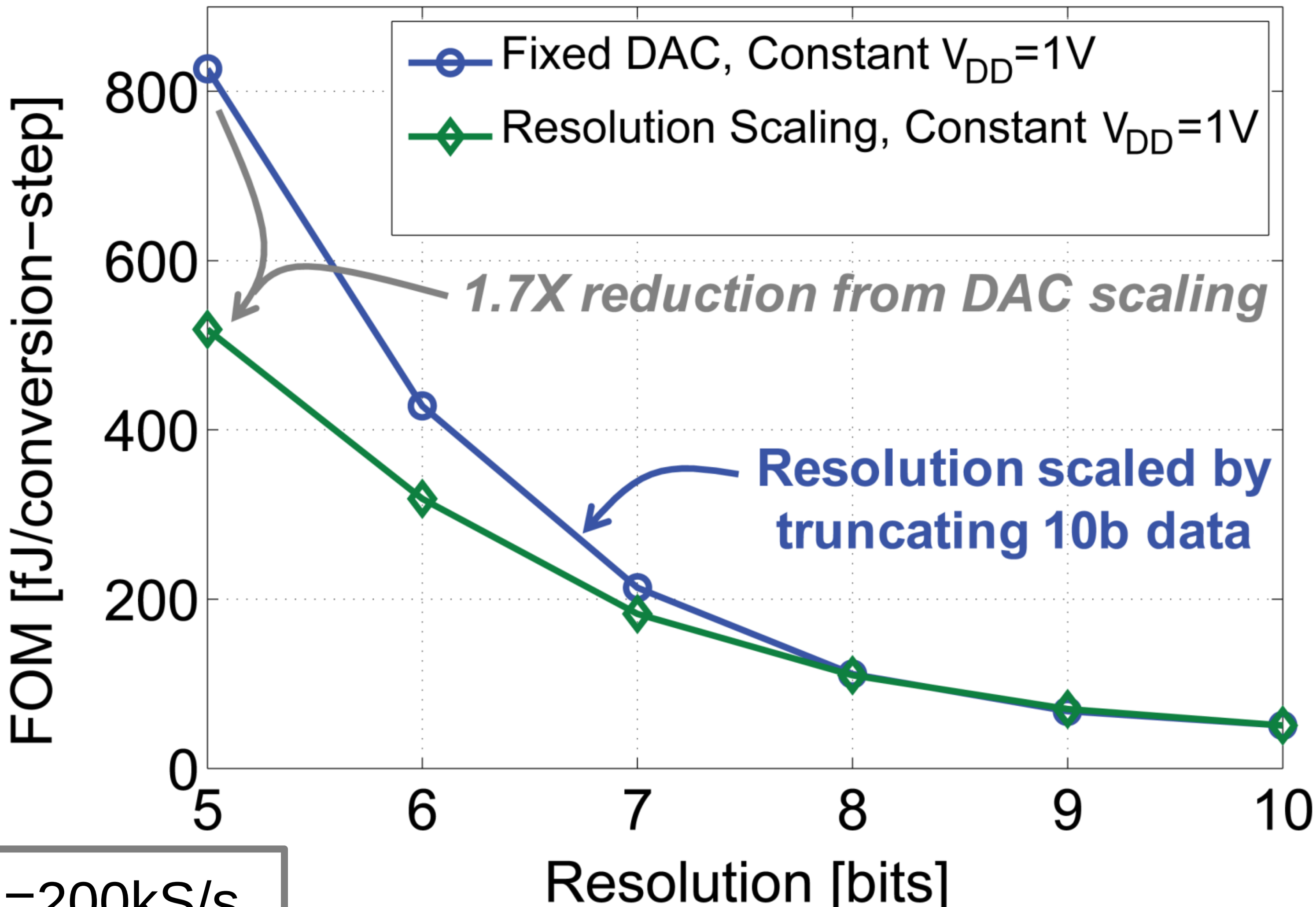
Measured Resolution and Voltage Scaling Results



$$FOM = \frac{P}{2f_{IN} \cdot 2^{ENOB}}$$

f_S=200kS/s

Measured Resolution and Voltage Scaling Results



f_S=200kS/s

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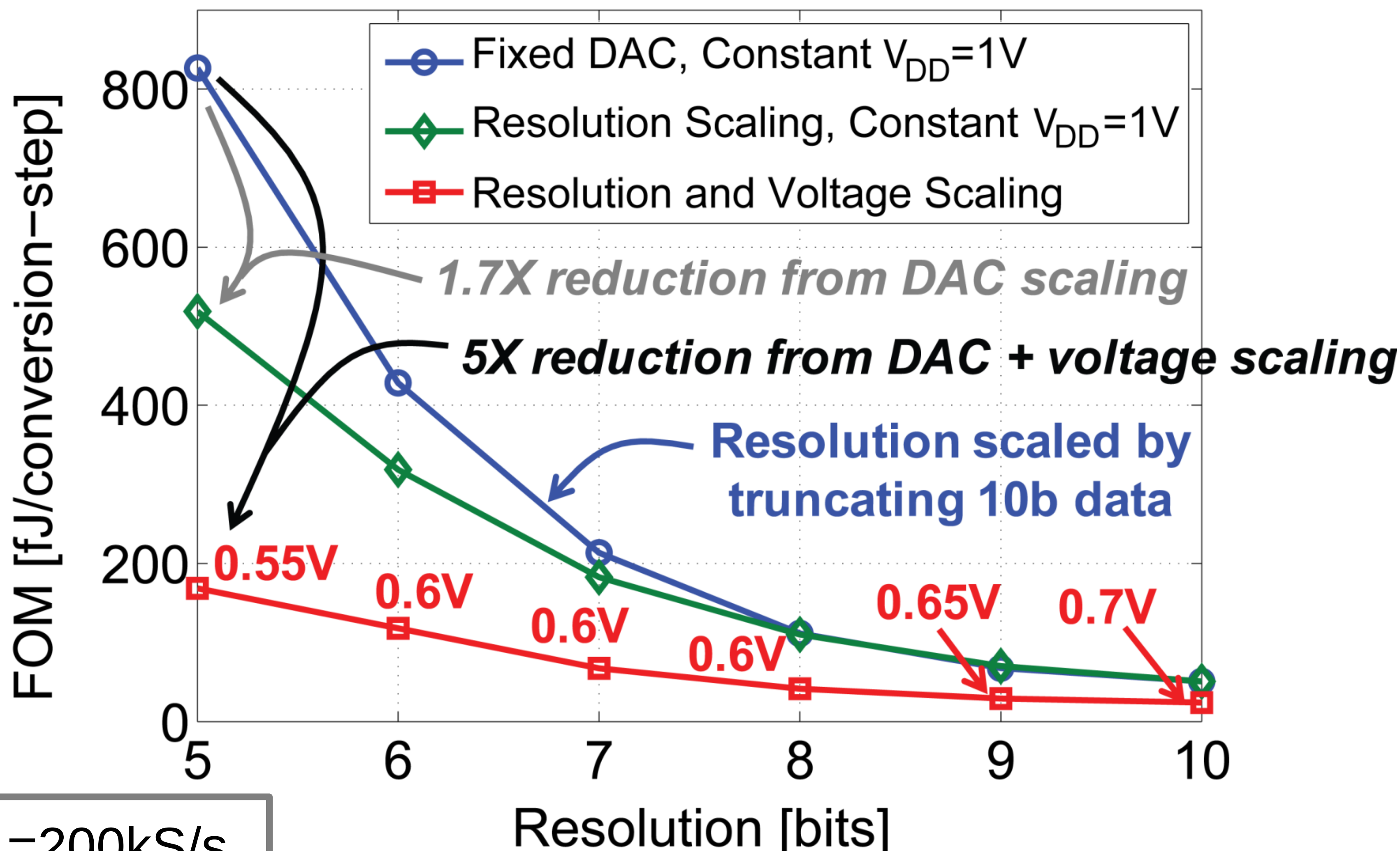
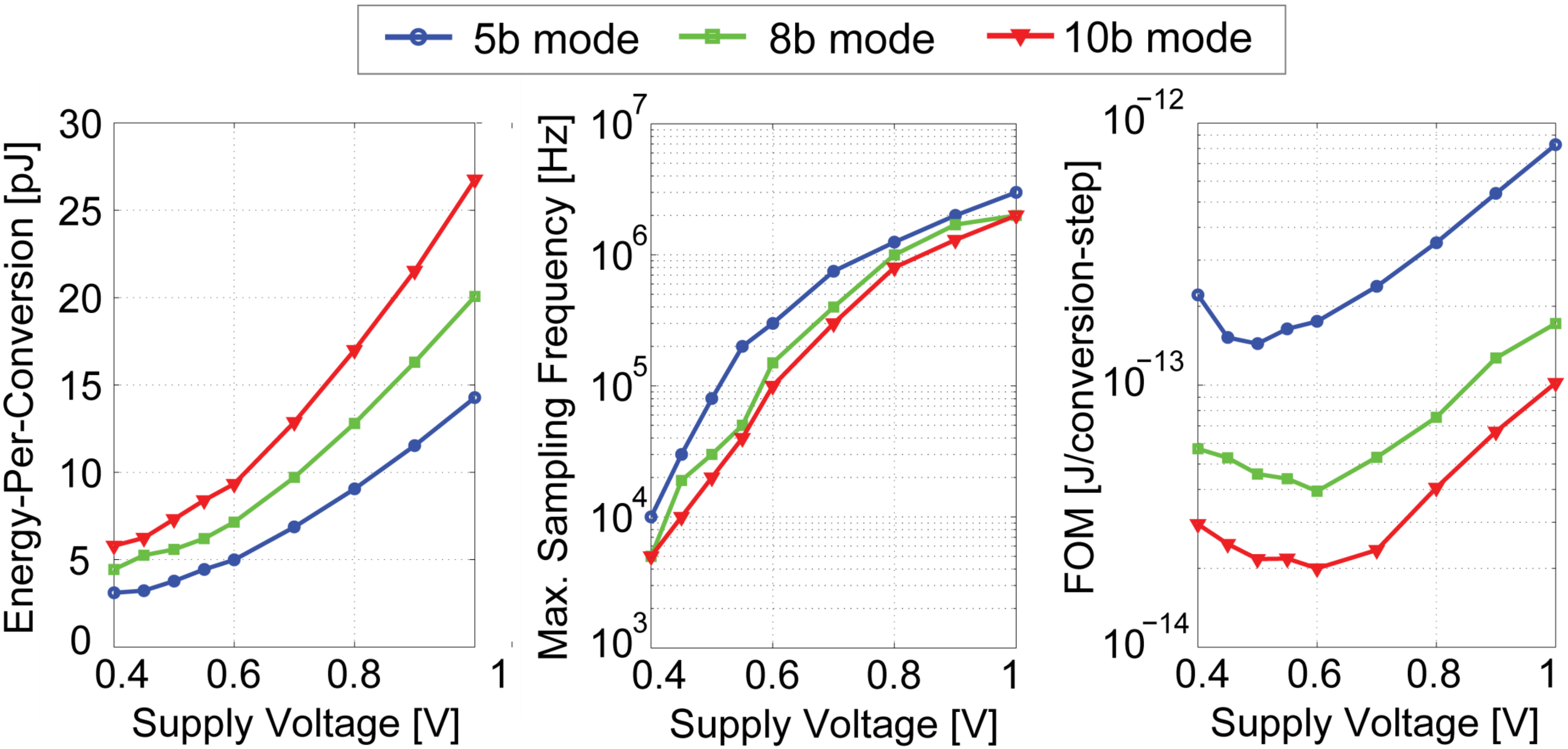


f_S=200kS/s

Optimum Efficiency Point



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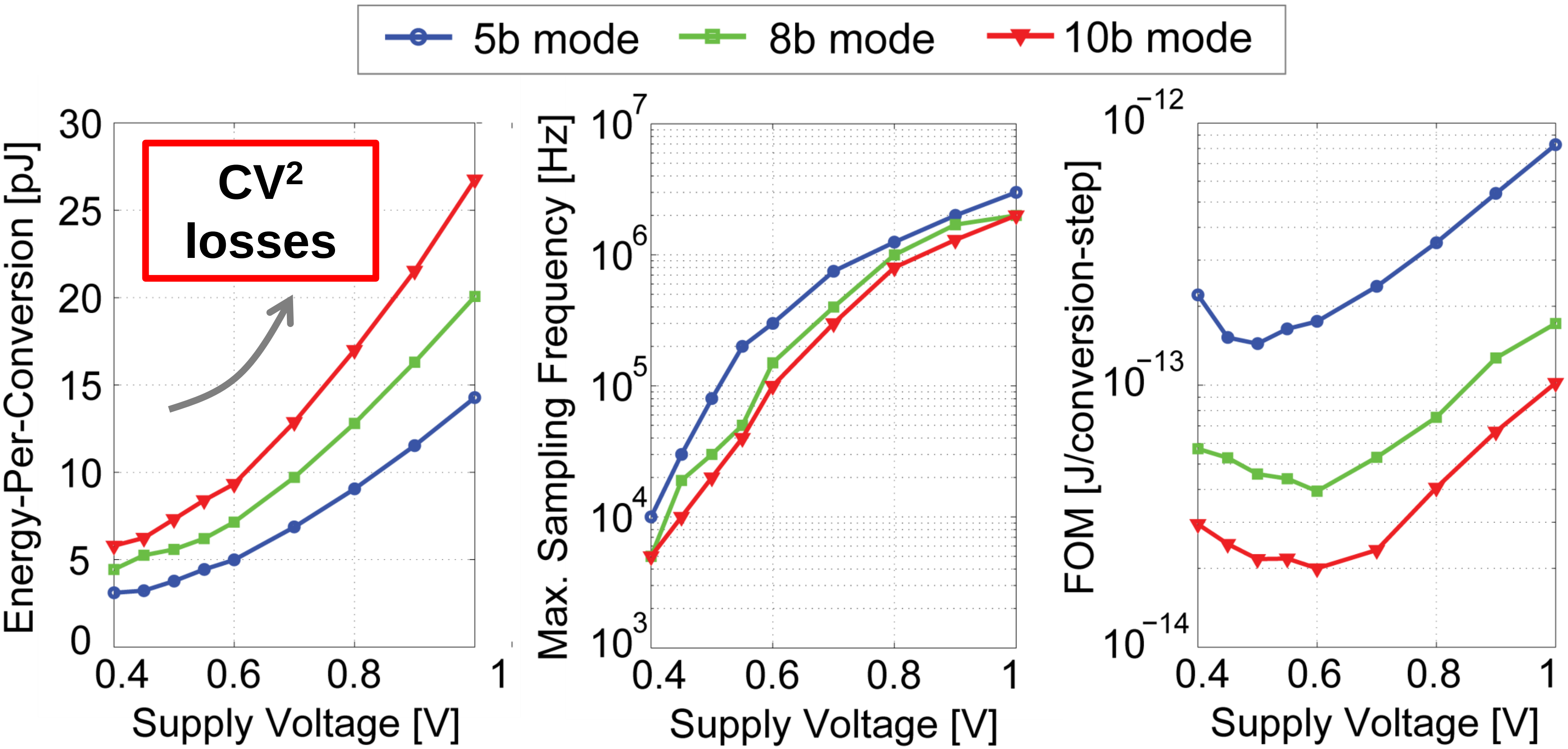

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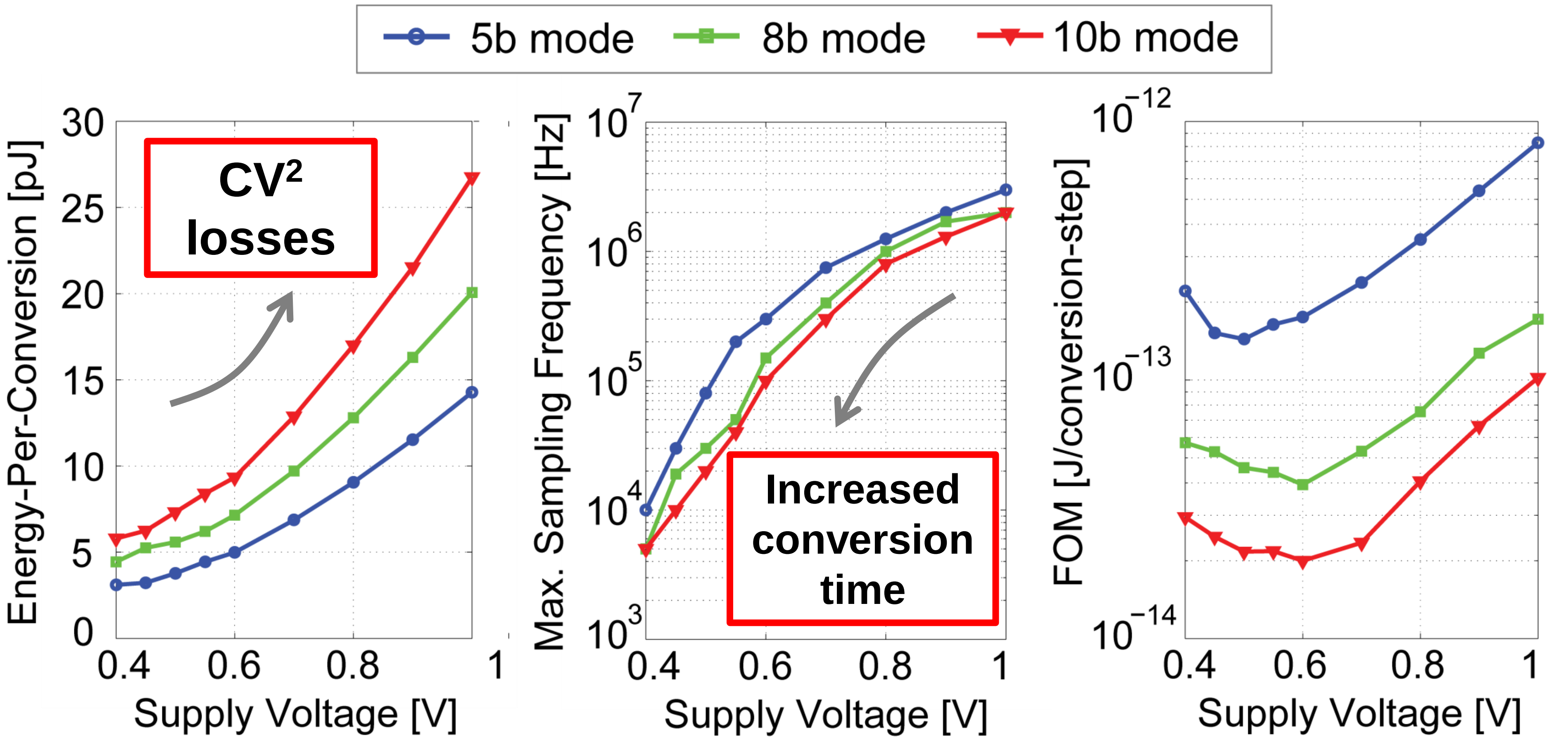

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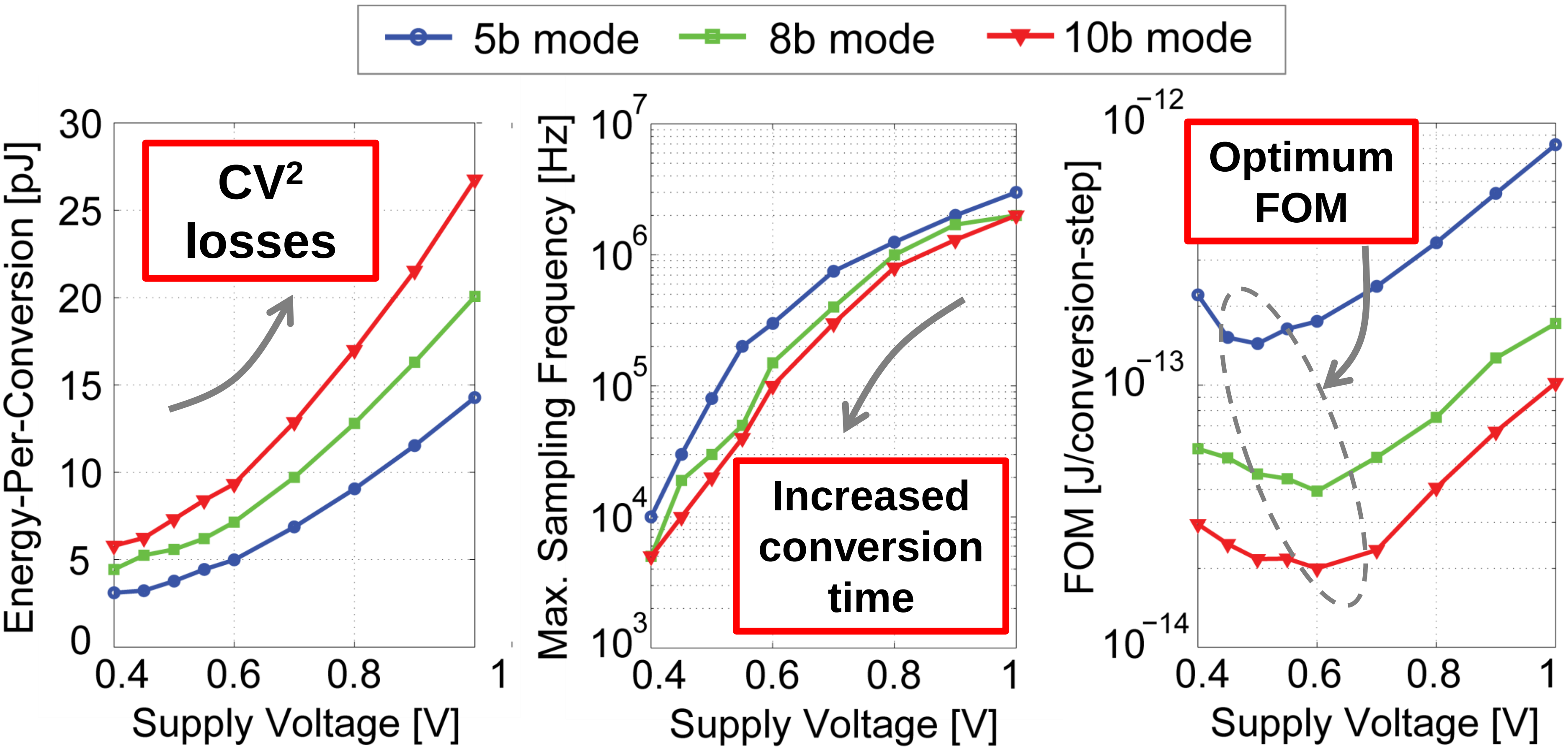
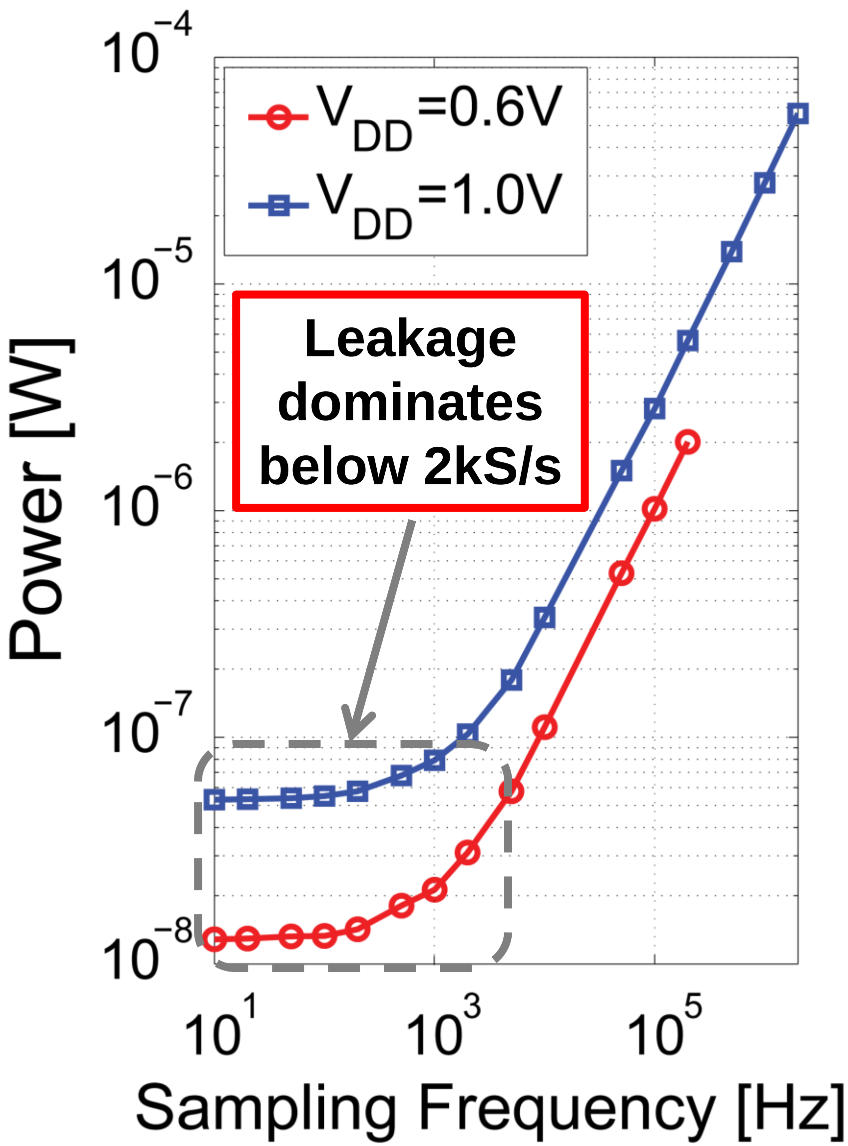
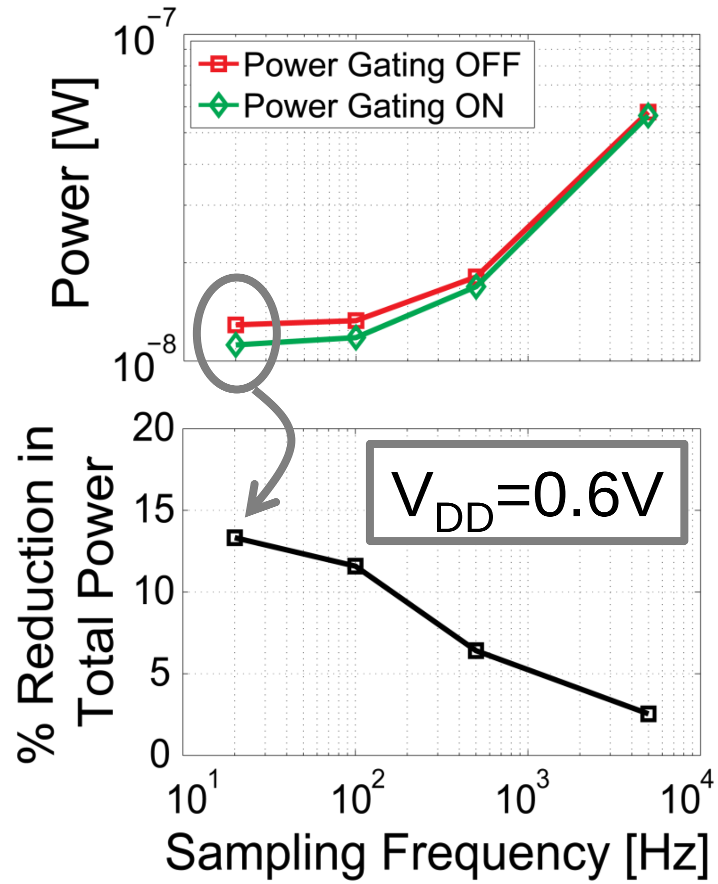


Power vs Sampling Frequency





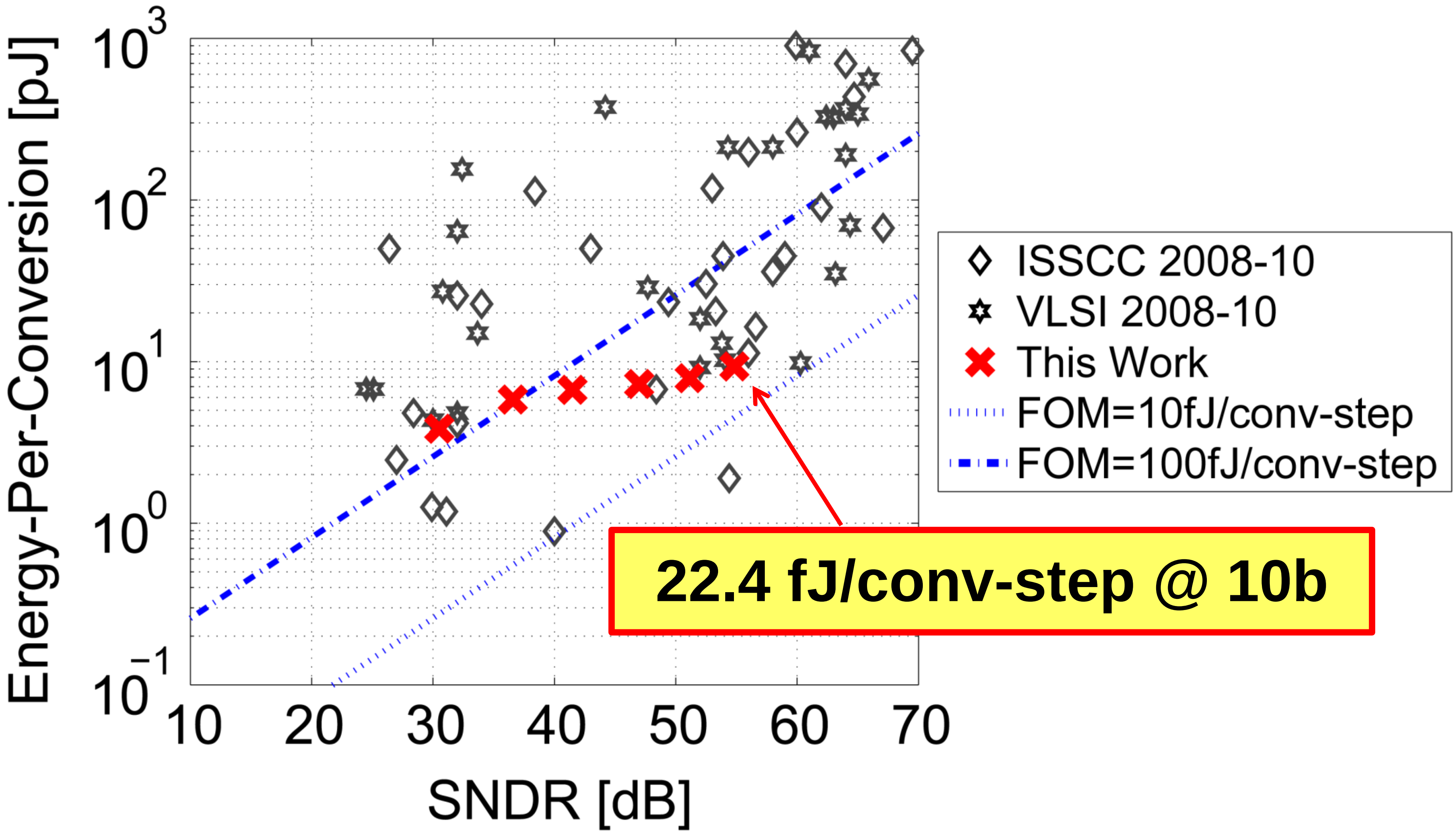
Leakage Power-Gating reduces total power by up to 14% at low frequencies

ADC Performance Summary

Active Die Area	0.212 mm^2 (65nm low-leakage CMOS)					
Supply Voltage (V_{DD})	0.4V to 1V (differential input range is $\pm V_{DD}$)					
Maximum Sampling Rate (all resolutions)	5kS/s @ 0.4V 2MS/s @ 1V					
Resolution Mode	5b	6b	7b	8b	9b	10b
INL [LSB] @ 0.6V, 100kS/s	0.07	0.33	0.33	0.43	0.50	0.57
DNL [LSB] @ 0.6V, 100kS/s	0.11	0.35	0.40	0.51	0.55	0.58
Dynamic Performance @ 0.55V, 20kS/s (*except for 5b data @ 0.5V, 60kS/s)						
SFDR [dB] @ Nyquist	*44.0	48.5	54.6	61.2	63.0	68.8
SNDR [dB] @ Nyquist	*30.4	36.6	41.5	47.0	51.2	55.0
ENOB	*4.77	5.79	6.60	7.51	8.21	8.84
Power Consumption [nW]	*234	116	133	146	159	206

10 samples tested

Comparison with State-of-the-Art



Data courtesy of B. Murmann, "ADC Performance Survey 1997-2010, [Online]".

Conclusion

- Power scalable SAR ADC with reconfigurable resolution (5 to 10b)
  - DAC resolution scaling
  - Voltage scaling
- Leakage power-gating important at low sample rates
- Energy-efficient over wide range of resolutions and sample rates

Acknowledgements:
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