18Gb/s Optical IO: VCSEL Driver and TIA in 90nm CMOS

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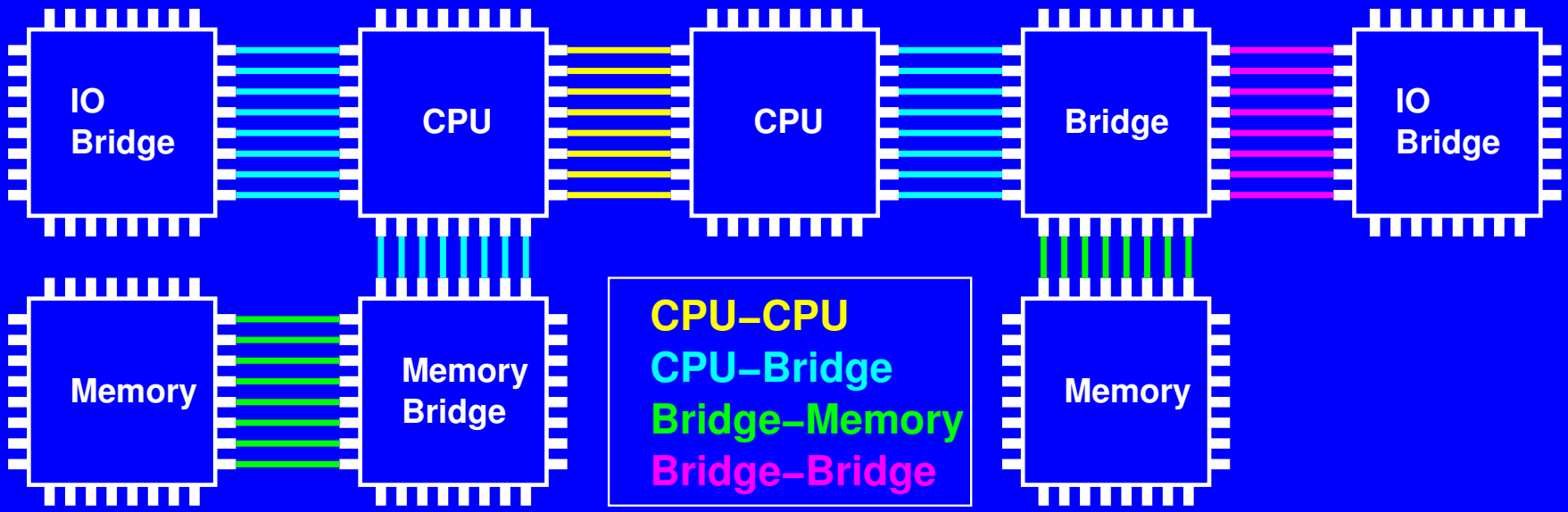
Outline

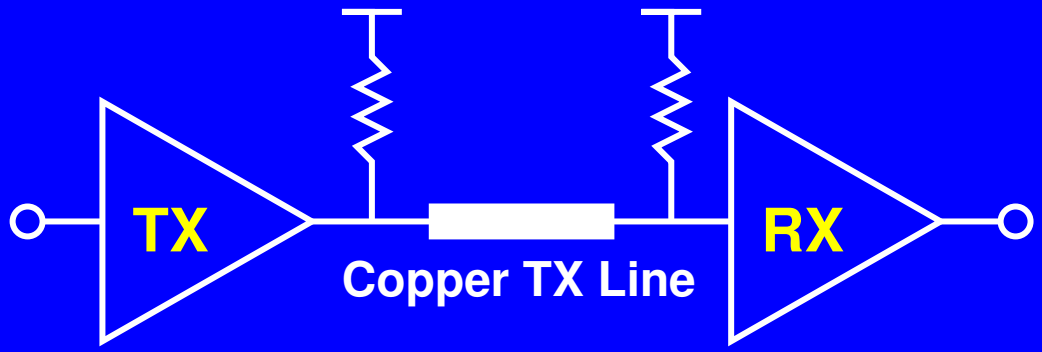
1. Introduction and Background
2. Pre-Emphasis VCSEL Driver
3. Cross-Coupled Cascode TIA
4. Conclusions

Applications for Optical IO



- IO performance requirements scale with processing power
- Optical IO has the potential to outperform electrical IO in the critical metrics of high data rate and low power consumption

Optical Versus Electrical Links



- **Electrical links: Performance is limited by copper traces**
  - **ISSCC(2006): 7” @ 20Gb/s with TX/RX equalization (Intel)**
- **Optical links: Performance is limited by optical components**
  - **VCSEL and photodiode properties directly influence data rate**
  - **Typical capacitance: 700fF for VCSEL and 250fF for PD**

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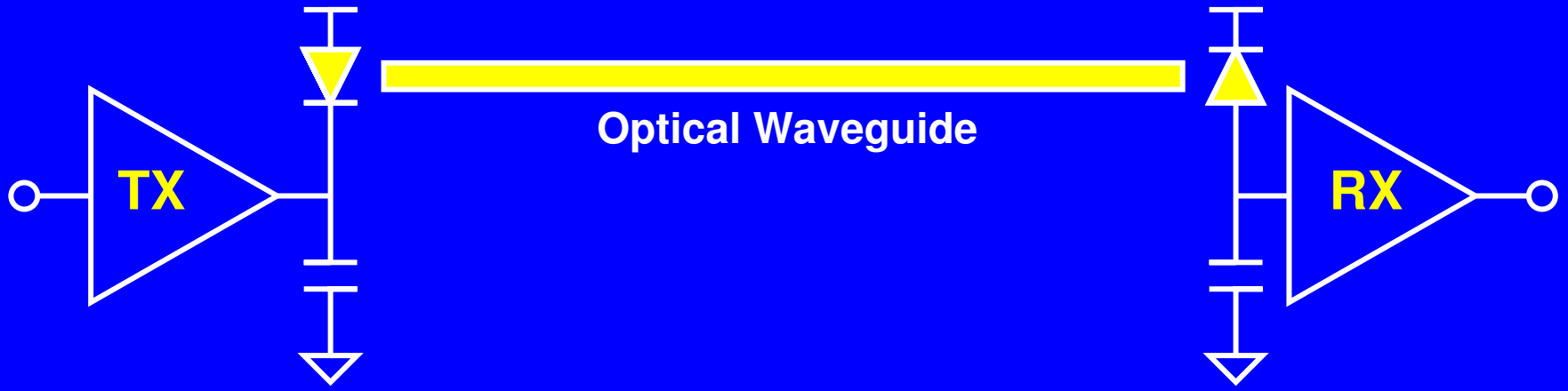

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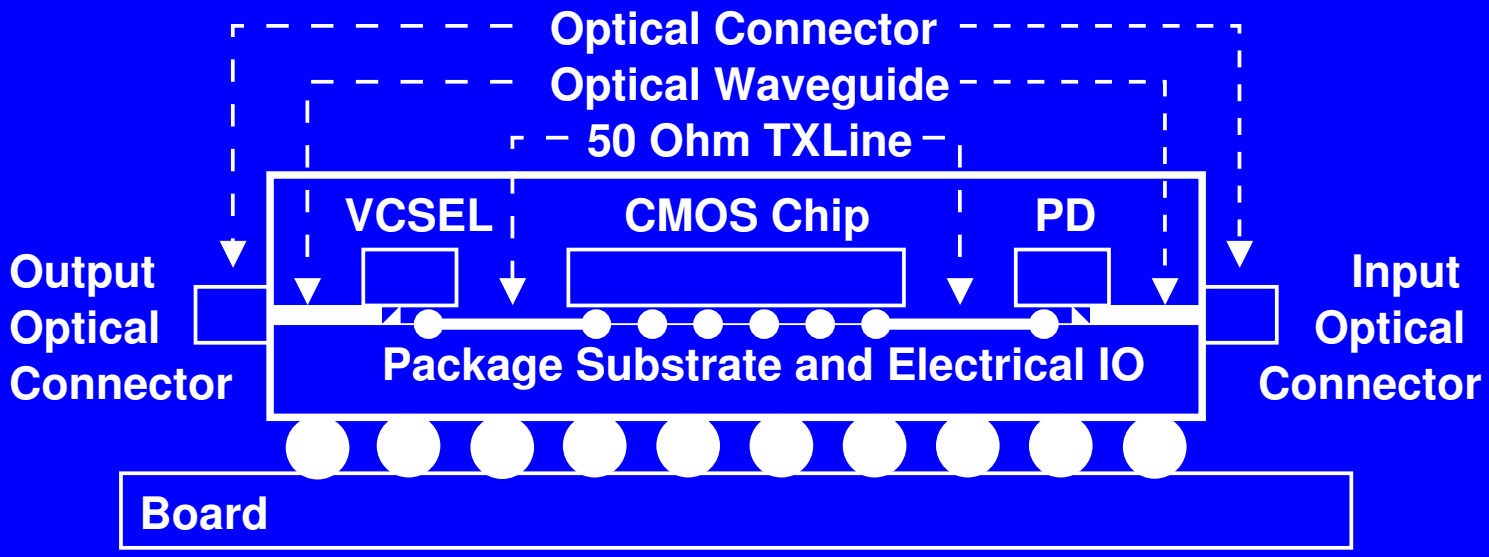
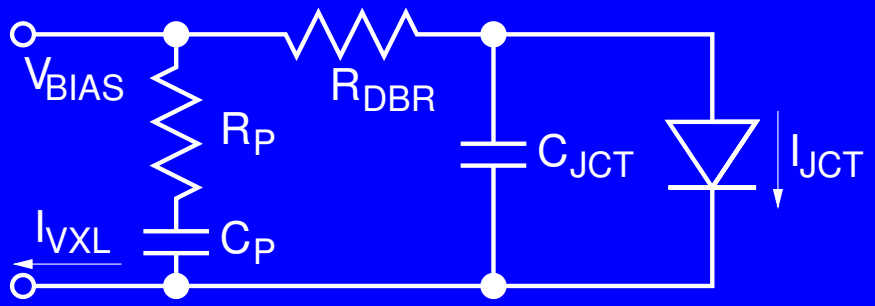
Link Overview and Design Criteria

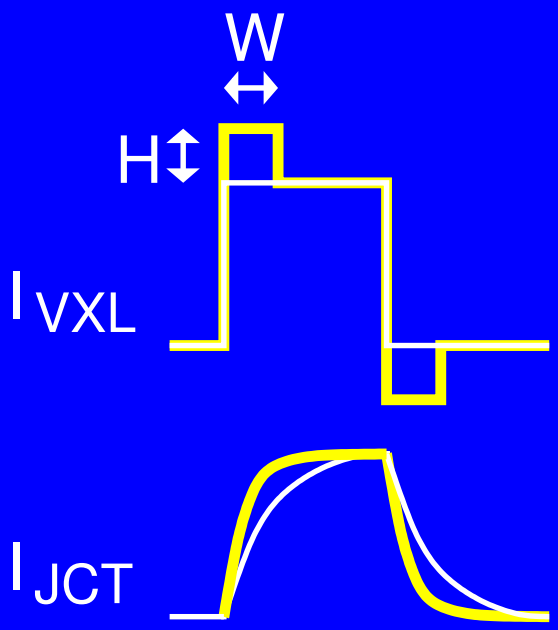


Reference: Intel Technology Journal. May, 2004.

- TX/RX designed for a link built with an Intel MCM package
- 50Ω termination included for package compatibility
- Circuit techniques are applied to maximize data rate
- Uses commercial GaAs components and no inductors

Pre-Emphasis Driver Concept





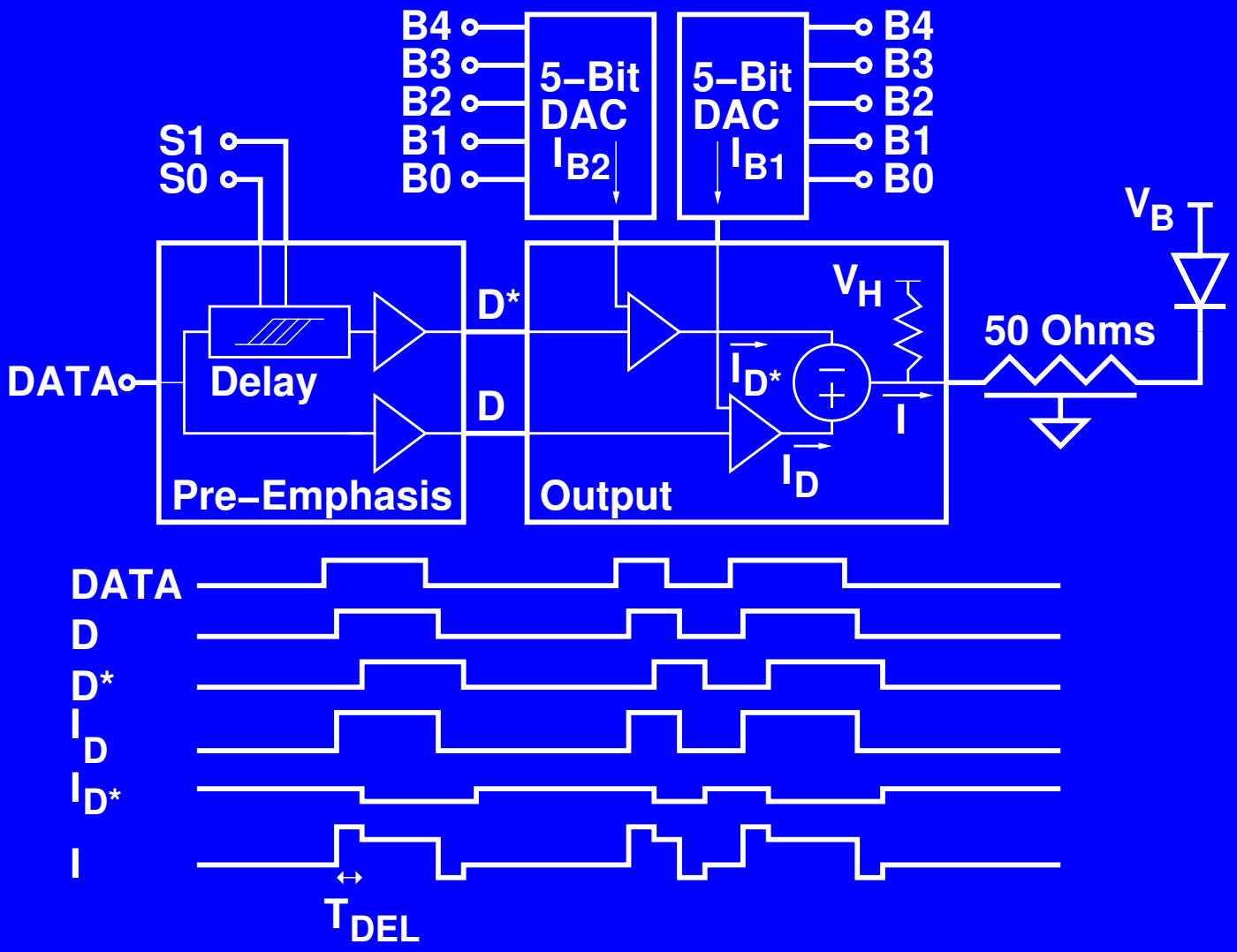
- Optical and electical VCSEL limitations
  - Relatively linear electrical parasitics
  - Non-linear optical dynamics: fast rising edge and slow falling edge
- Pre-emphasis can compensate for both of these limitations

Prior VCSEL Driver Work

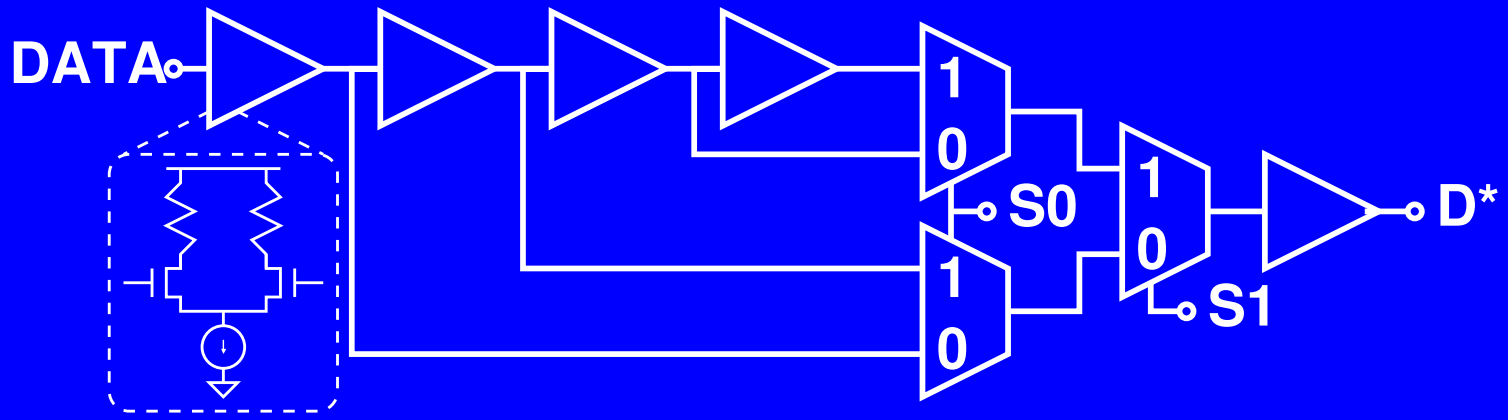
CMOS Process	0.13μm	90nm	90nm	90nm
VCSEL Material	InGaAs	GaAs	GaAs	GaAs
C_{VCSEL}	160fF	740fF	700fF	700fF
Data Rate	20Gb/s	10Gb/s	16Gb/s	18Gb/s
Power (mW/Gb/s)	3.5	2.1	3.0	7.1
Inductors?	Yes	Yes	No	No
Full Rate?	Yes	Yes	No	Yes
Reference	ISSCC (2005)	JSSC (2005)	ISSCC (2007)	This Work

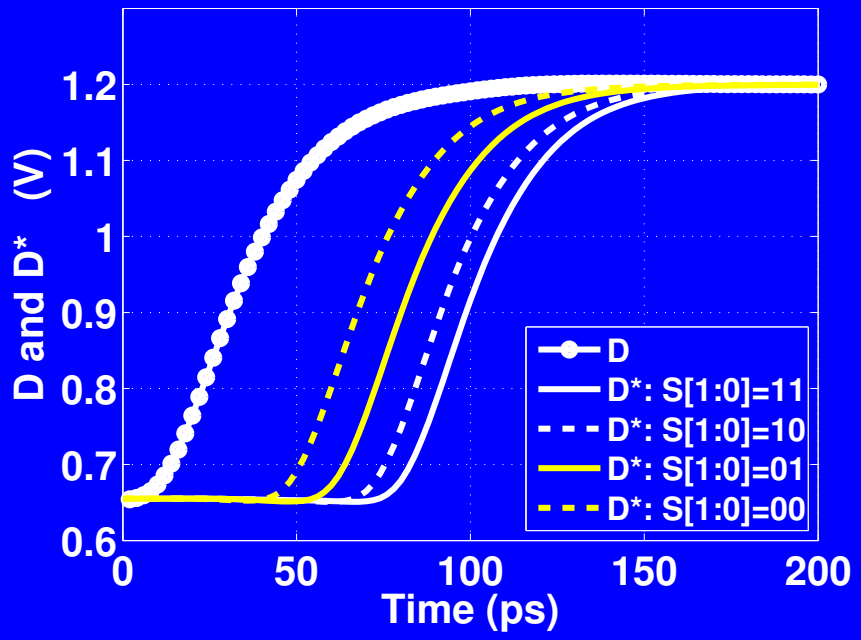
- This work presents: Full-rate, dual-edge pre-emphasis at 18Gb/s with a commercial GaAs VCSEL and no inductors

Driver Architecture



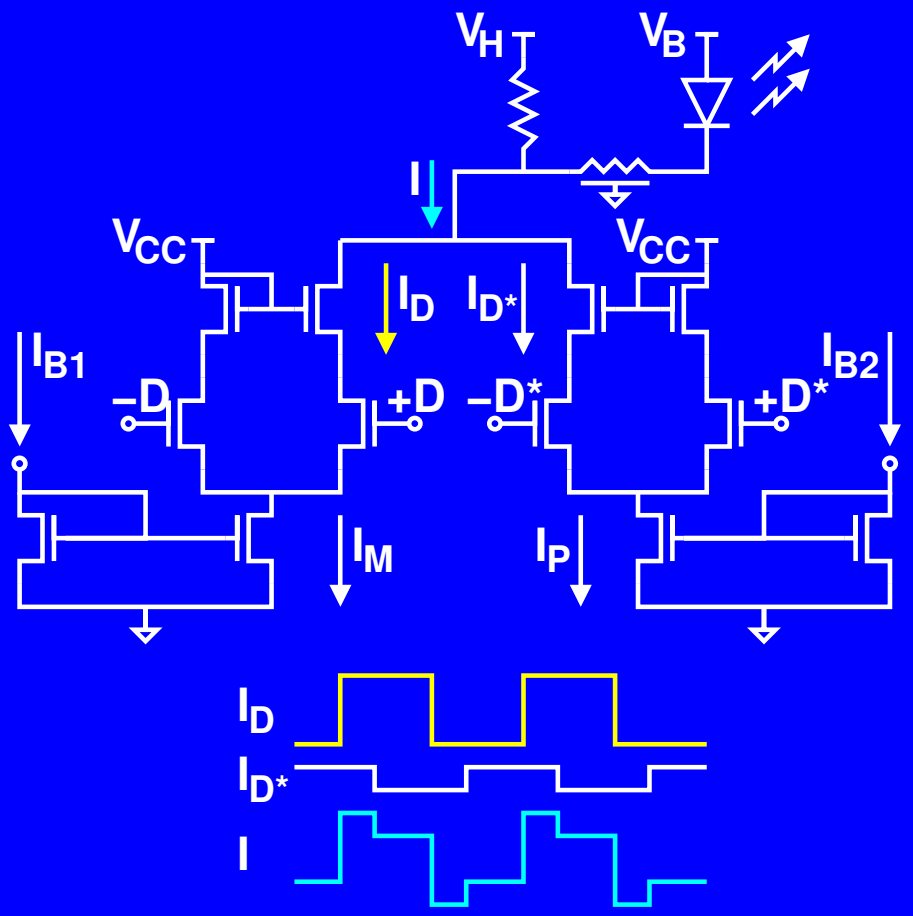
Delay Line





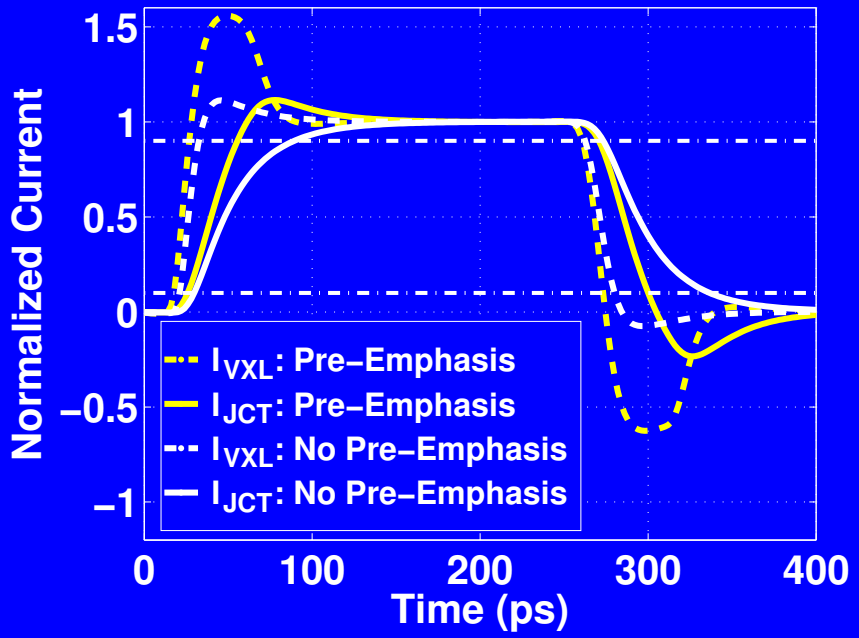
- Four delay stages
- Two-level MUX tree
- Range of 30ps to 60ps
- Resolution of 10ps per step
- Fine pulse width resolution for optimized pre-emphasis

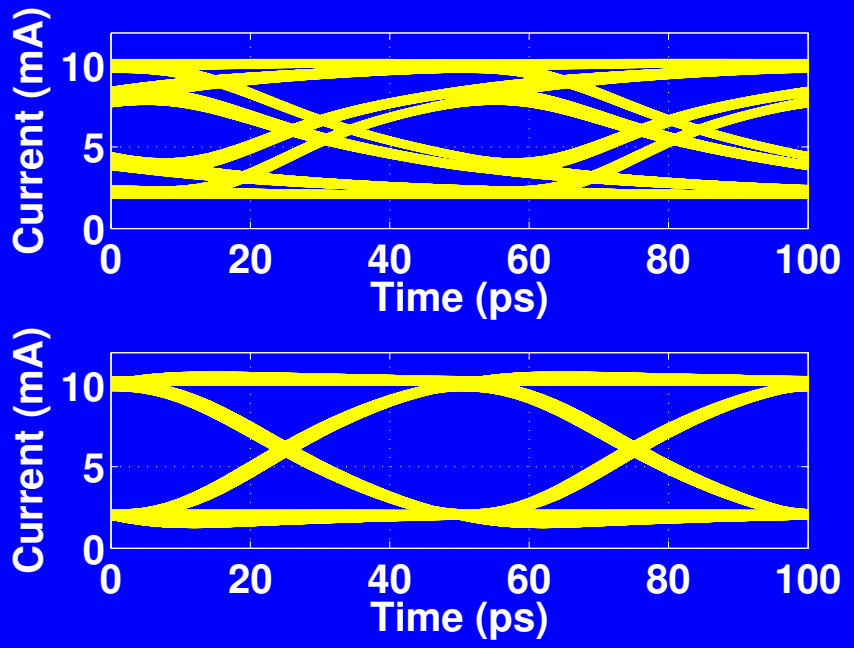
Output Stage



- Two 3:1 ratioed output stages
- Current summed at output node
- Cascodes isolate input pair from output swing
- IB1 and IB2 adjust modulation and pre-emphasis currents around nominal values

Pre-Emphasis Driver Simulations

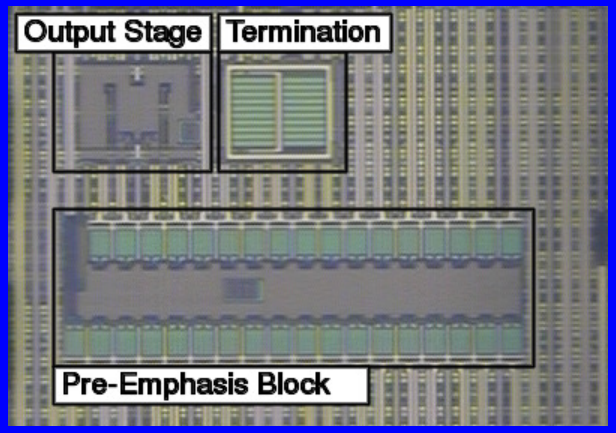




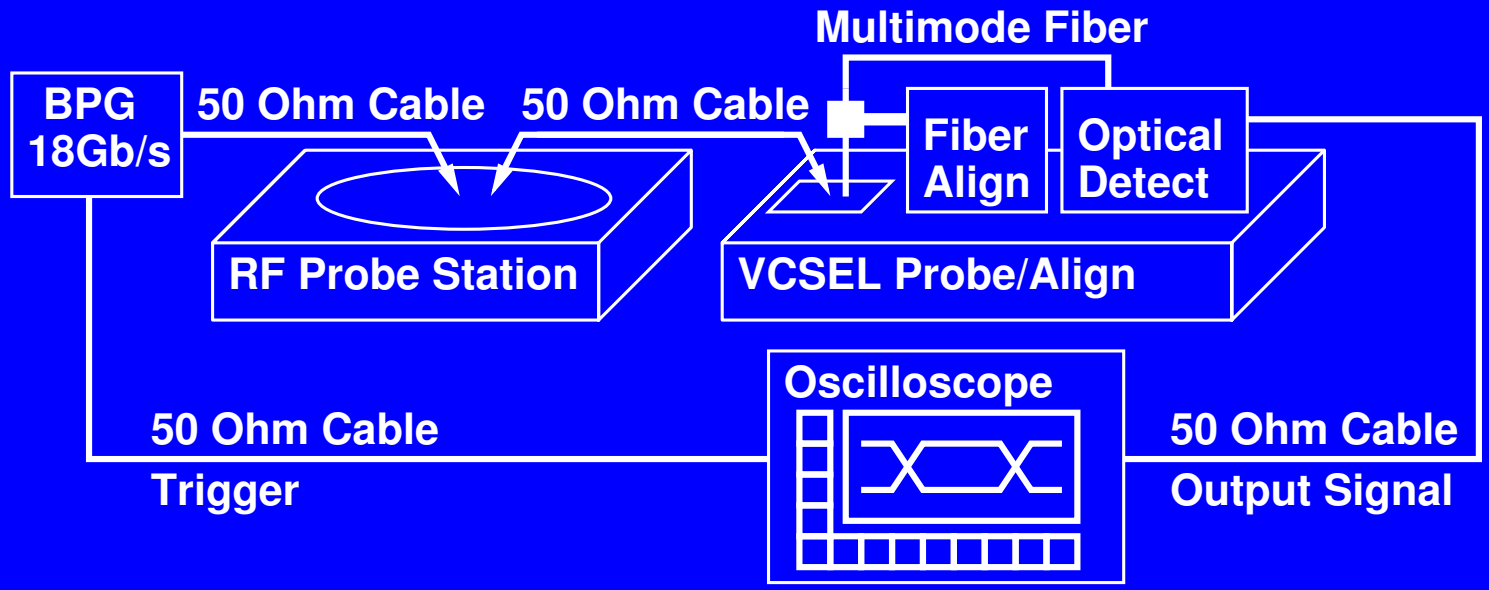
- Electrical simulations of pre-emphasis effect
- Pre-emphasis reduces transition time: 60ps to 30ps

- Electrical eye diagrams: 2mA to 10mA
- Pre-emphasis completely opens the electrical eye

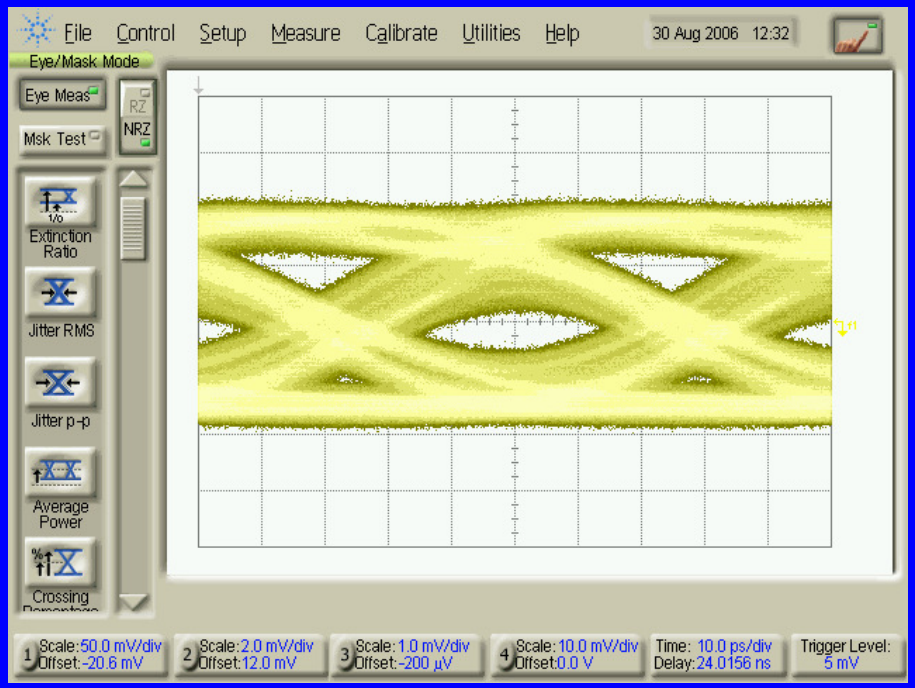
Fabrication and Testing



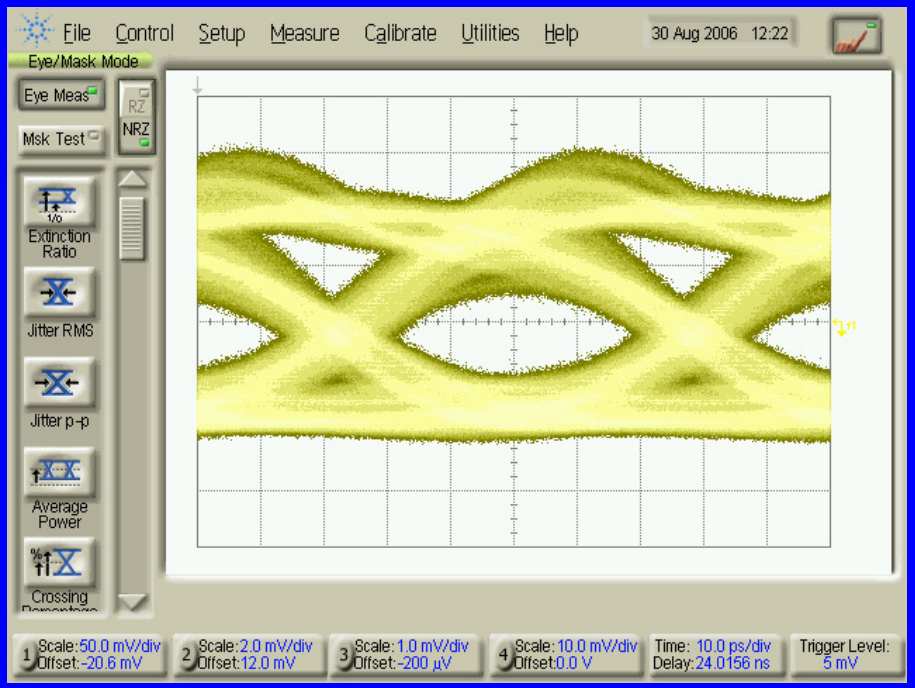
- Fabricated in 90nm CMOS
- Measured on RF probe station
- Probes connect CMOS to VCSEL
- VCSEL output measured with 12GHz NewFocus detector



18Gb/s Optical Eye Diagrams



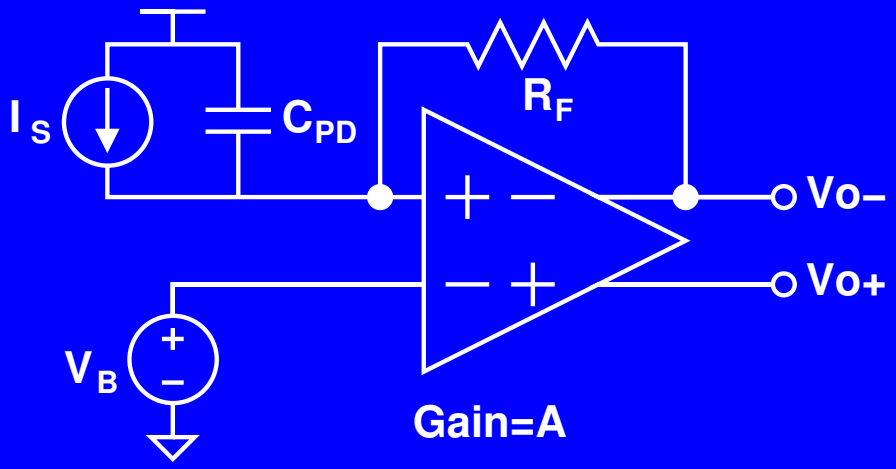
Without pre-emphasis



With pre-emphasis

- 2mA to 10mA modulation and 2.1dBm power at detector
- Improves vertical eye 122% and horizontal eye 76%
- Consumes 131mW/109mW power with/without pre-emphasis

Feedback TIA Theory



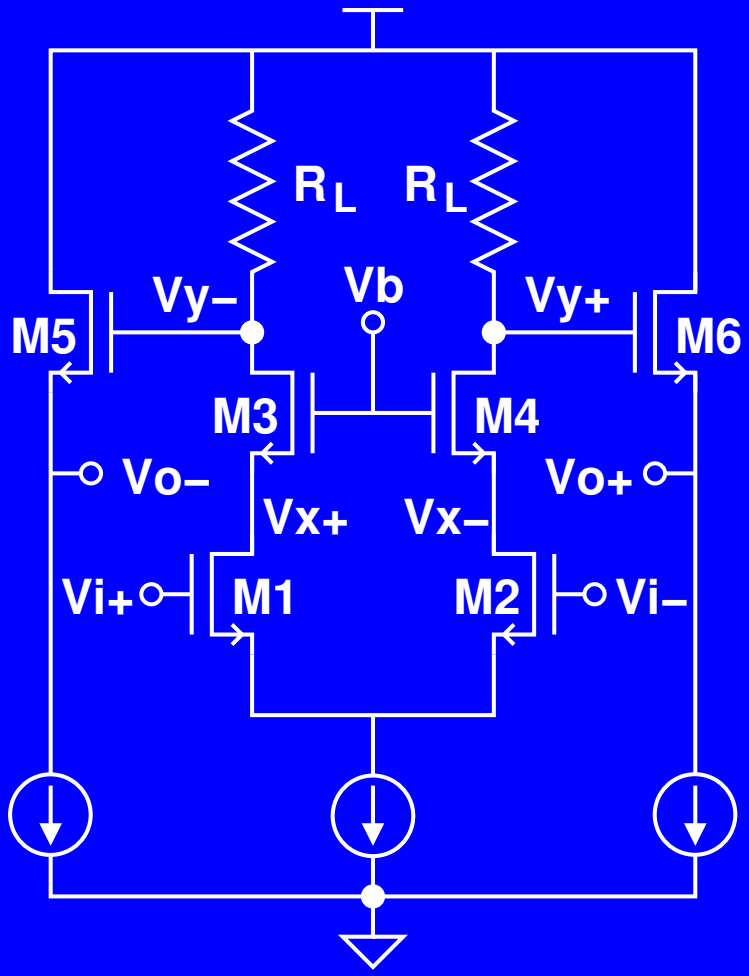
$$R_{IN} = \frac{1}{2\pi \cdot BW \cdot C_{PD}}$$

$$\frac{V_o}{I_S} = A \cdot R_{IN}$$

$$R_F = R_{IN} \cdot \left(1 + \frac{A}{2}\right)$$

- System specifications
  - Input current: 200μA
  - Output voltage: 2$\times$50mV
  - PD capacitance: 250fF
  - Target bandwidth: 10GHz
- TIA specifications
  - R_{IN}: 64Ω
  - A: 7.8 (2$\times$3.9)
  - R_F: 314Ω
- Other requirements
  - Single-ended input
  - Differential output
  - Broadband design

Core Voltage Amplifier Topology



Cascode Gain

$$\frac{V_{y+}}{V_{i+}} \approx \frac{g_{m1}}{G_L} \approx 4.8$$

Cross-Coupled Cascode Gain

$$\frac{V_{y+}}{V_{i+}} \approx \frac{g_{m1}}{G_L - g_{ds1}} \approx 9.1$$

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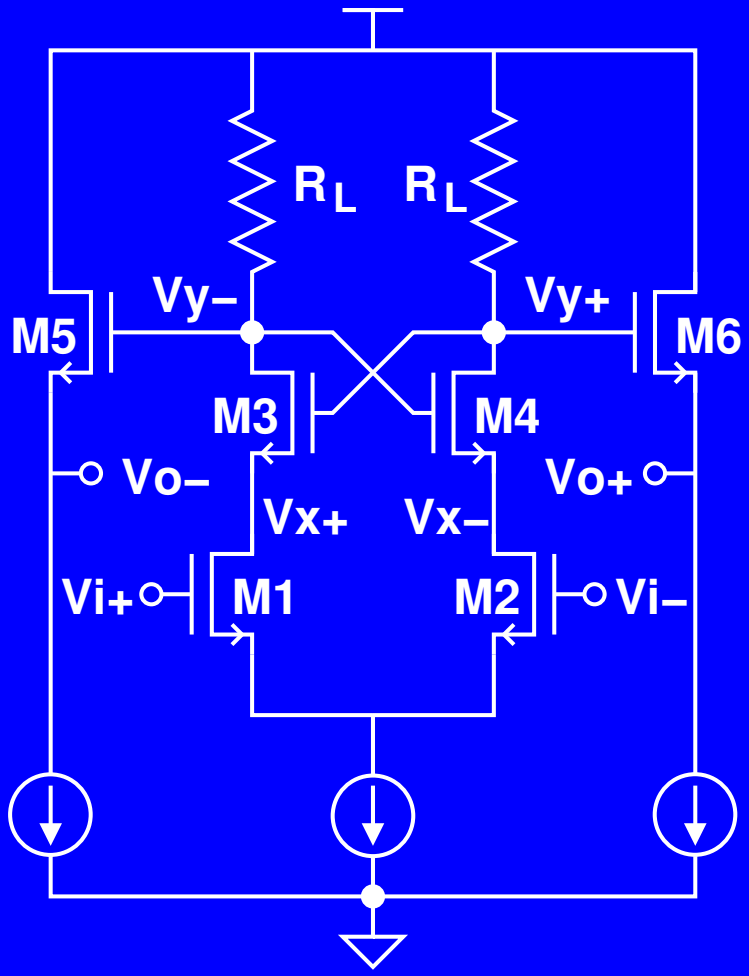

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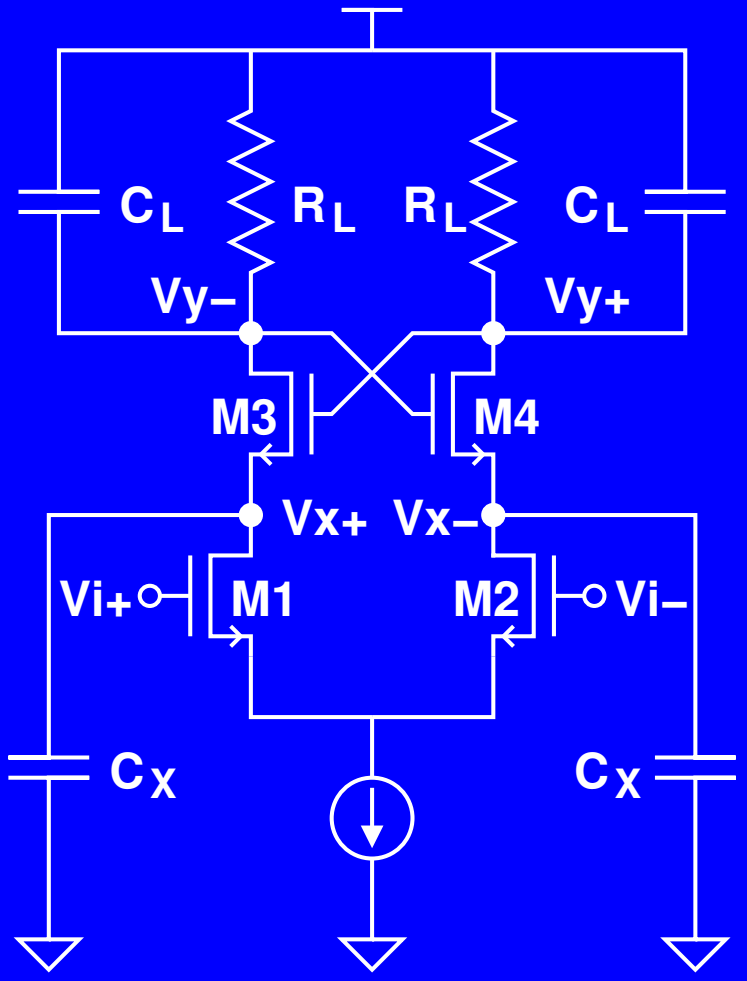
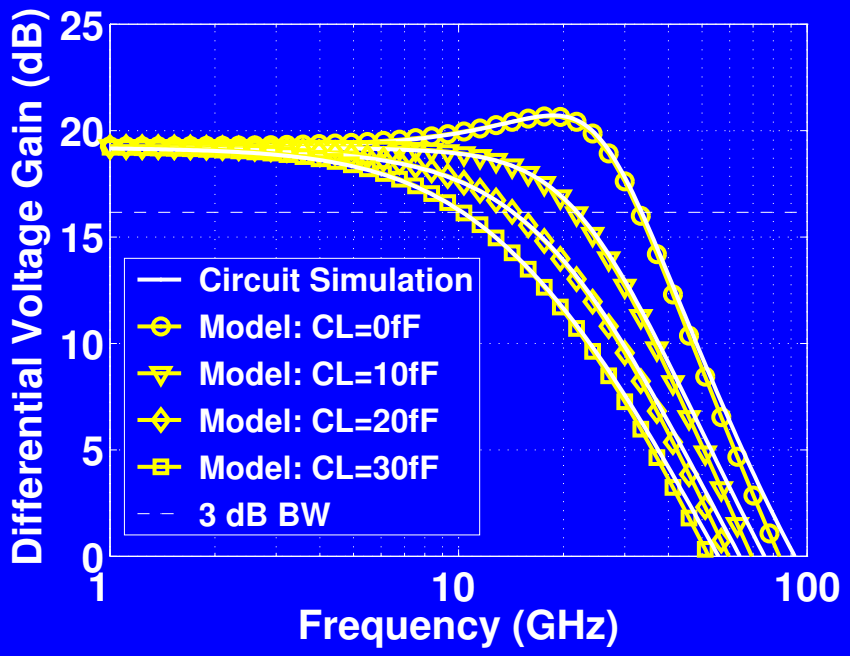


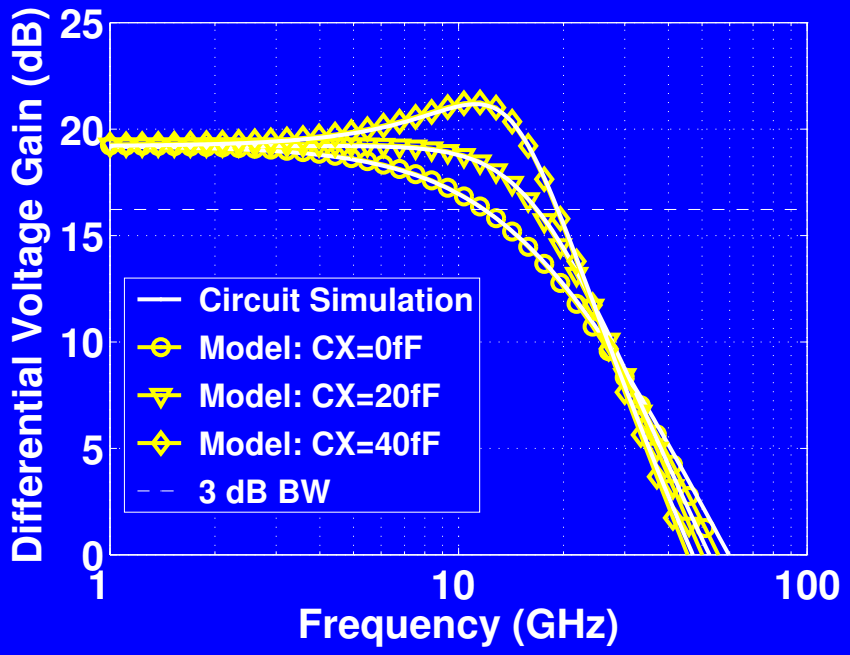
- Negative impedance from cross-coupled cascodes allows gain peaking to compensate for large C_L
- Larger C_X splits two poles into a complex pair
- Proper placement of the two poles maximizes bandwidth

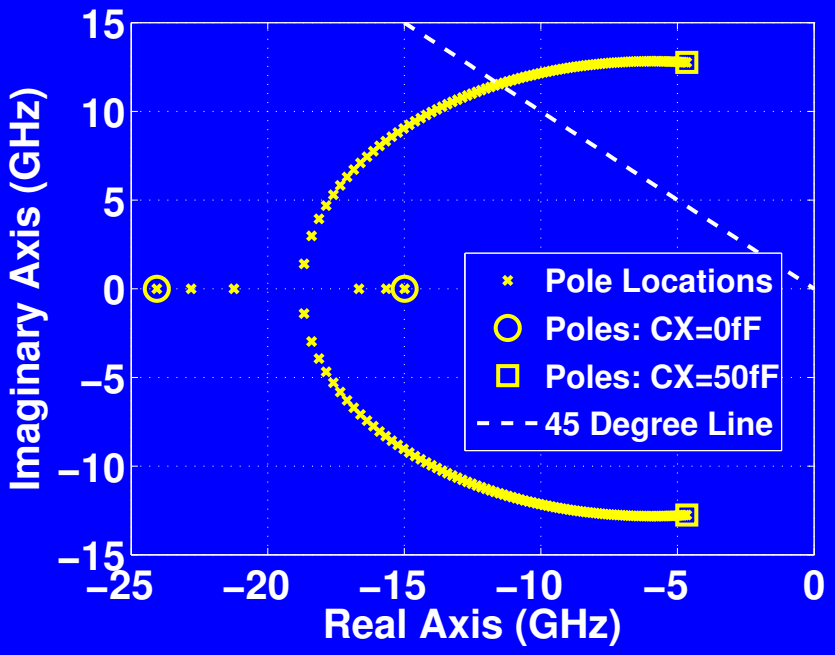
Sweep of Load Capacitance



- Load capacitance swept from 0fF to 30fF
- No additional peaking capacitance (C_X)
- Larger load capacitance limits amplifier bandwidth

Sweep of Peaking Capacitance C_X

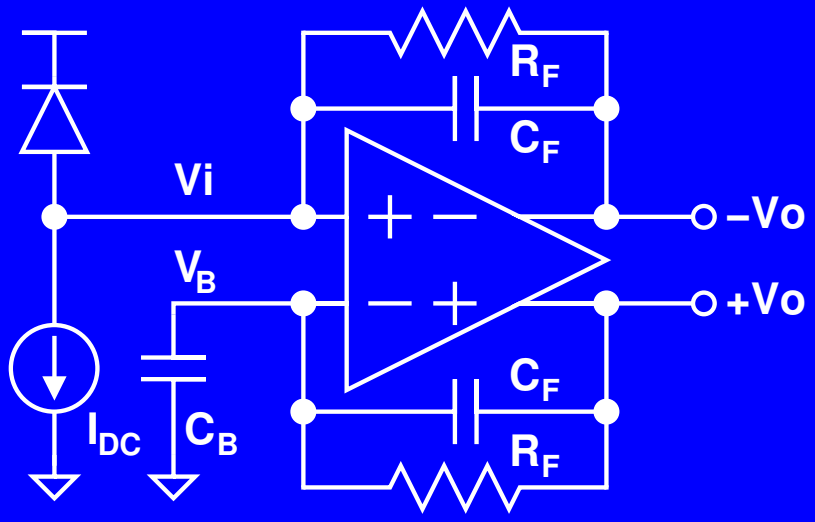




- Load capacitance: C_L=25fF
- Capacitance C_X swept from 0fF to 40fF in 20fF steps
- Larger C_X values increase amplifier gain peaking

- Poles are real for small C_X
- Larger C_X splits two real poles into a complex pair
- Optimal pole placement increases bandwidth

Feedback Biasing Configurations



- Symmetric feedback
- Bias set by low-pass filtering one output
- Reduced gain at frequencies lower than $R_F C_B$ filter cutoff

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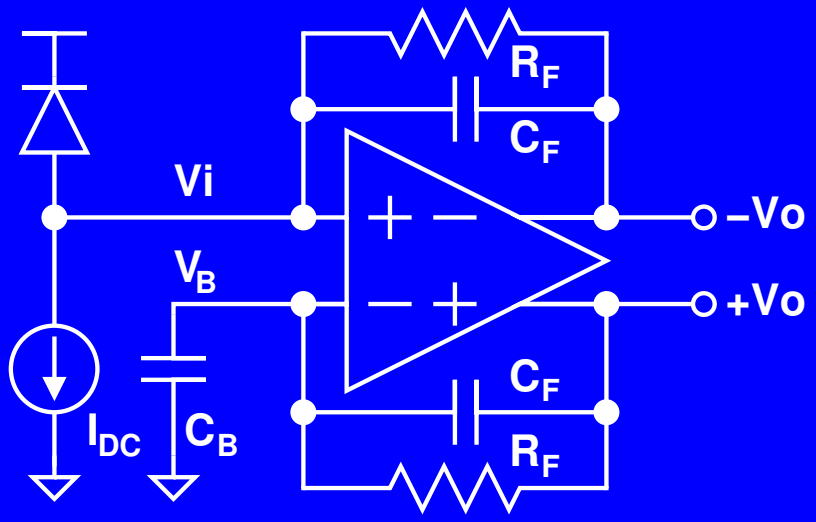

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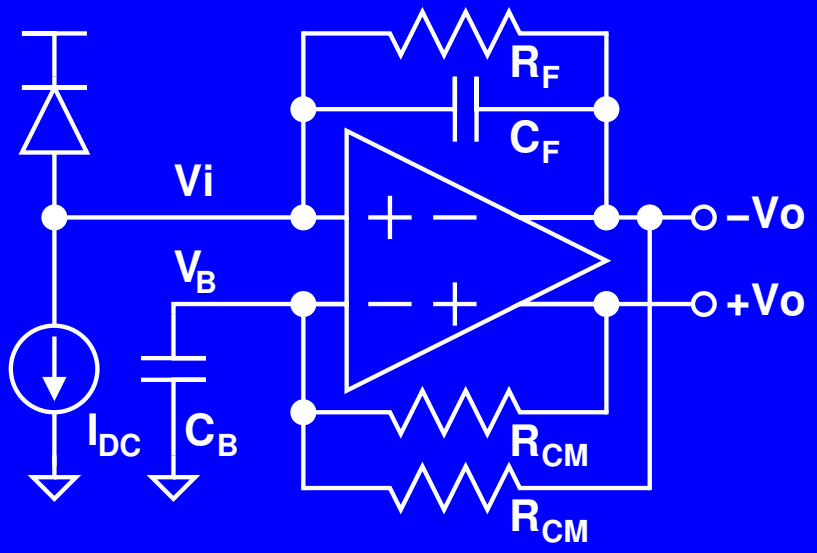
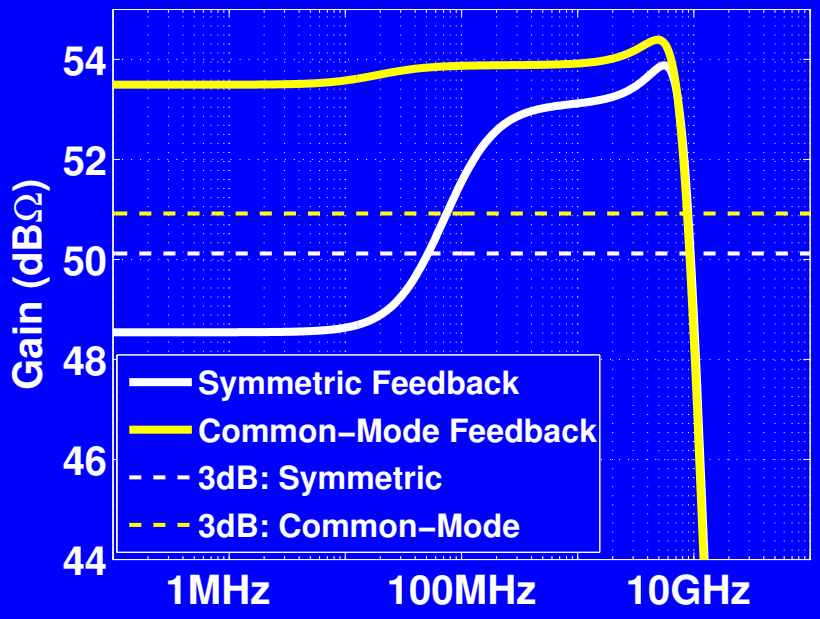


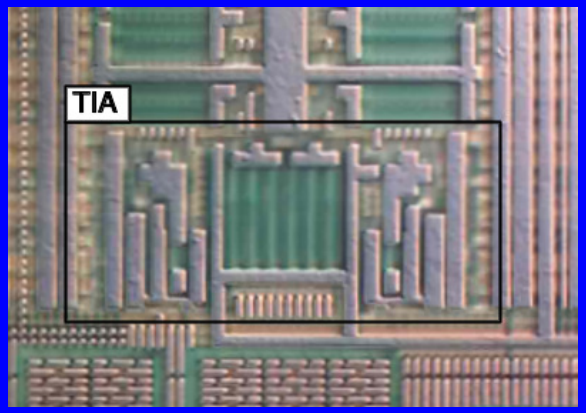
- Common-mode feedback
- Bias set by filtering the output common mode
- Bias independent of run length to first order

TIA: Extracted Simulations

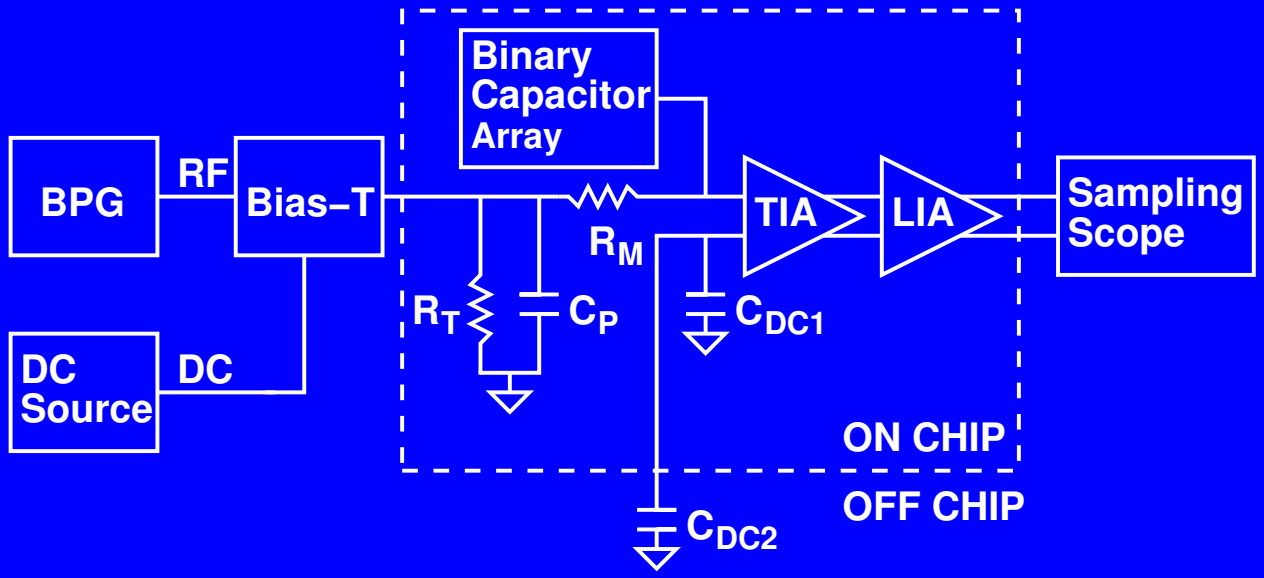


- Extracted simulations of feedback configurations
- 14mW power consumption
- Symmetric feedback
  - C_B=10pF
  - BW: 76MHz to 9.1GHz
  - Gain reduction: 4.7dBΩ
- Common-mode feedback
  - C_B=2pF
  - R_{CM}=8kΩ
  - BW: DC to 8.9GHz
  - Gain reduction: 0.4dBΩ

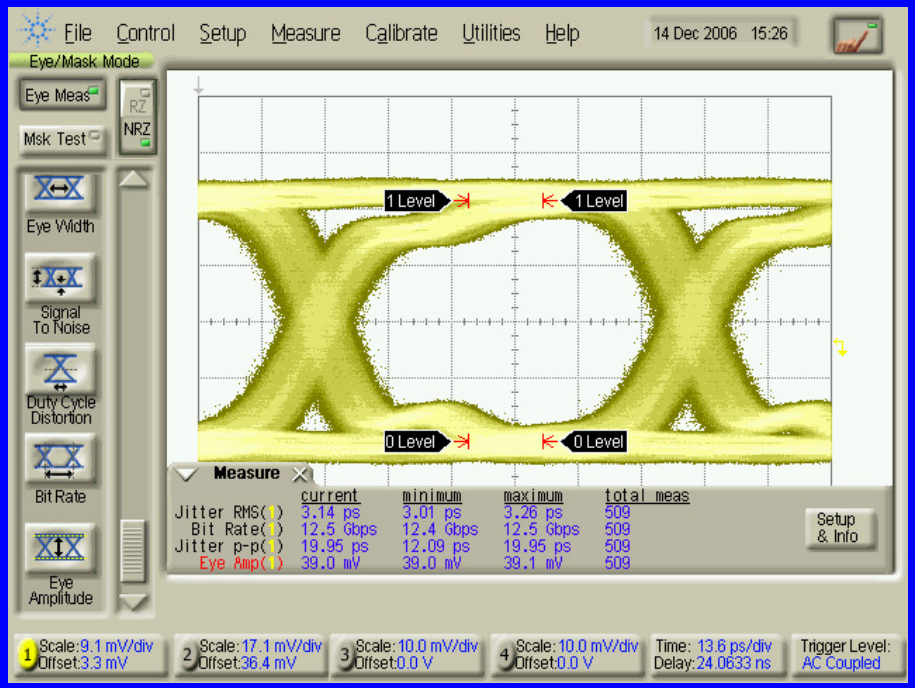
RF Measurement Setup



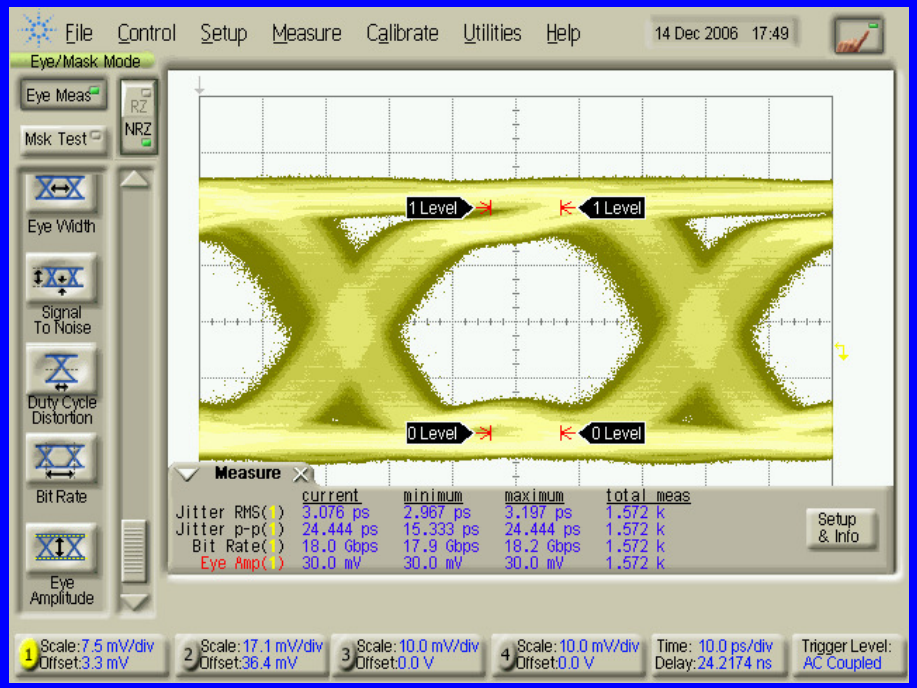
- Symmetric feedback configuration
- Electrical measurement of TIA+LIA completed using RF probe station
- On-chip binary capacitor array to test with varying capacitance



Data Rate Measurement with Varying Input Capacitance



- 12.5Gb/s
- 260fF input capacitance
- 200μA RF input current



- 18Gb/s
- 90fF input capacitance
- 200μA RF input current

Summary

- Pre-emphasis VCSEL driver
  - Optical data rate of 18Gb/s with GaAs VCSEL
  - Full-rate architecture with digitally-tunable pre-emphasis
- Cross-coupled cascode TIA
  - Cross-coupled cascodes increase gain and bandwidth
  - Data rate of 12.5Gb/s with 260fF input capacitance
  - Reducing input capacitance to 90fF allows 18Gb/s operation

Acknowledgements

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