A 180mV FFT Processor Using Subthreshold Circuit Techniques

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Extreme Sensor Networking

Emerging Sensor Applications

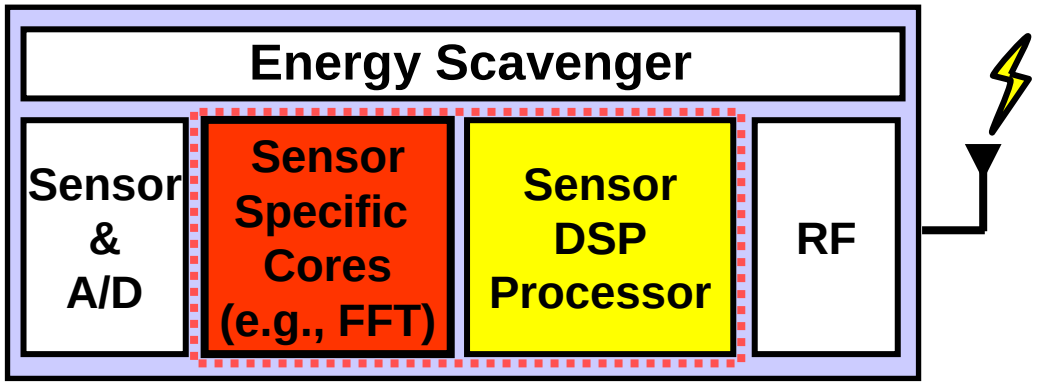
Target Tracking & Detection (Courtesy of ARL)

Operating Room of the Future (courtesy John Guttag)

Machine Monitoring (courtesy ABB)

Enabler: Self-Powered Sensor System

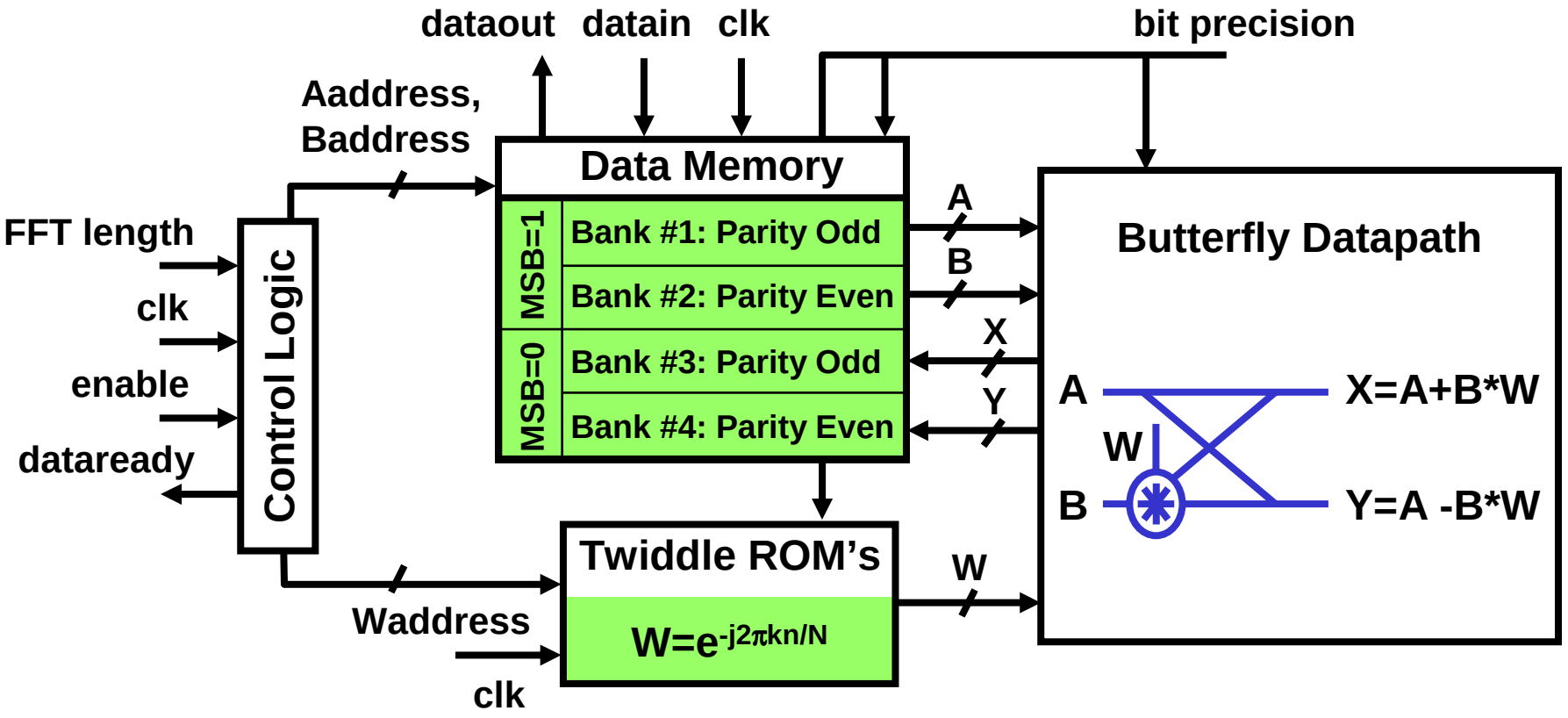
System Power < 10μW for Energy Scavenging



Design Considerations

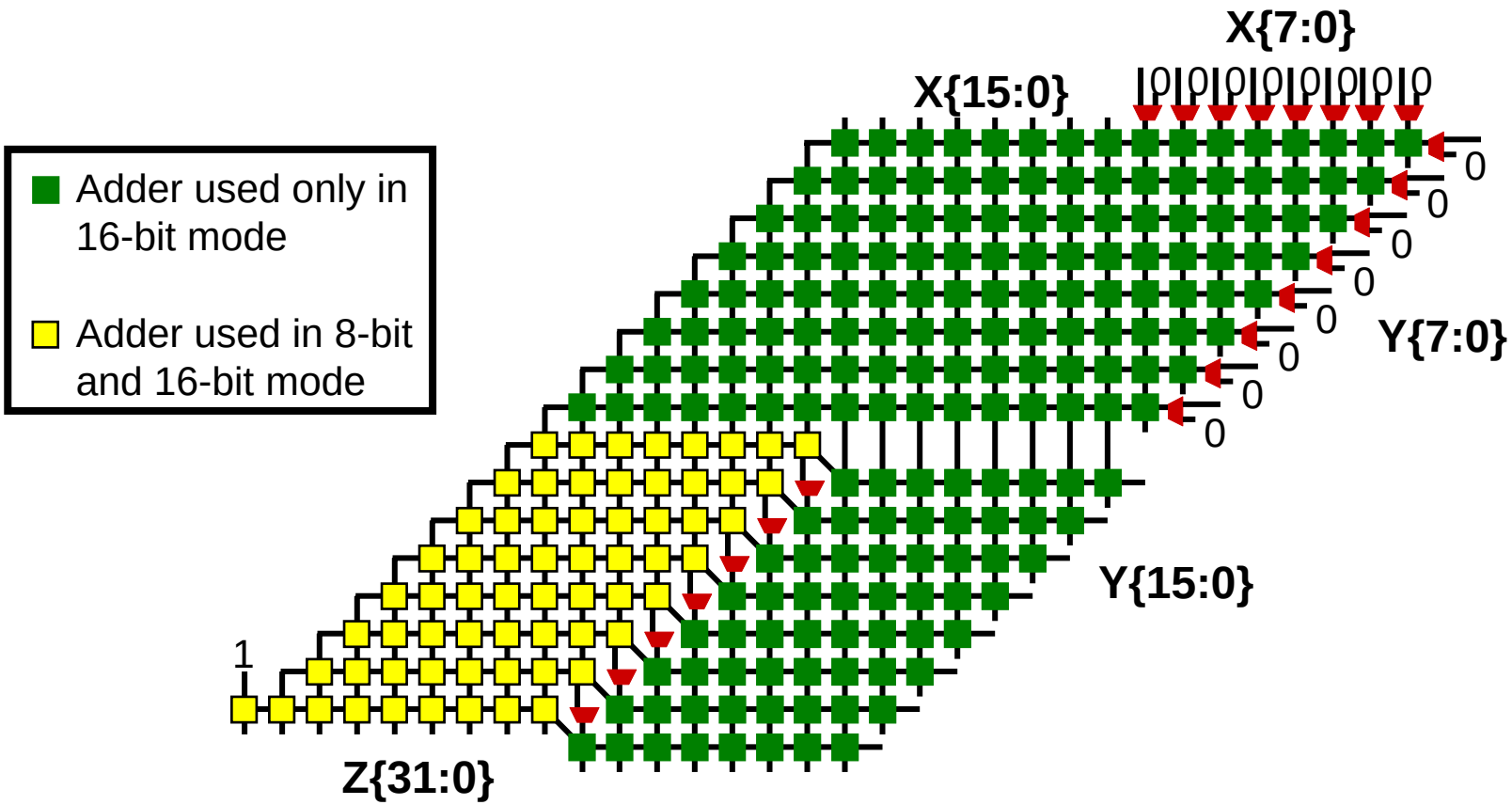
- For emerging low-performance microsensor applications, **computing speed is not critical**. Energy dissipation per function must be minimized.
- Traditional low-power design is optimized for the worst-case operating scenario.
- Significant diversity in operating scenarios:
  - Operating modes: threshold detection (low-activity), source detection (medium-activity), localization and classification (high-activity)
  - Event statistics
  - User-specified latency and quality
- The **node must be energy aware** and able to adapt energy consumption over a variety of operating scenarios.

Energy Aware FFT Architecture



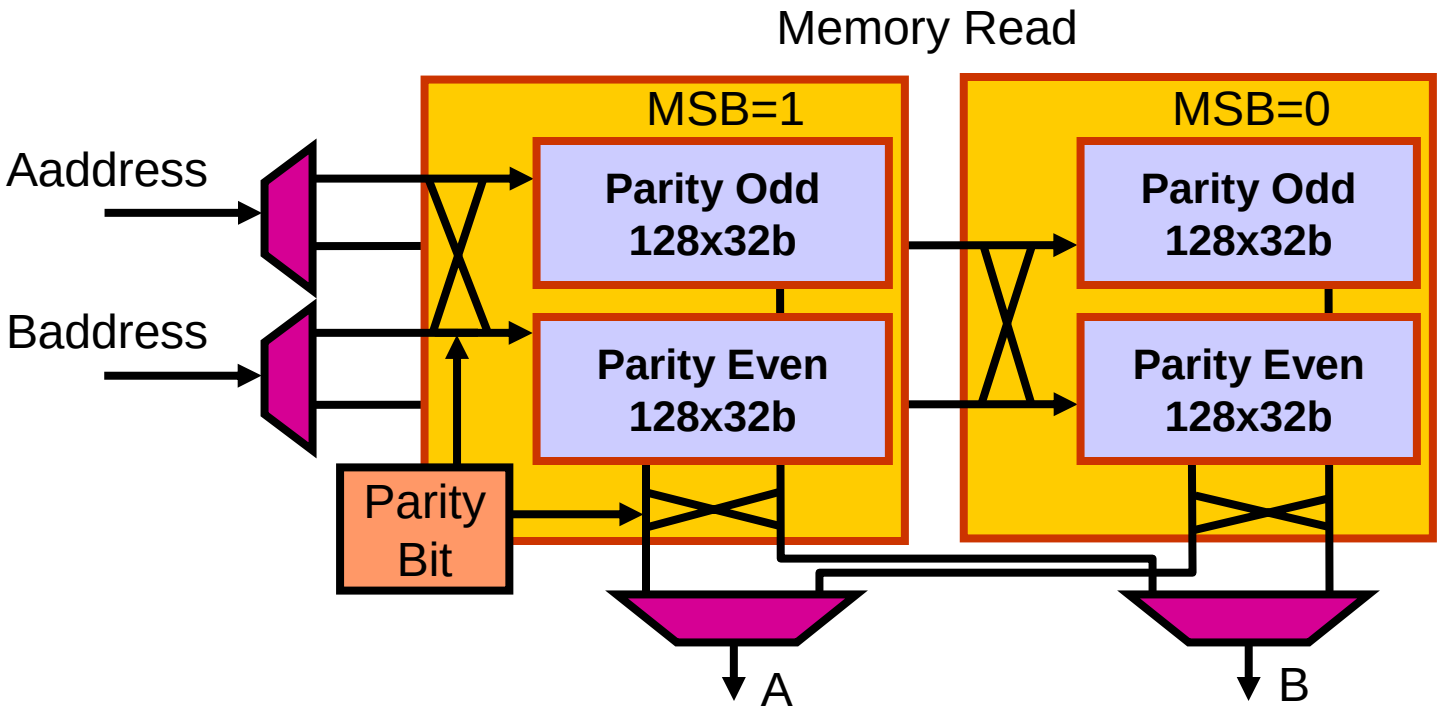
- Energy aware FFT architecture scales gracefully from 128 to 1024 point lengths and supports 8b and 16b precision.

Bit-scalable Baugh-Wooley Multiplier



- Fine-grained gating reduces activity factor and achieves energy savings with minimal area overhead.
- Bit-precision scaling architectures are used in the butterfly datapath, data memory and Twiddle ROMs.

Variable FFT Length

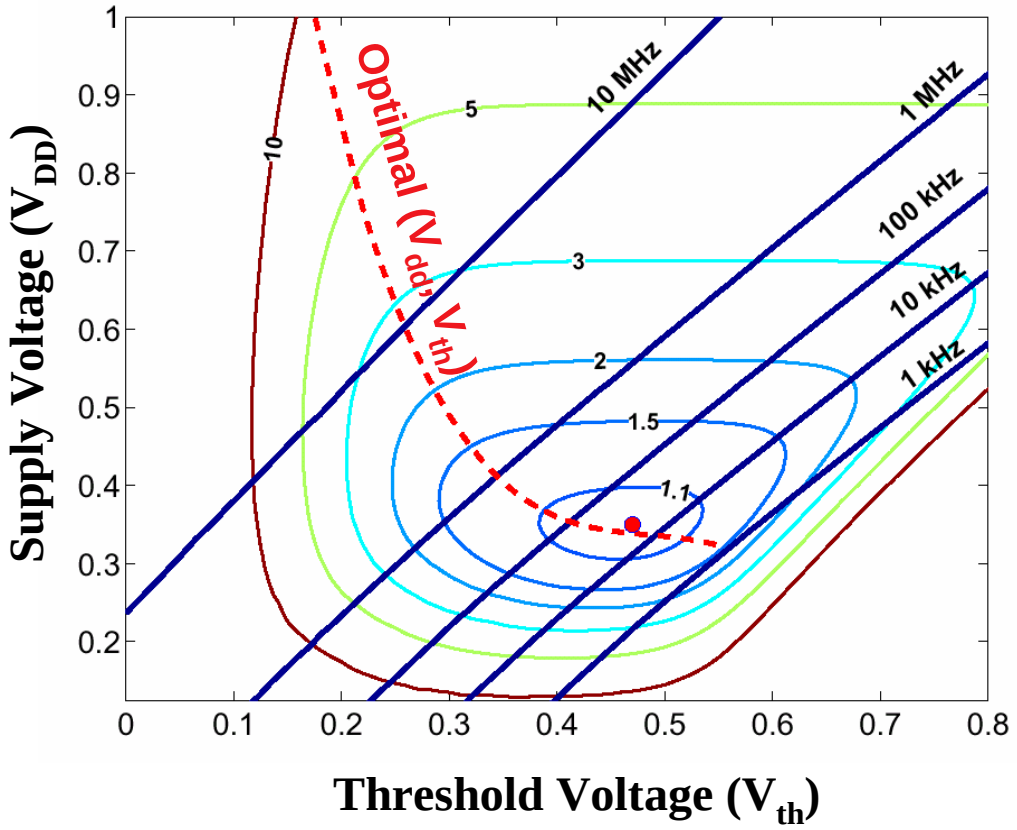


- Dedicated memory structure contains an MSB and parity-bit crossbar to avoid read/write hazards.
- The energy aware control logic scales the number of butterflies with FFT length.

FFT Energy/Performance Contours

$$E_{Switching} = a \cdot C_L \cdot V_{DD}^{\ 2}$$

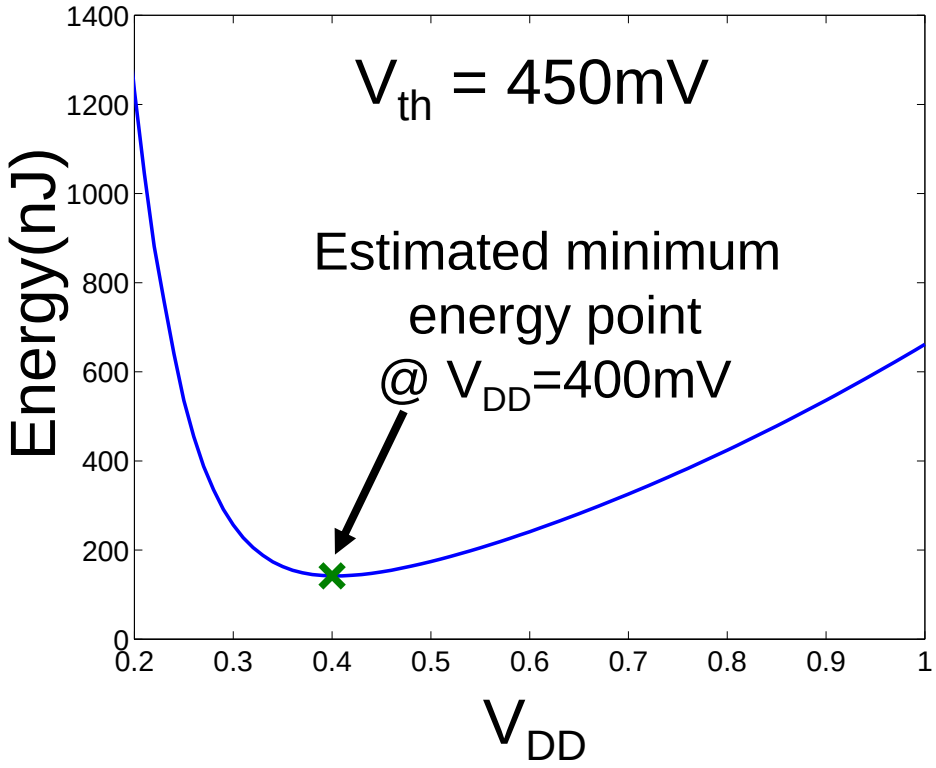
$$E_{Leakage} = I_S \cdot V_{DD} \cdot 10^{-\frac{V_{th}}{S}} \cdot T$$



- The optimal V_{DD} for the 1024-point, 16b FFT is estimated from switching and leakage models for a 0.18µm process.

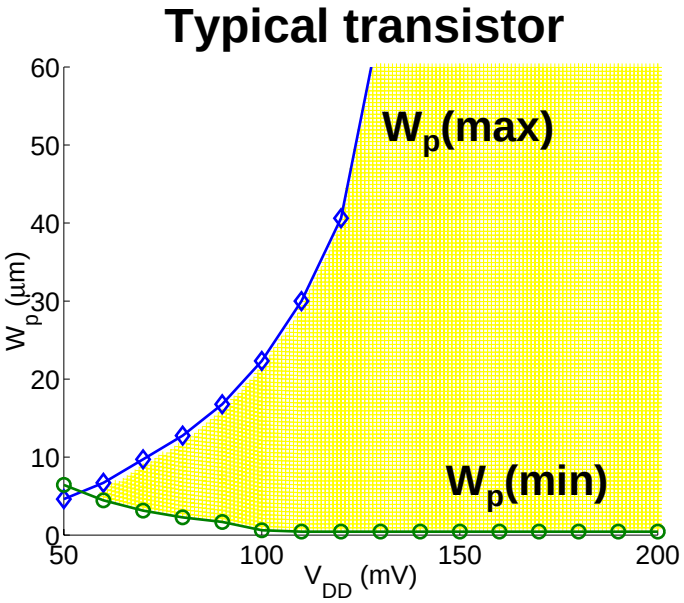
Exploit Subthreshold Operation for Sensor Circuits

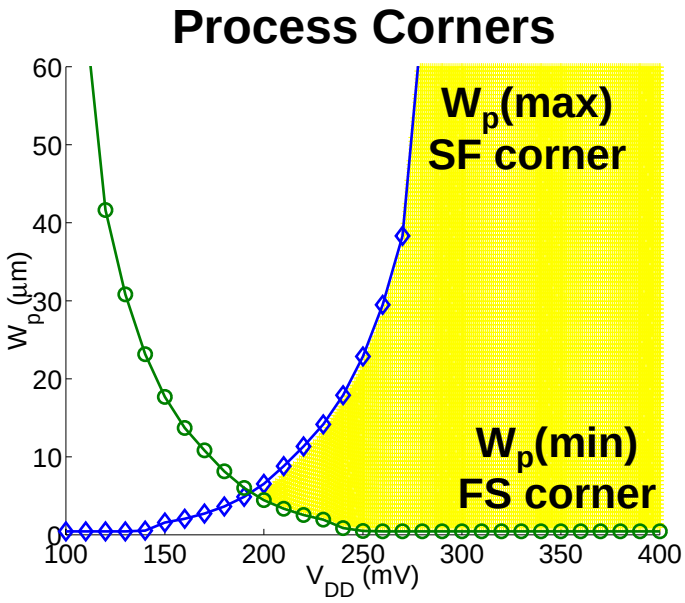
Optimum Power Supply

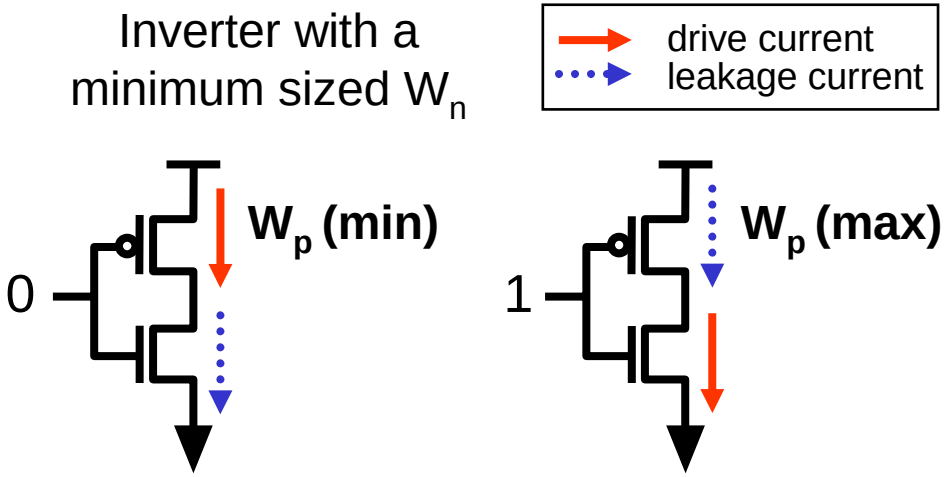


- There is a trade-off between leakage and switching energy as frequency, V_{DD} and activity factor is varied.
- The FFT design focuses on achieving supply voltages well below 400mV to investigate the minimum energy point.

Min-Max Sizing Curve

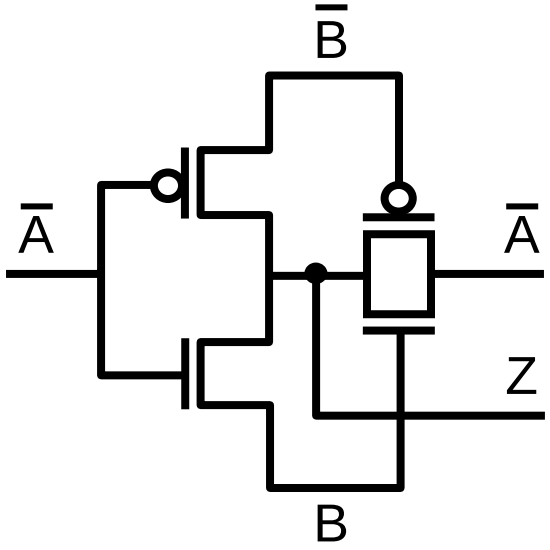


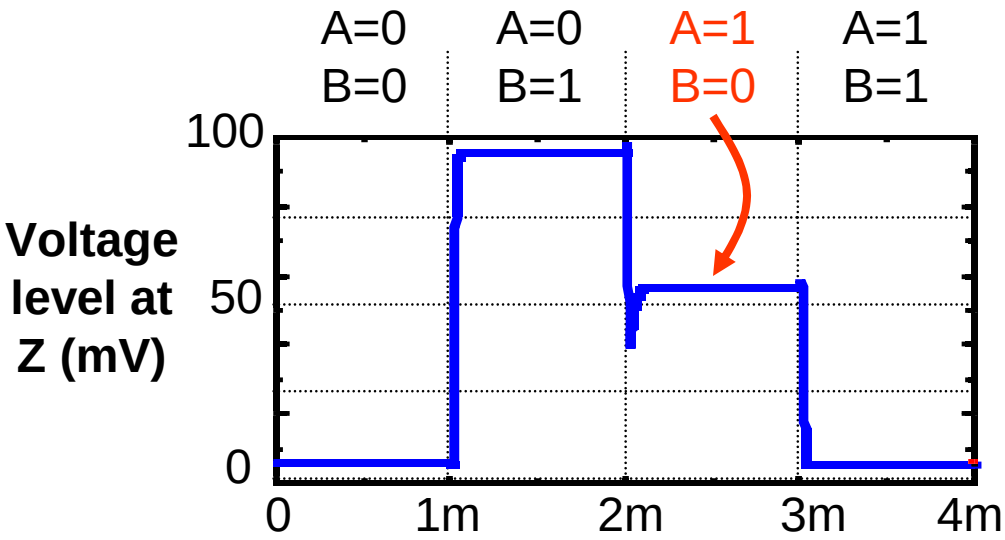


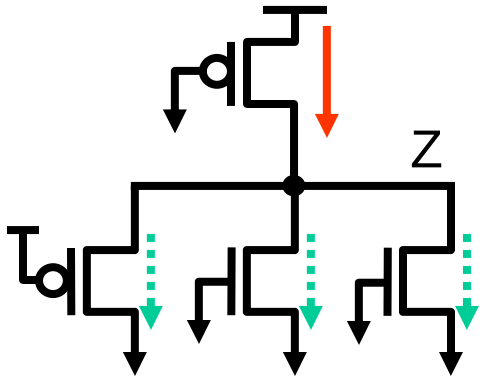


- The minimum supply voltage is limited by the effect of process variations.
- Inverter sizing analysis and minimum supply voltage analysis are performed at the corners.

Tiny XOR at 100mV







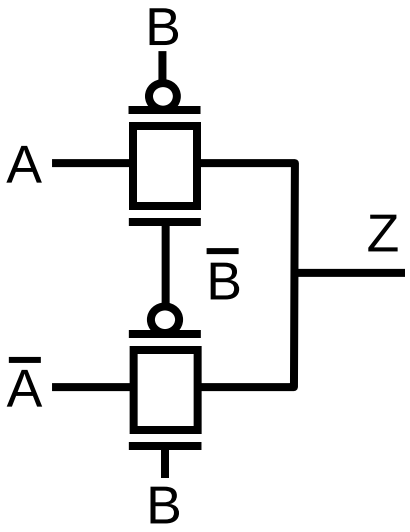
A=1, B=0, Z=1

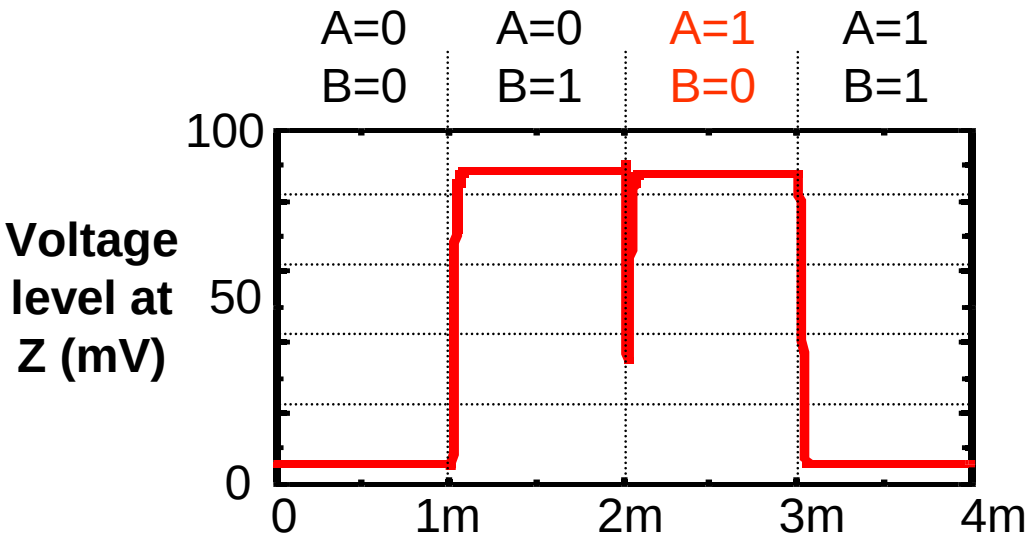
idle current

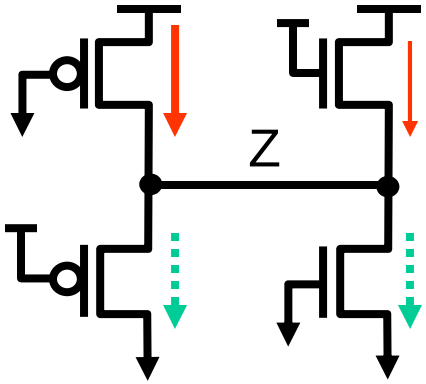
drive current

- Leakage through the parallel devices causes the tiny XOR to fail at 100mV.

Transmission Gate XOR







A=1, B=0, Z=1

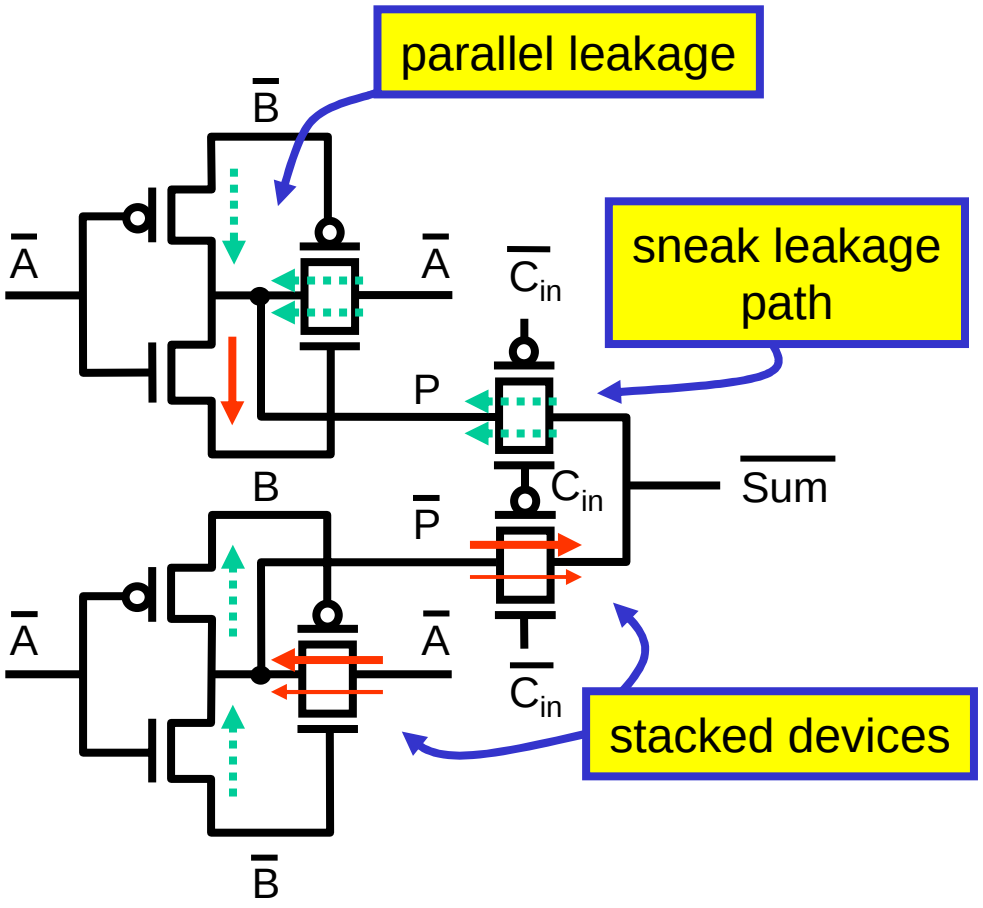
idle current

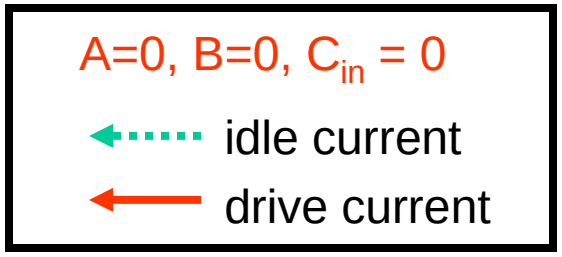
drive current

weak drive current

- Balanced number of devices reduces the effects of leakage and process variations.

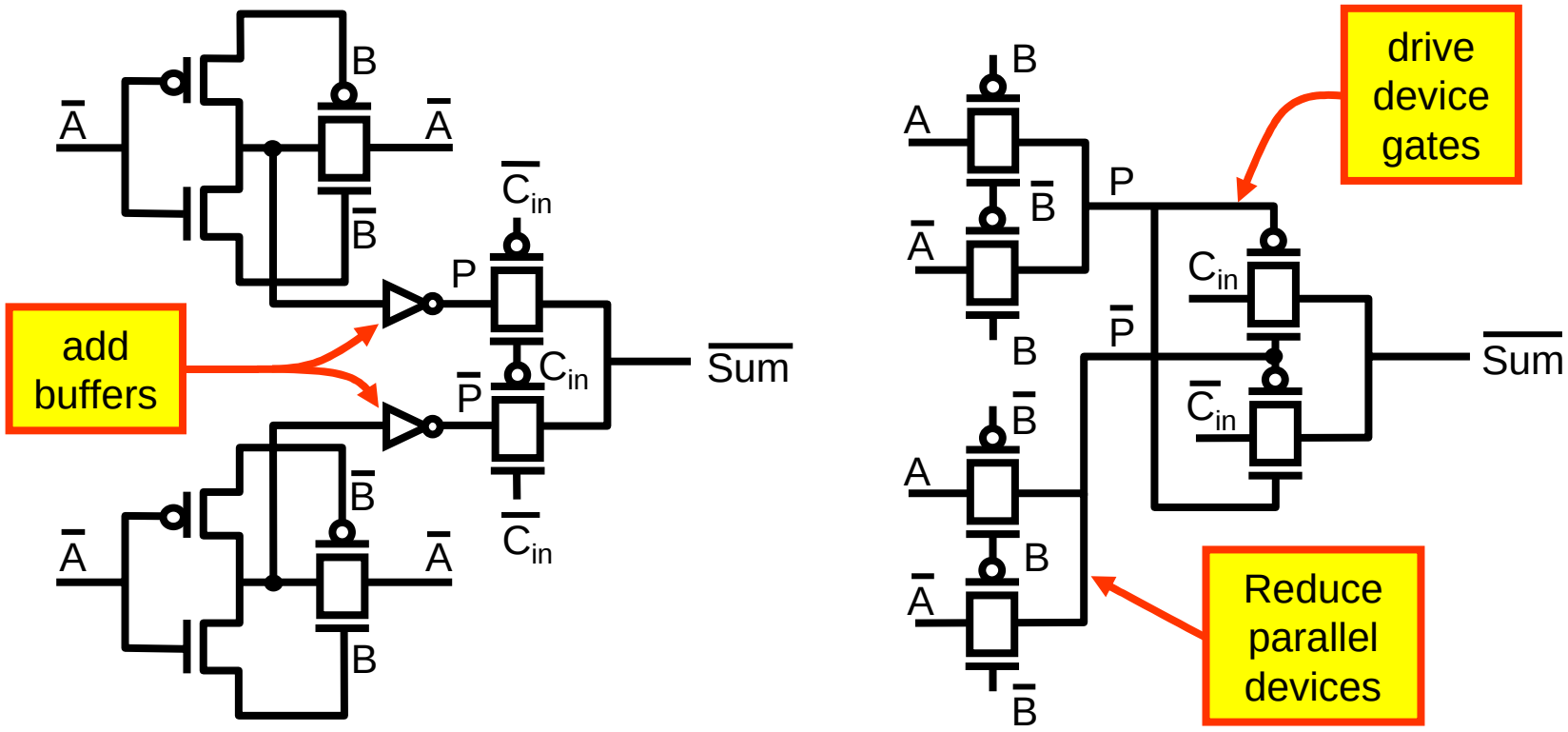
Sneak Leakage and Stacked Devices





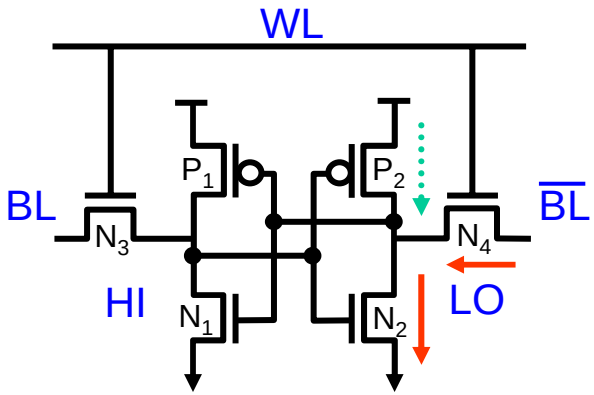
- Traditional circuits suffer from effects such as parallel leakage, stacked devices, and sneak leakage paths.

Subthreshold Library Methodology



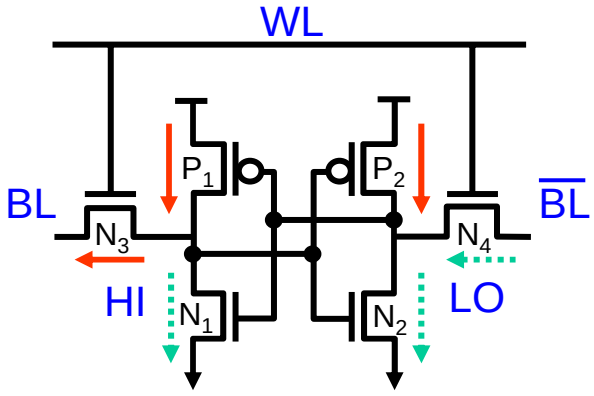
- Buffering, reducing parallel devices, and driving device gates are methods used in subthreshold standard cell logic design.

Sizing Tradeoffs - SRAM cell



WL=1
BL=1
$\overline{BL}$=1
HI=1
LO=0→ΔV_{LO}

Increasing W_{N2} prevents the memory cell from being rewritten during a read access.

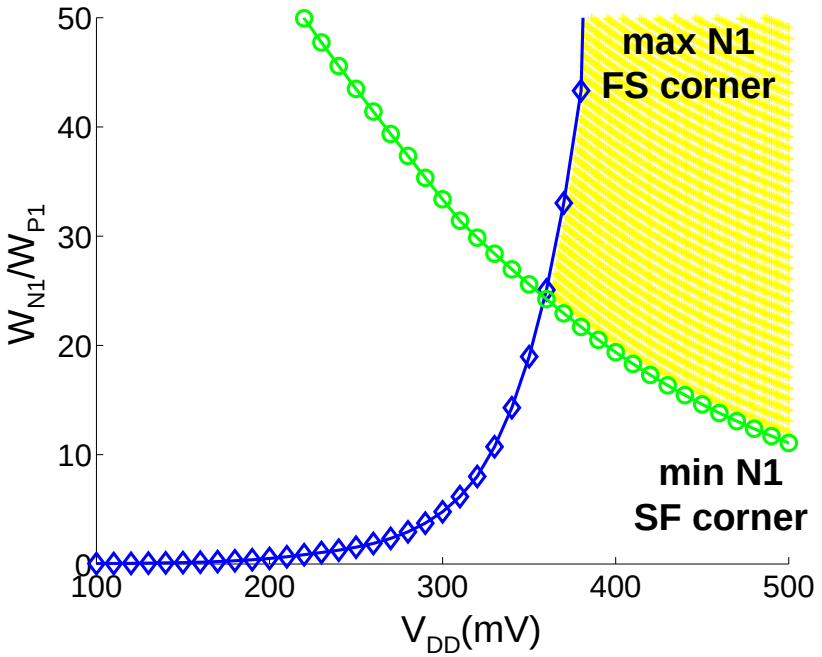


WL=1
BL=0
$\overline{BL}$=1
HI =1→ΔV_{HI}
LO=0→ΔV_{LO}

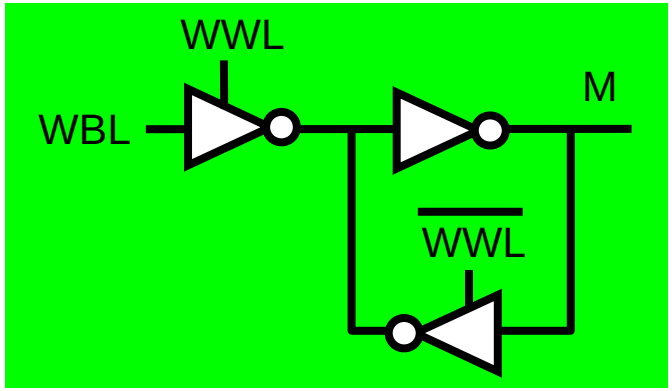
Write condition trade-off

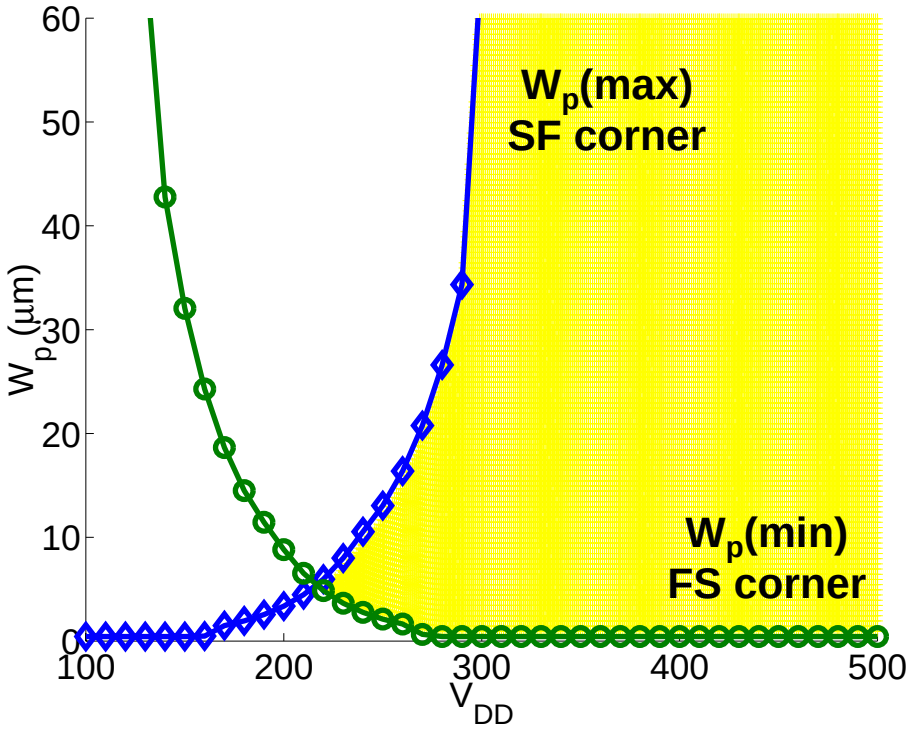
W_{N3}/W_{P1} large: write '0' into HI at the SF corner

W_{N2}/W_{P2} small: write '1' into LO at the FS corner



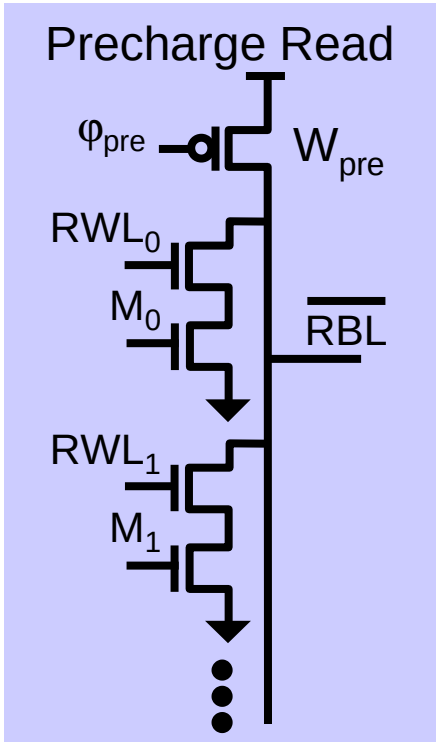
Tristate Write Access





- Tristate latch-based write access achieves low voltage operation at process corners.

Read Bitline at 100mV



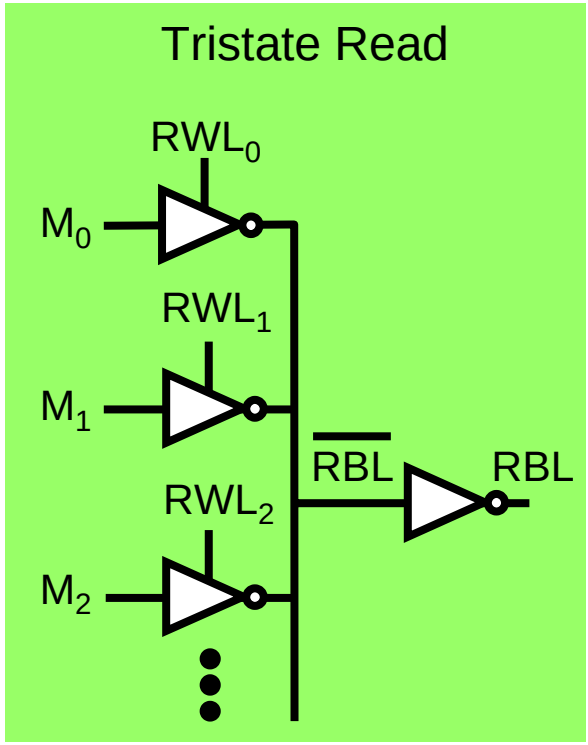
Data dependent leakage

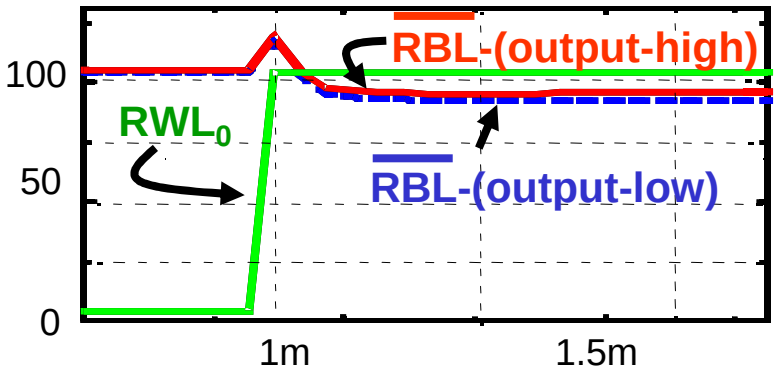
Worst case output-high:

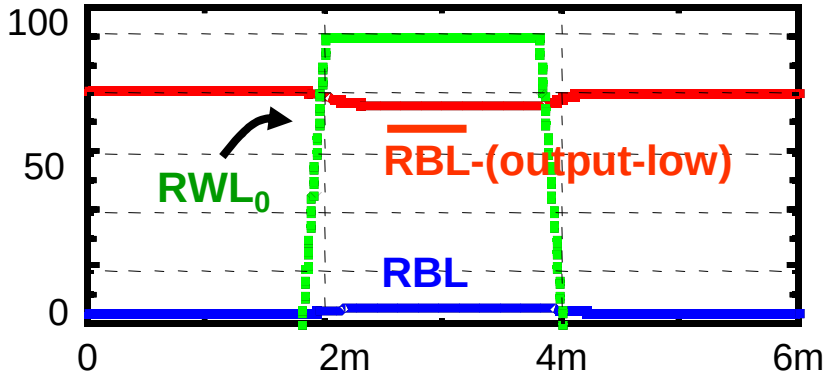
M_0=0, M_1-M_{127}=1

Worst case output-low:

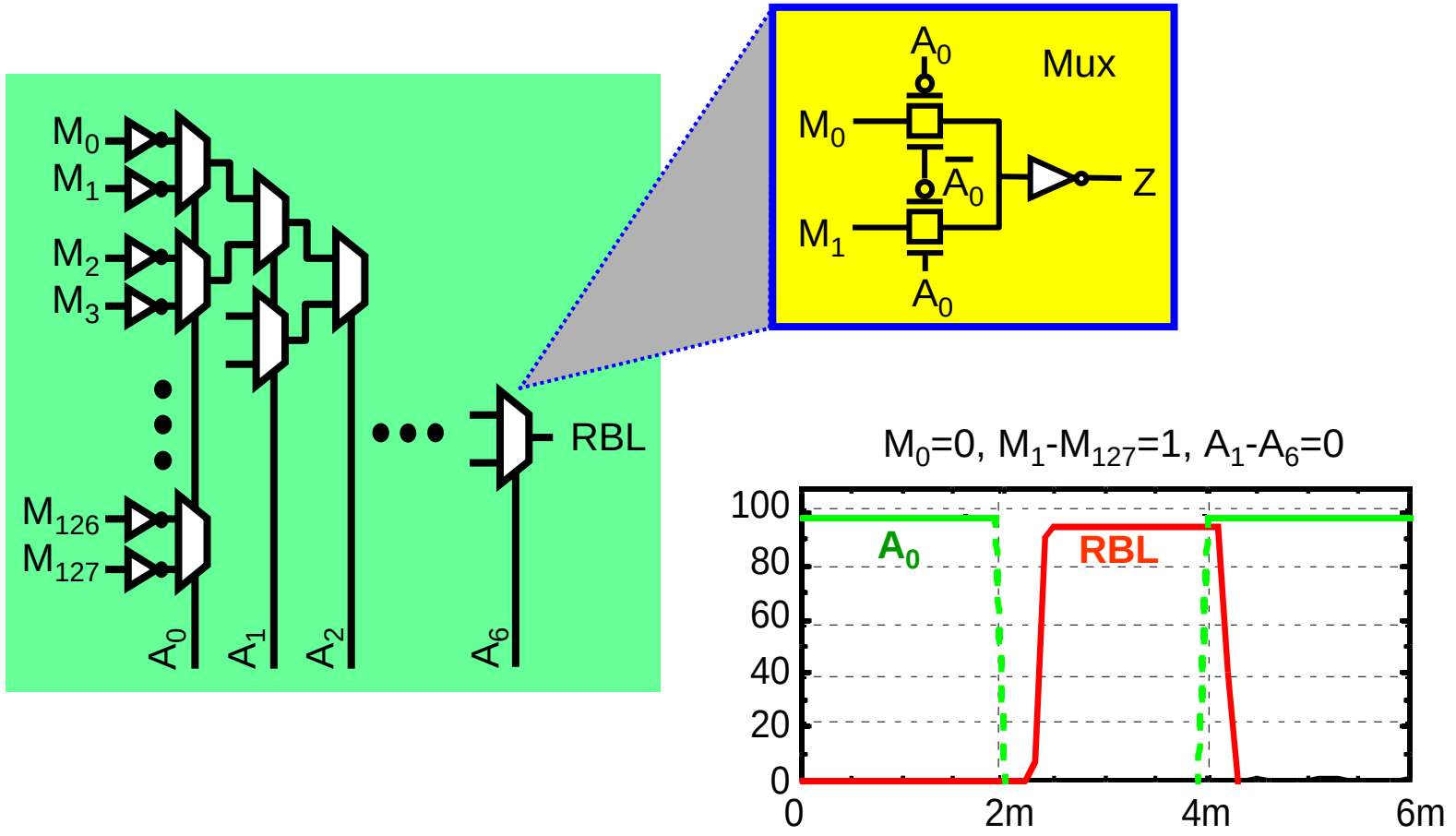
M_0=1, M_1-M_{127}=0





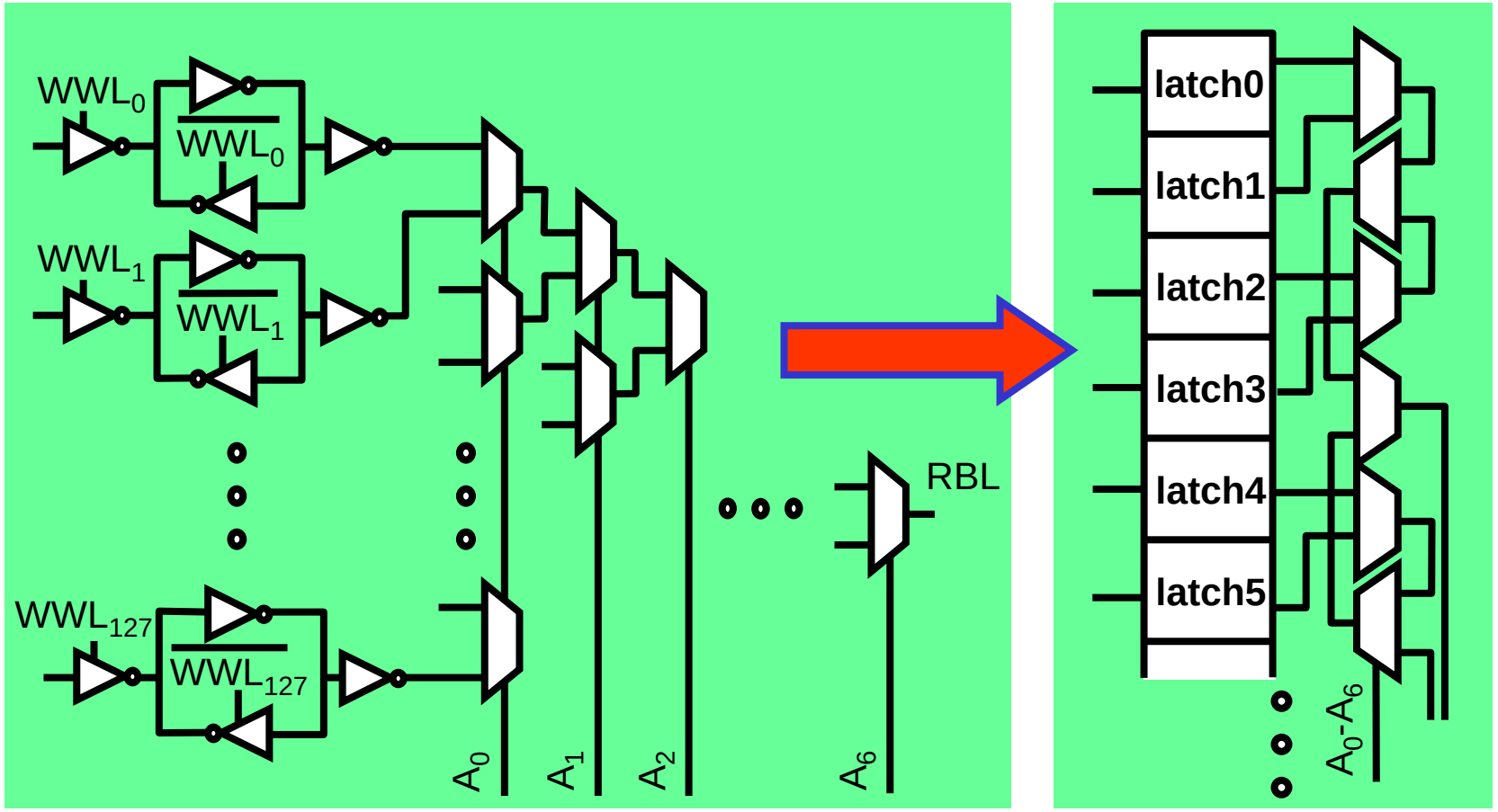


Hierarchical-Read Bitline



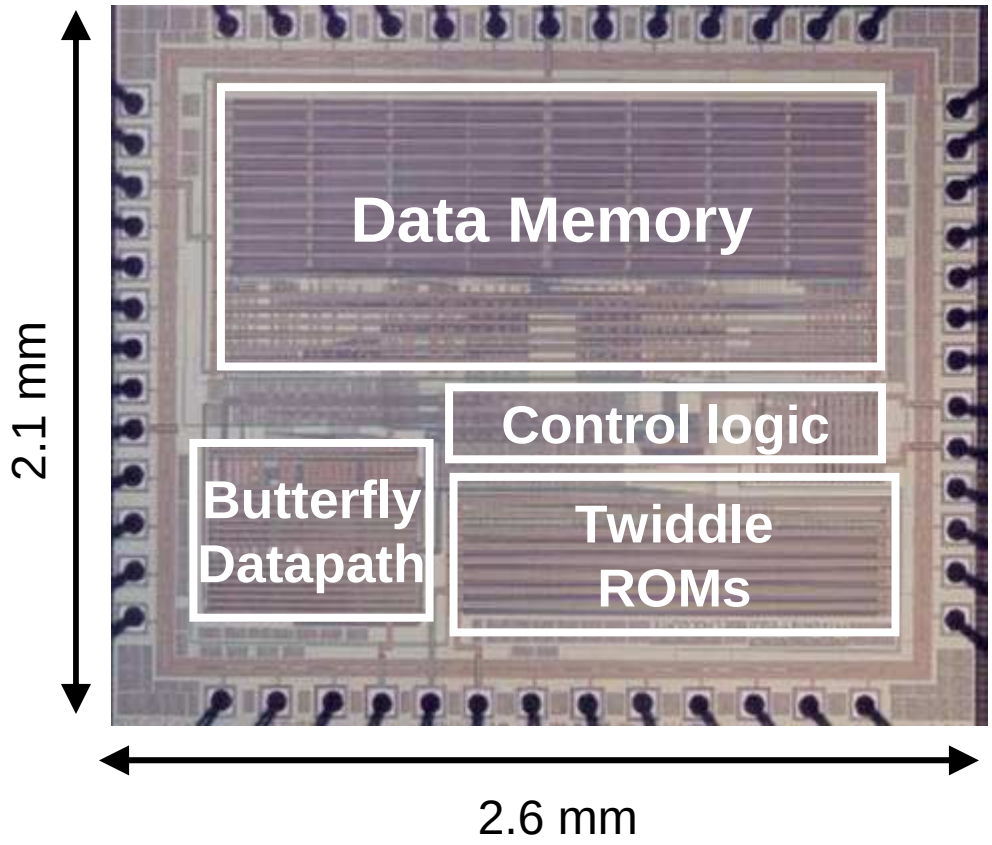
- The hierarchical-read bitline eliminates parallel leakage and stacked devices.

Latch-Write and Hierarchical-Read Memory



- Muxes are daisy-chained for compact layout area.

Custom Subthreshold FFT



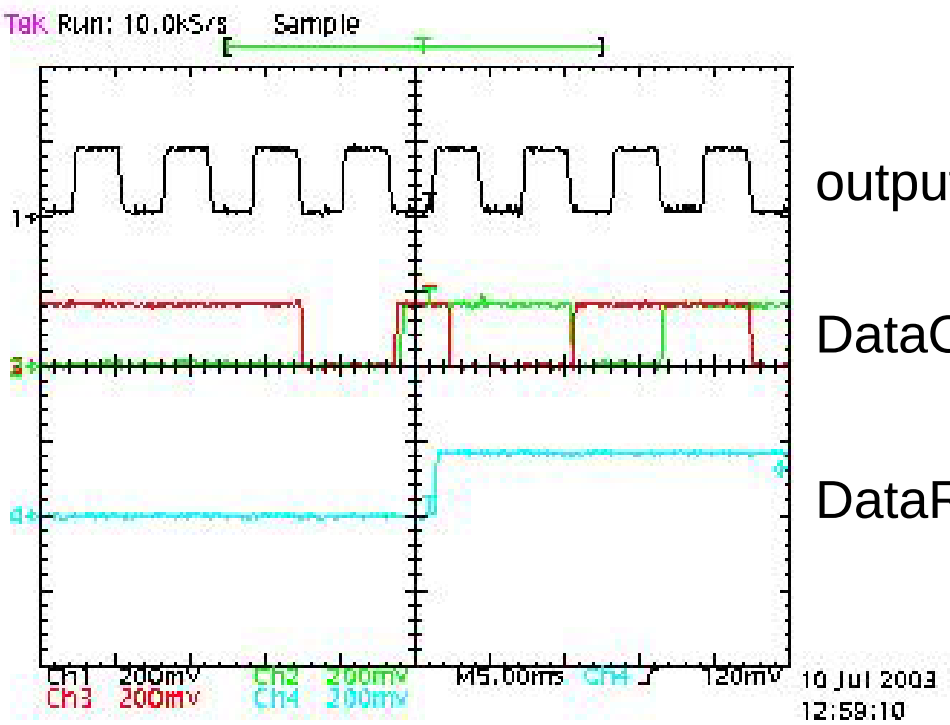
Process Details

- 0.18µm CMOS process
- 6 layer metal
- 628k transistors

Design Flow

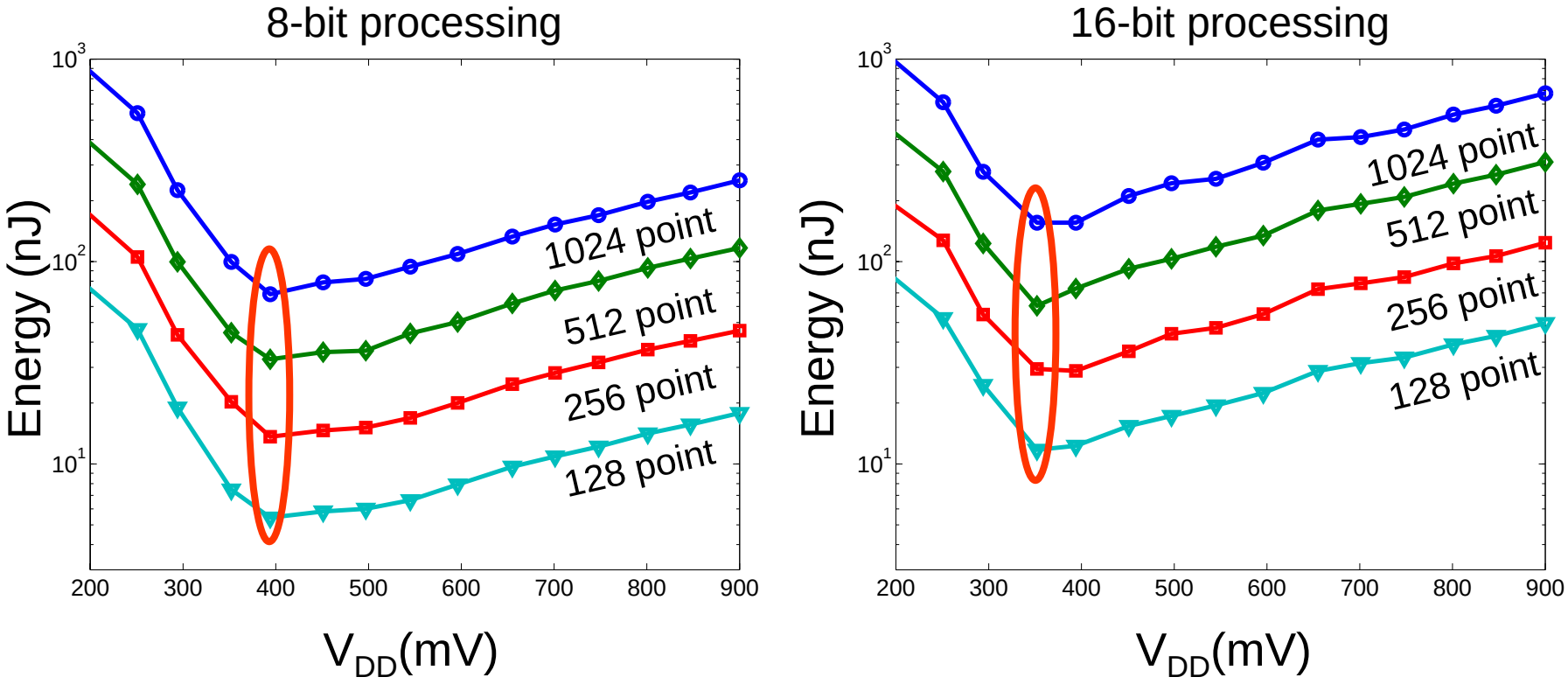
- Custom subthreshold logic cells
- Custom Skill-based memory generators and multipliers
- Skill code place-and-route

180 mV Supply Demonstration



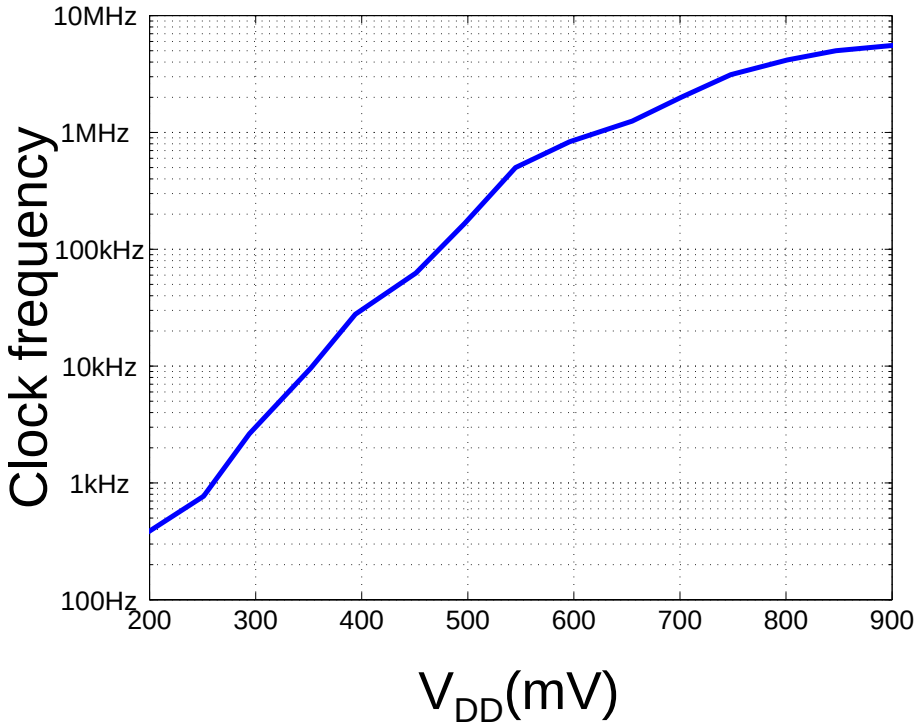
- The FFT processor achieves 180mV operation for 16-bit, 1024-point operation. The clock frequency is 164 Hz.

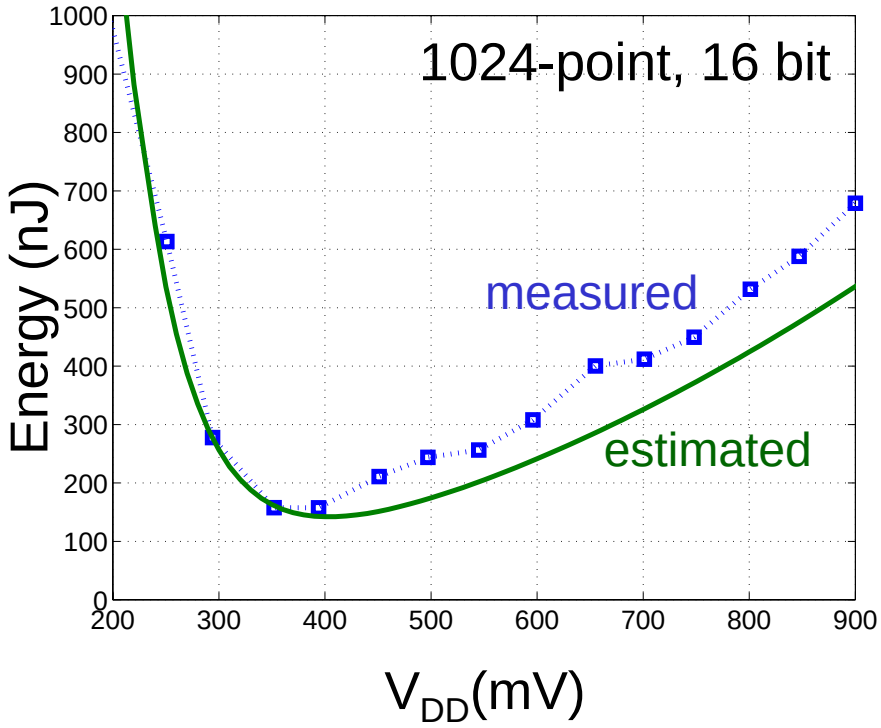
Energy-Scalability Measurements



- The FFT is able to operate at 128, 256, 512 and 1024-point FFT lengths and 8 and 16b precisions.
- 8b processing leads operation at a larger minimum V_{DD} due to reduced activity factor.

Energy Estimation





- The FFT operates between V_{DD}=180mV-900mV and clock frequency of 164Hz-6MHz.
- The minimum energy dissipated is 155nJ/FFT at 350 mV for a 1024-point 16b FFT. The clock frequency is 10kHz and the FFT processor dissipates 0.6µW.

Conclusions

- Subthreshold operation at the optimal supply voltage and clock frequency is necessary to minimize energy dissipation of digital circuits in wireless sensor applications.
- Process variations limit the minimum supply voltage operation of CMOS circuits.
- Subthreshold logic and memory design methodology minimizes parallel leakage, stacked devices and sneak leakage effects.
- Demonstrated a 180mV FFT Processor using subthreshold circuit techniques.