



Power Aware Wireless Microsensor Systems

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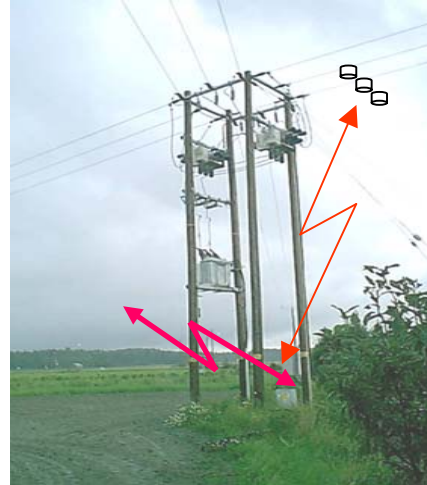




Emerging Microsensor Applications



Industrial Plants and Power Line Monitoring (courtesy ABB)



Operating Room of the Future (courtesy John Guttag)



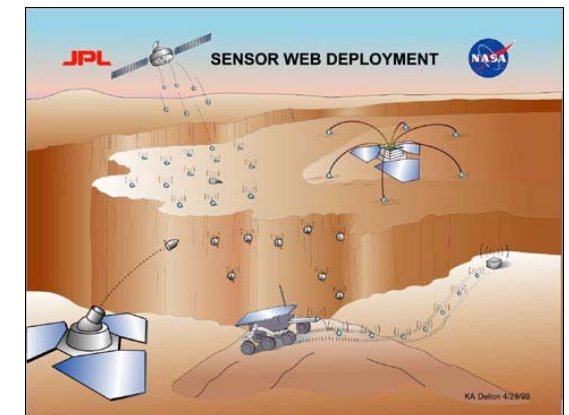
Target Tracking & Detection (Courtesy of ARL)



Location Awareness (Courtesy of Mark Smith, HP)



NASA/JPL sensorwebs





Sensor System Requirements



Predictable Constraints

Application Characteristics	Typical Values
Data Rate	bps to kbps
Spatial Density	0.1-10 nodes/m ²
Transmission Distance	10 – 100m
Extended Lifetime	5 years
Small Size	1 “AA” battery

Unpredictable Diversity

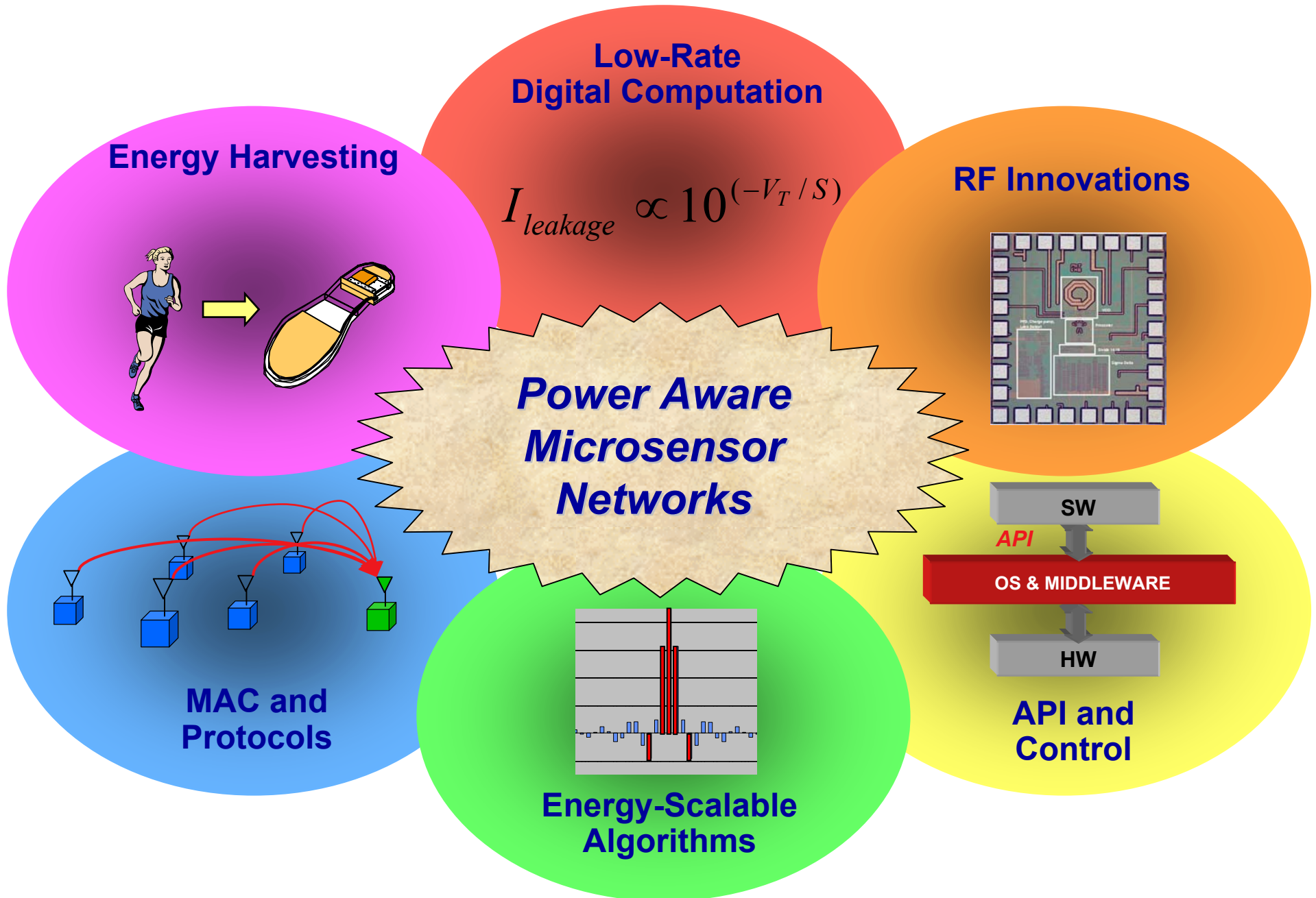
- *Network roles:*
relay, sensor, aggregator
- *Environment:*
event and signal statistics
- *User/Application:*
required latency, quality

Application-specific designs provide energy efficient point solutions

Power-aware designs adapt energy consumption to operating conditions

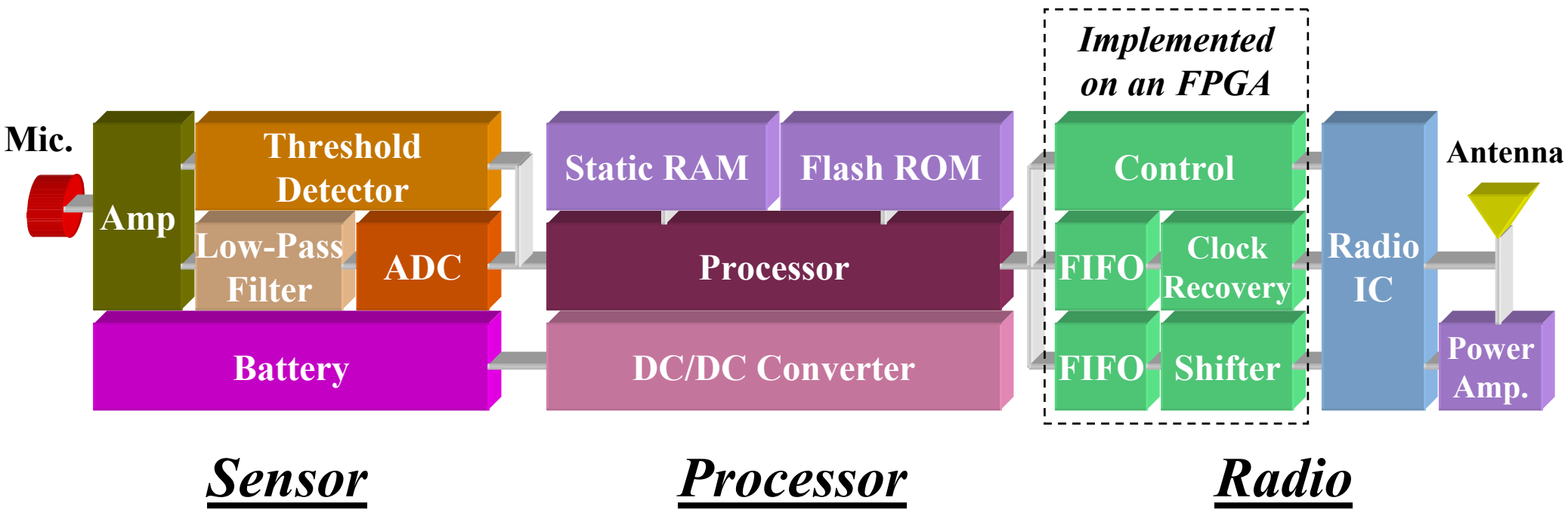


Power Aware Microsensor Considerations





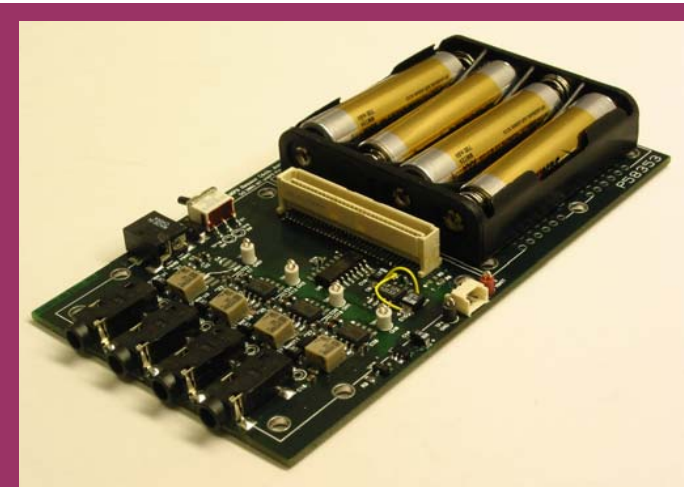
First Generation Wireless Microsensor



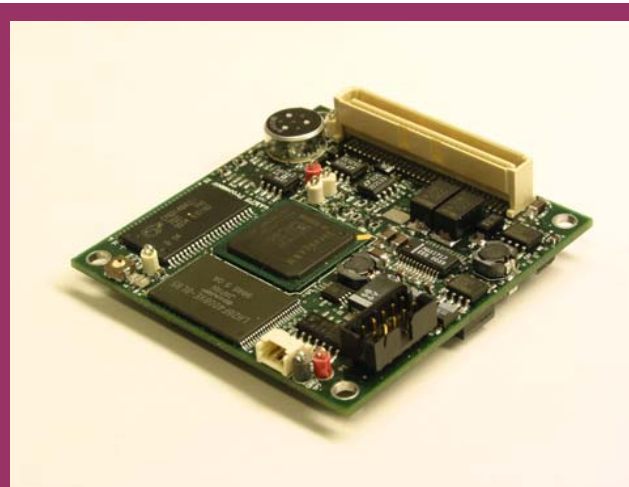
Sensor

Processor

Radio



4-channel acoustic



206MHz StrongARM



2.4GHz ISM band



OS-Controlled Power Down Modes

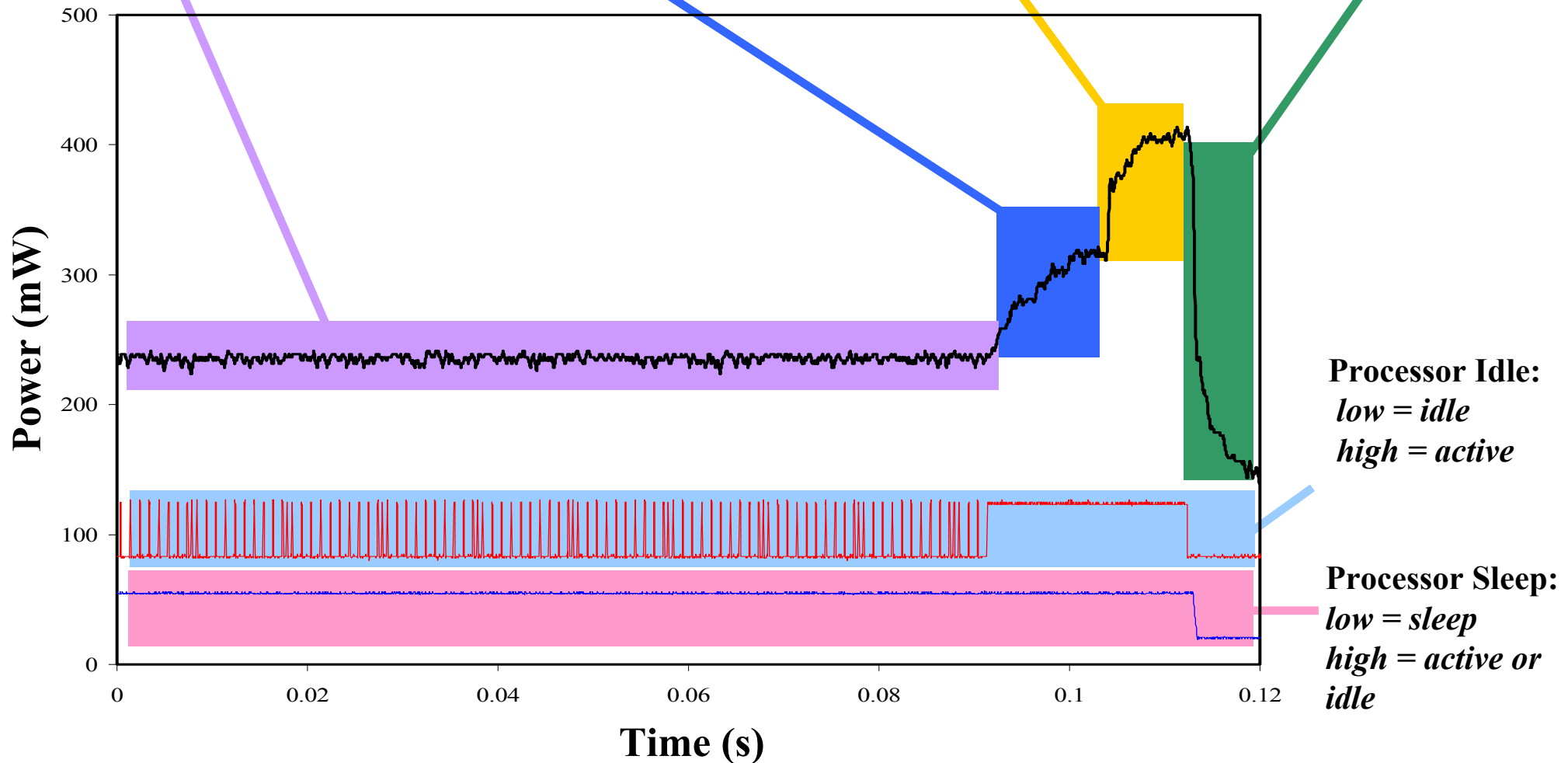


Data collection: 1024 samples at 1kSPS
(Processor alternates between idle/active)

LOB Calculation
(Processor active full-time)

Data transmission
(Radio transmitter active)

Sleep
(All systems power down)

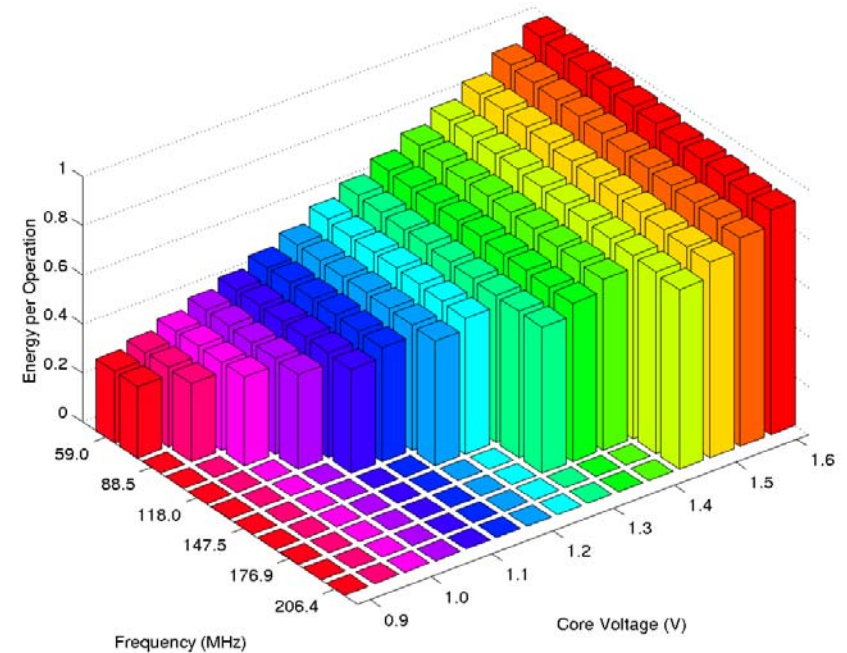
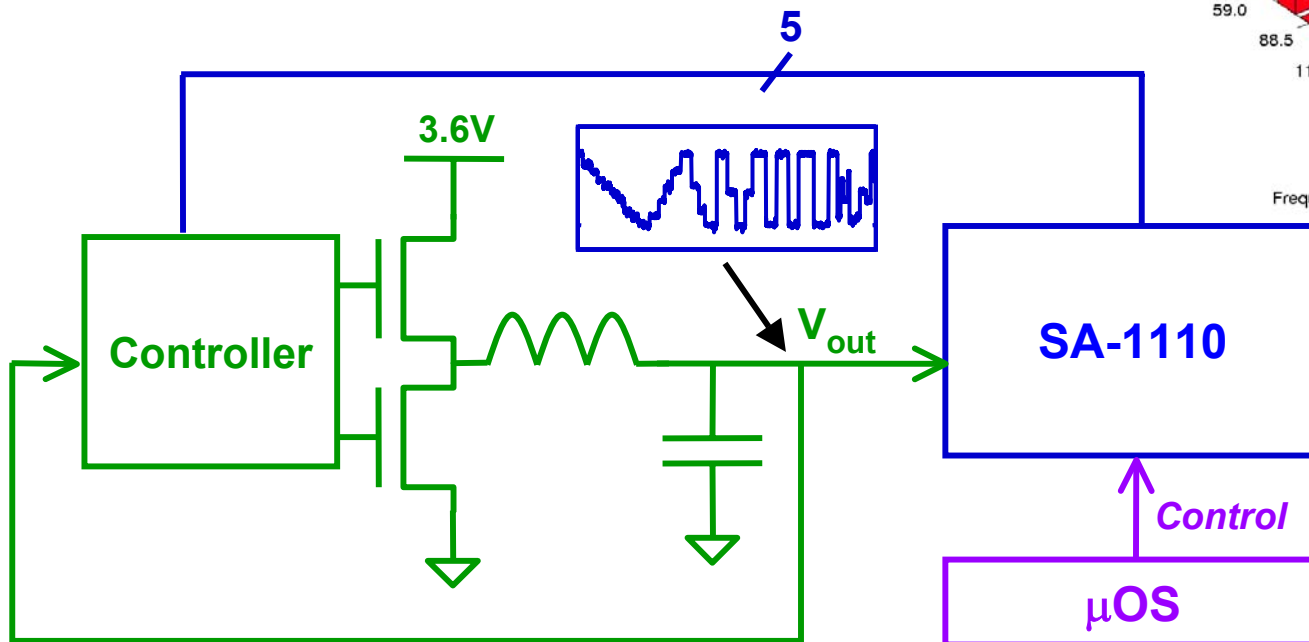




Dynamic Voltage Scaling



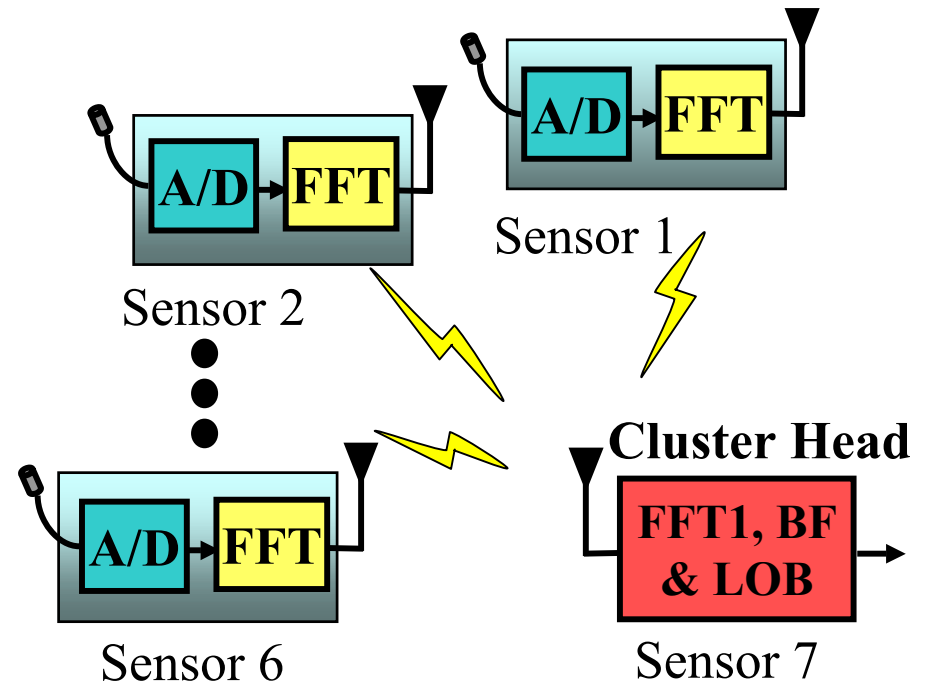
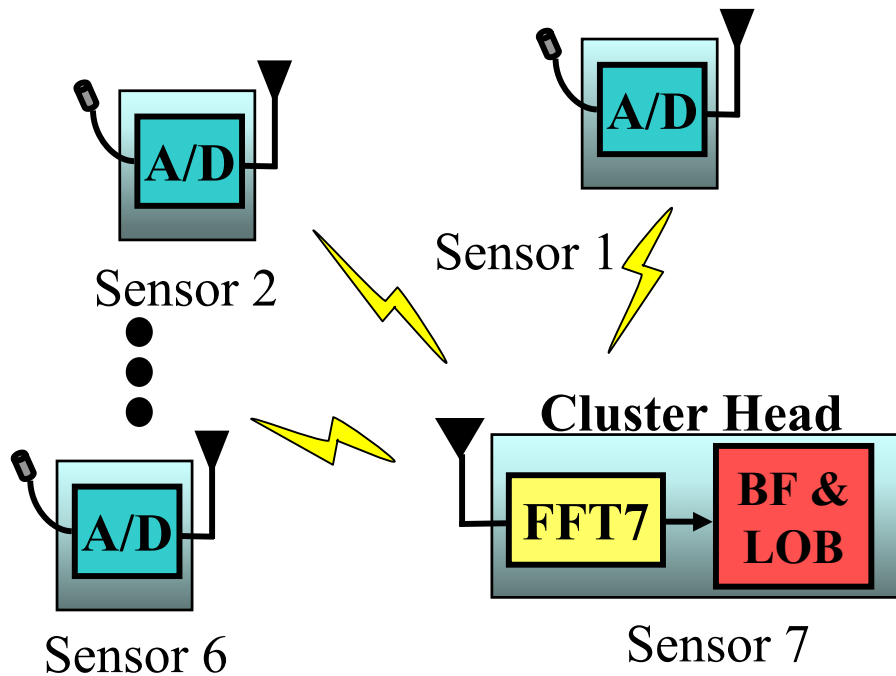
Digitally adjustable DC-DC converter powers SA-1110 core



μOS selects appropriate clock frequency based on workload and latency constraints



Distributed Processing Exploiting DVS



Approach 1: All latency-critical computation at aggregating node

$$E_{\text{comp}}(V_{\text{dd}}=1.5\text{V}) = 7E_{\text{fft}} + E_{\text{bf}} + E_{\text{LOB}}$$

$$= \mathbf{27.27 \text{ mJ}} \text{ on SA-1100}$$

Approach 2: Distributed processing ameliorates latency-critical computation

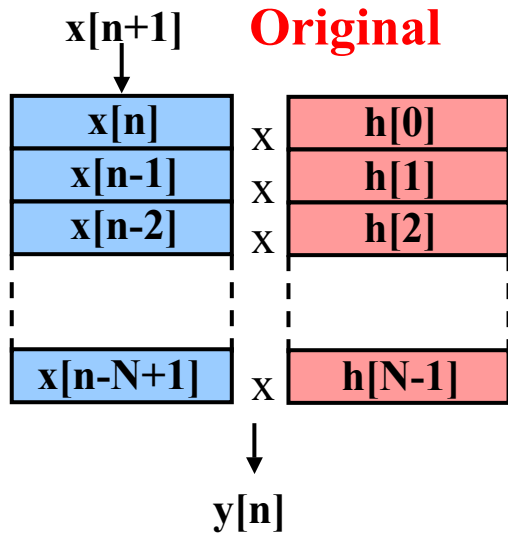
$$\text{FFT: } V_{\text{dd}} = 0.9 \text{ V}$$

$$\text{BF \& LOB: } V_{\text{dd}} = 1.3 \text{ V}$$

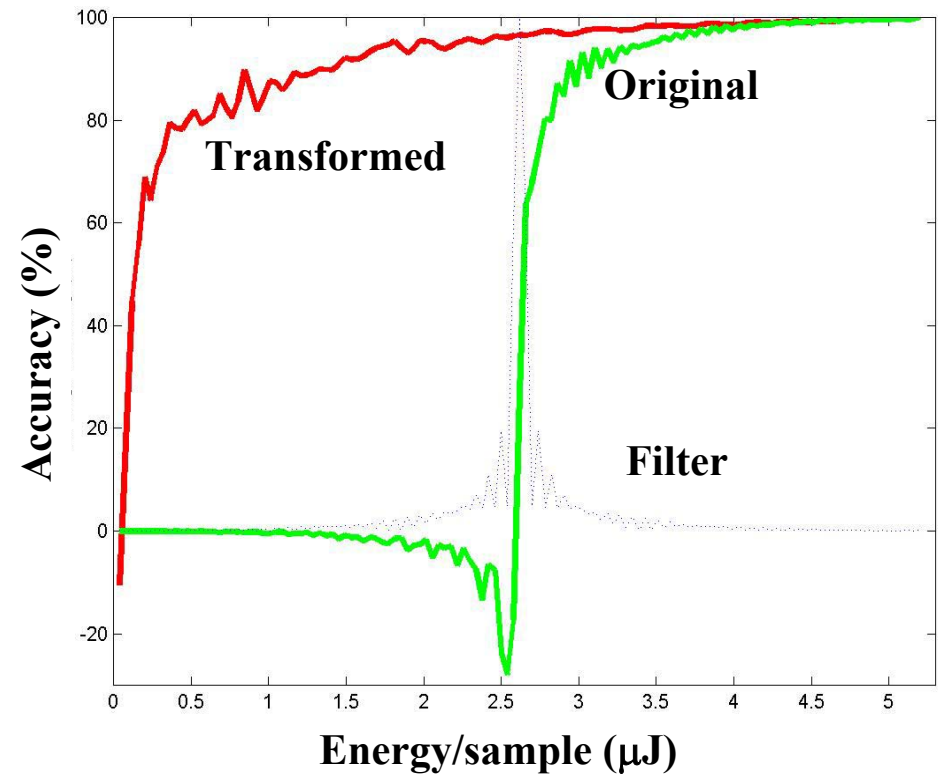
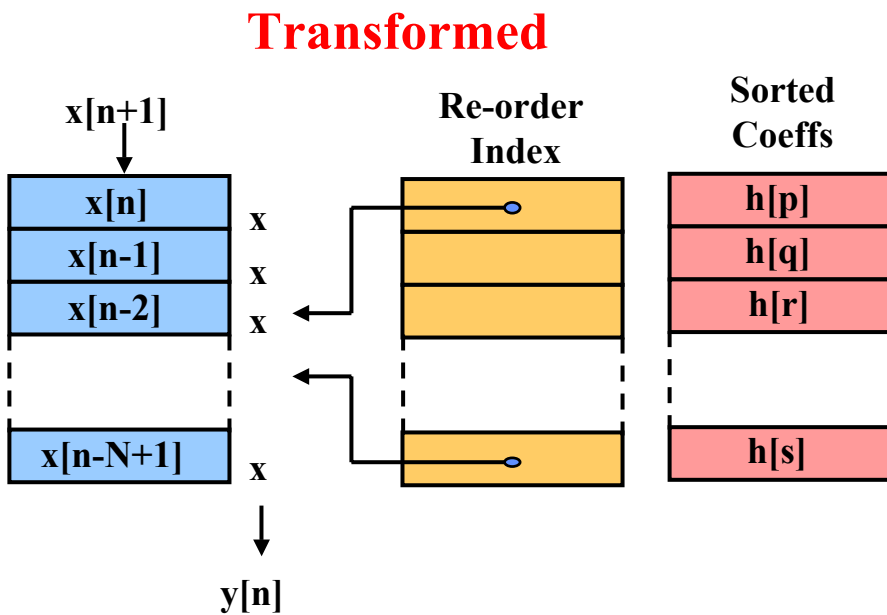
$$E_{\text{comp}}(\text{variable } V_{\text{dd}}) = \mathbf{15.16 \text{ mJ}}$$



Energy Scalable Algorithms



$$y[n] = \sum_{k=0}^{N-1} h[k]x[n-k]$$

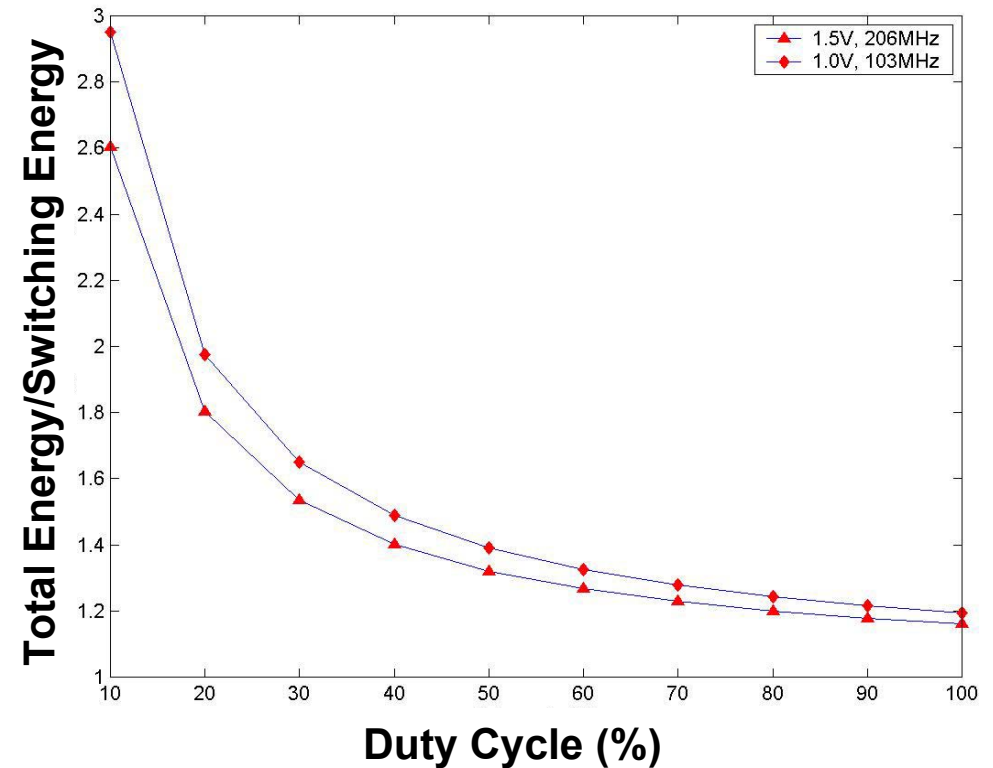
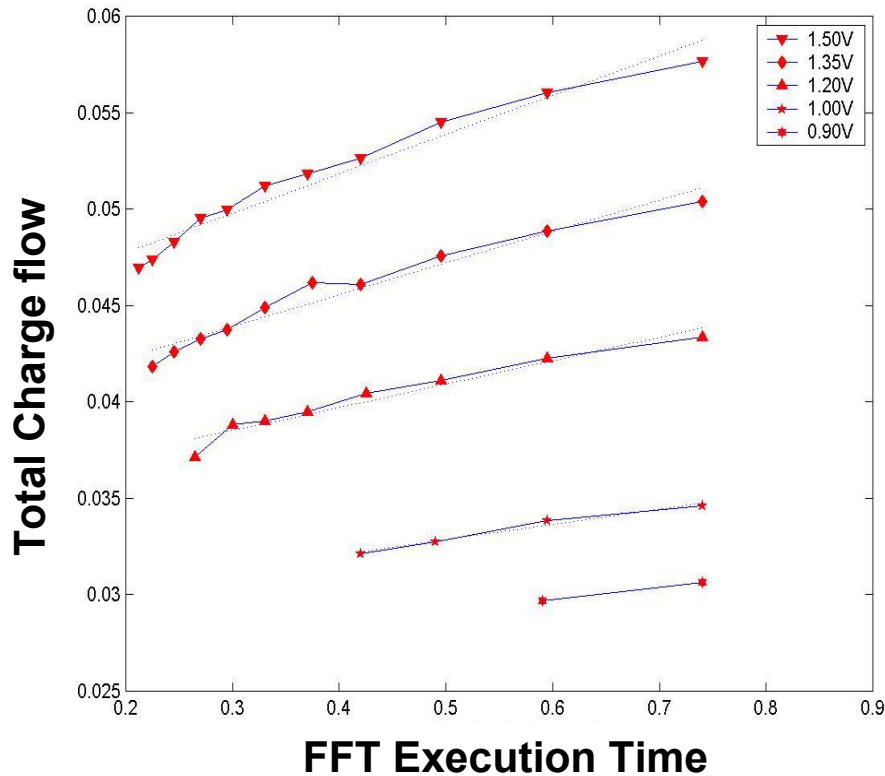


[Sinha, ISLPED '00]

- Maximize quality for a given energy availability



Leakage : Low Duty Cycle Concern

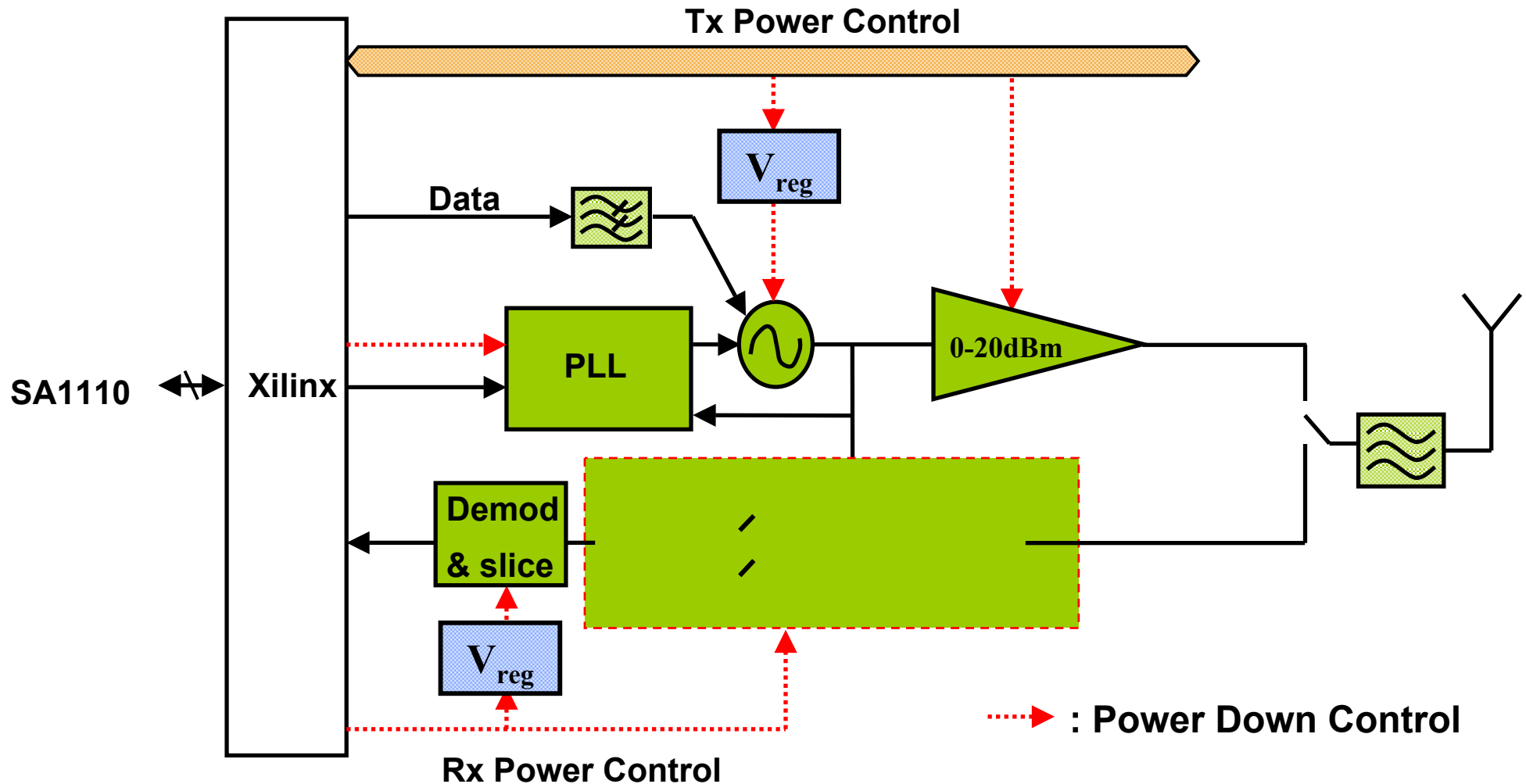


$$I_{leakage} \propto 10^{(-V_T / S)}$$

Leakage Dominates Switching Energy for Low Duty Cycles – “Off” State-centric Optimization



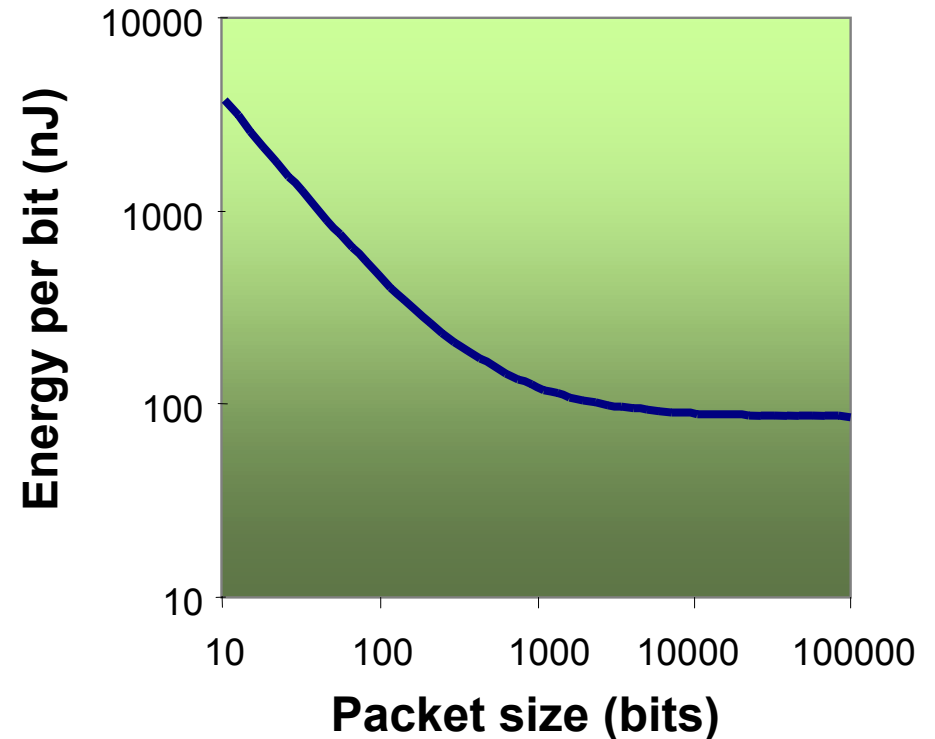
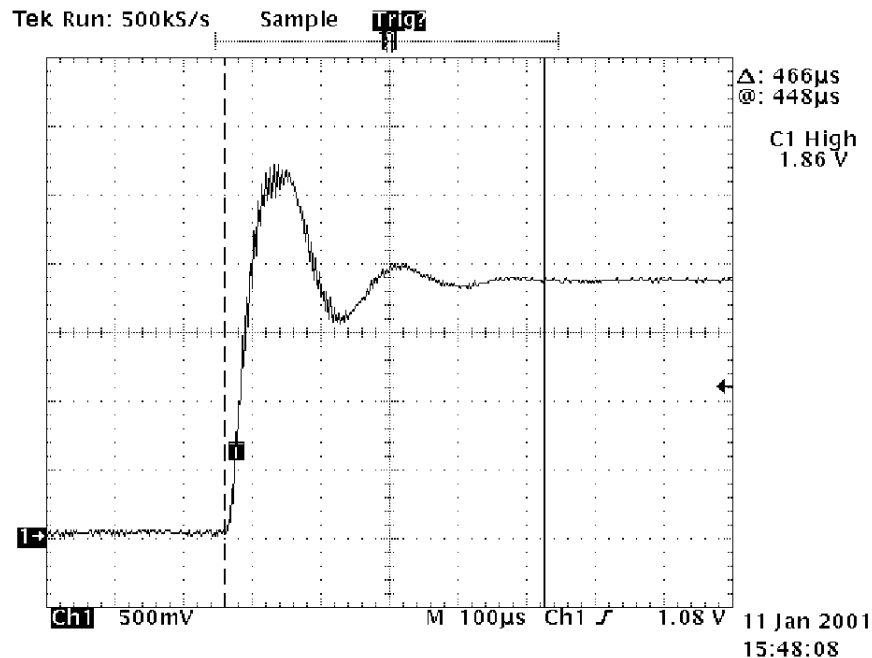
Power Aware Radio



- Fine-grain shutdown through regulators and bias control
- Variable 6-level PA allows efficient transmission for 10m to 100m



RF Start-up Energy Overhead



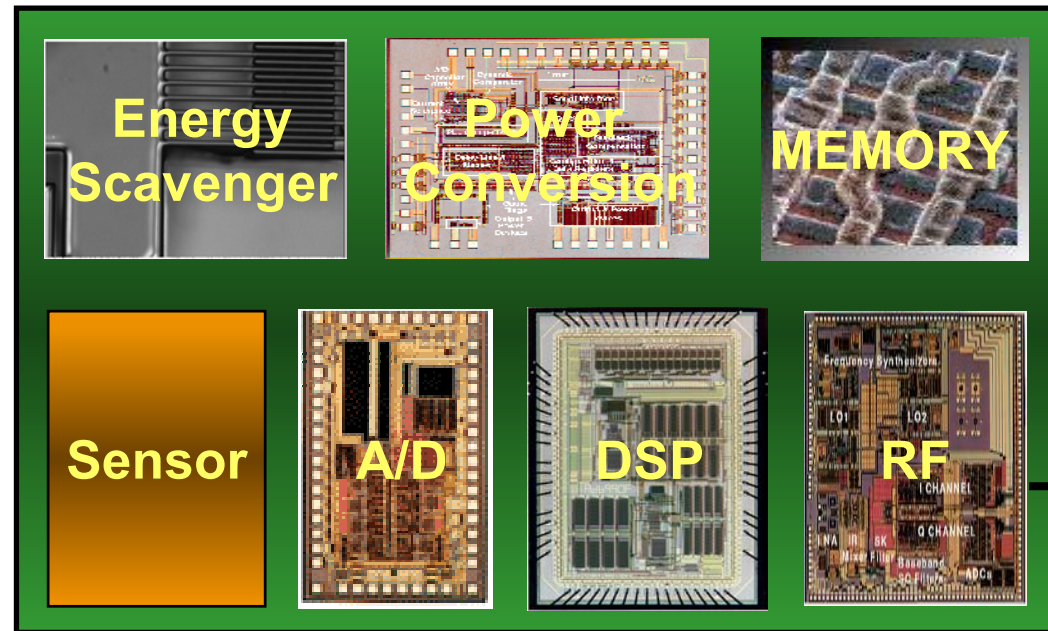
$$Energy = P_{tx_electronics} (T_{transmit} + T_{start}) + P_{out} T_{transmit}$$

- Significant loss in energy efficiency for small packet sizes

***Startup Costs are Fundamental –
Innovative Circuits and Protocols Required***



Integrated System-on-a-Chip Vision

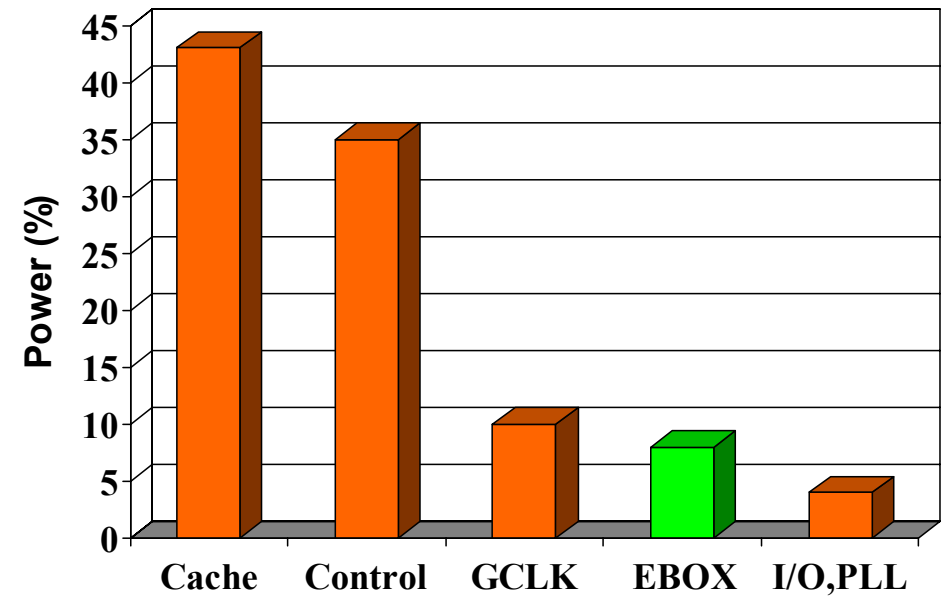
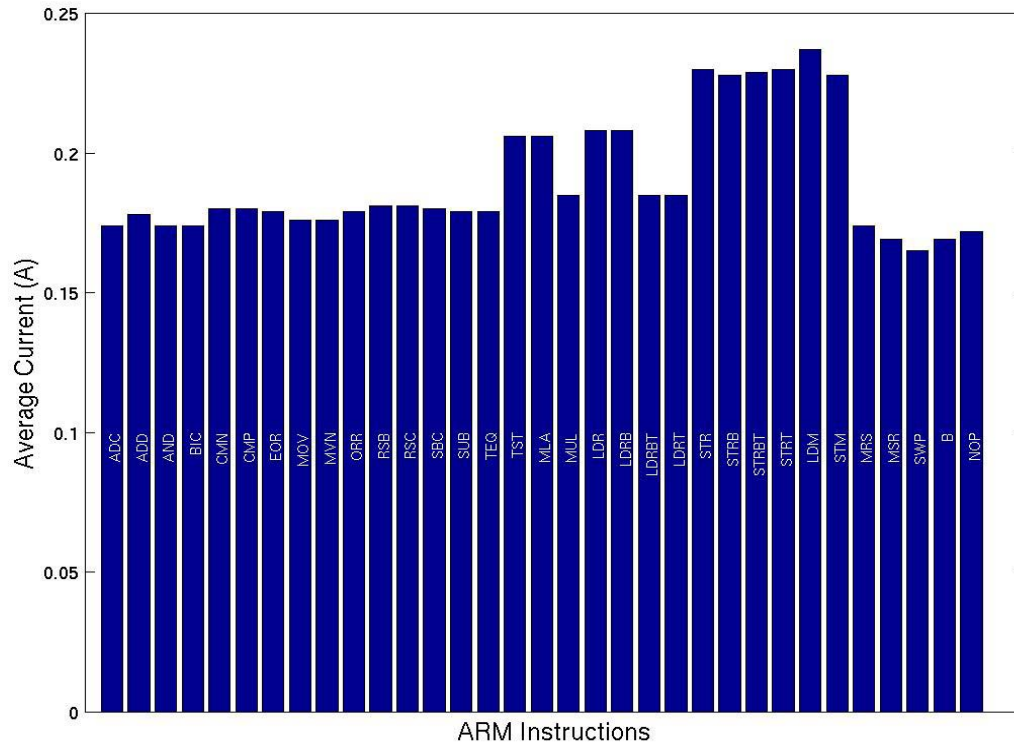


- Compact Form Factor ($\text{mm}^3 - \text{cm}^3$)
- Requires interconnection of **diverse process** technologies
- Low computational requirement, but **requires flexibility** to adapt to time-varying scenarios
- Cost, size and energy are the key design constraints

What is the best computation/communication fabric?



Why Not Software?

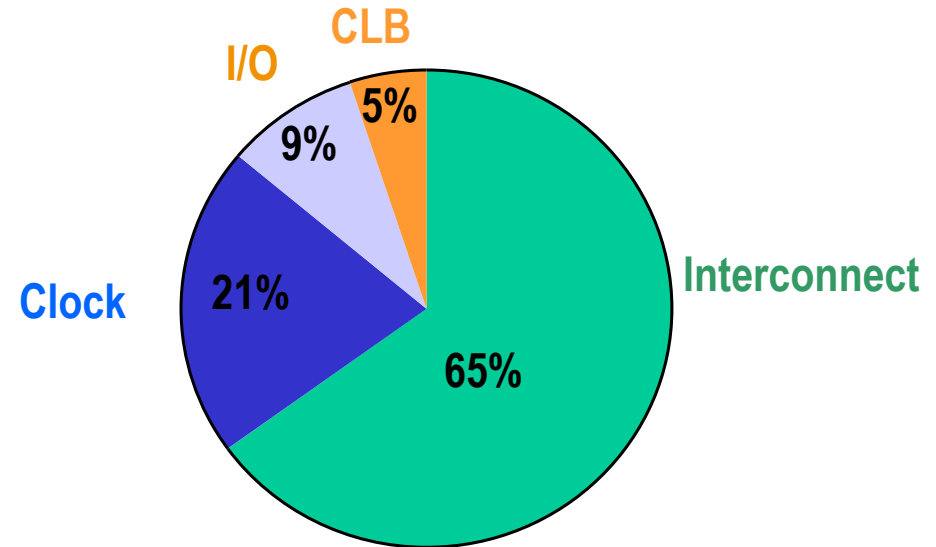
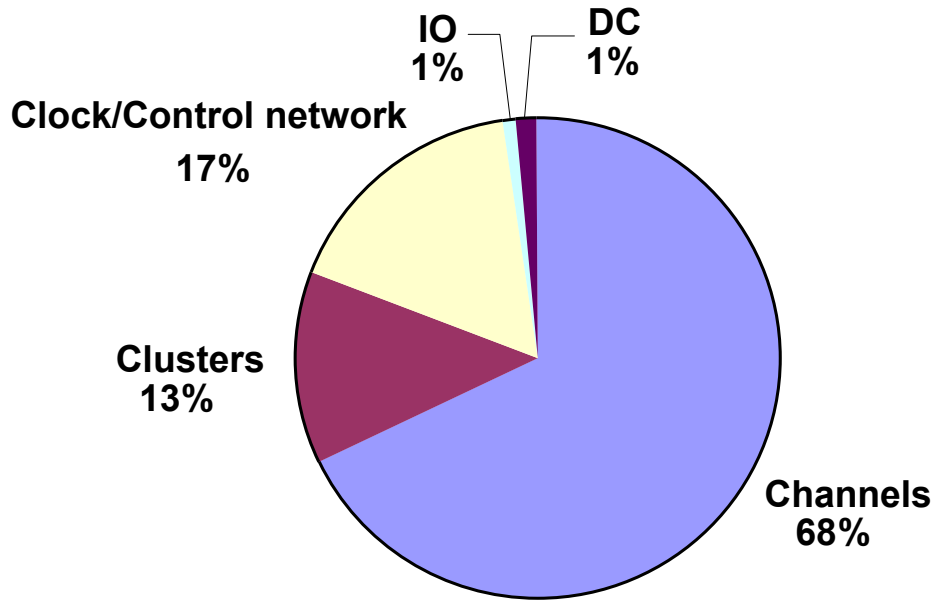
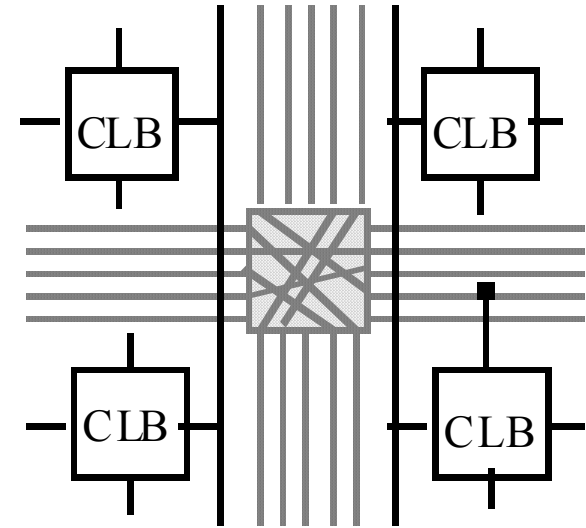
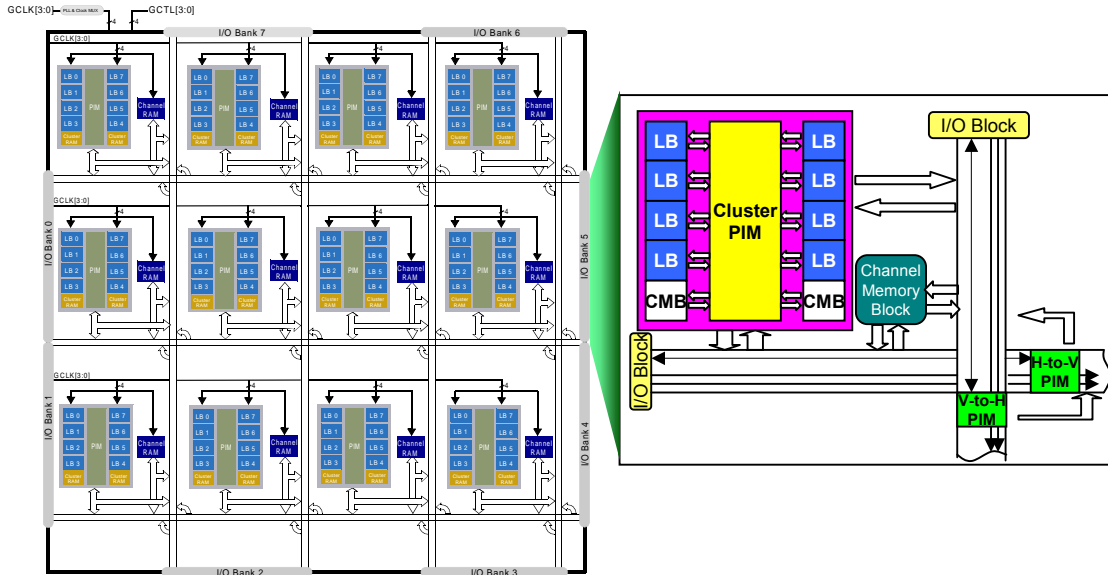


[Montanaro, JSSC '96]

Software Energy Dissipation is Dominated by Overhead and NOT by Useful Work



What about FPGAs?

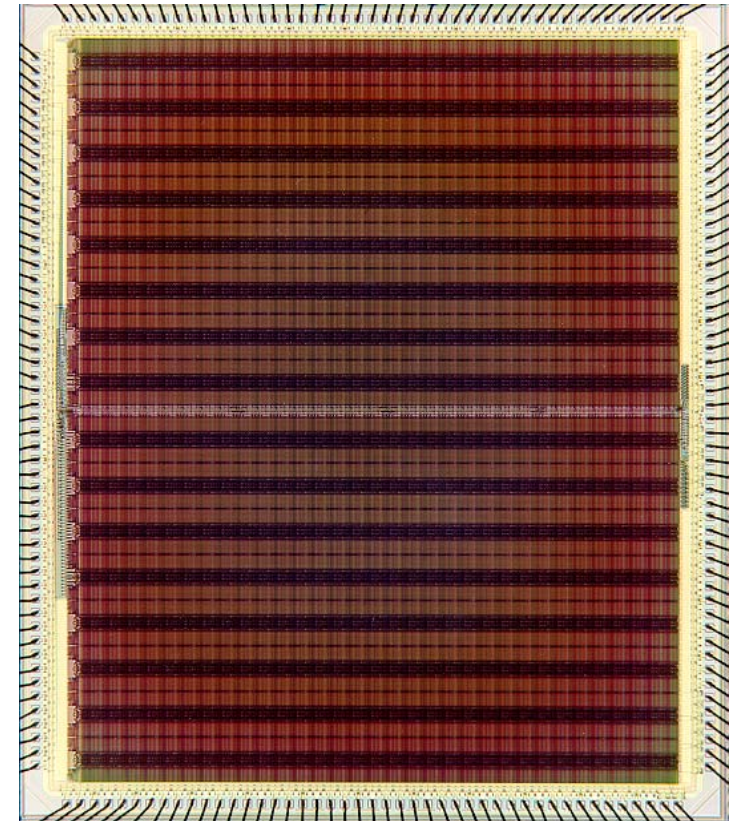
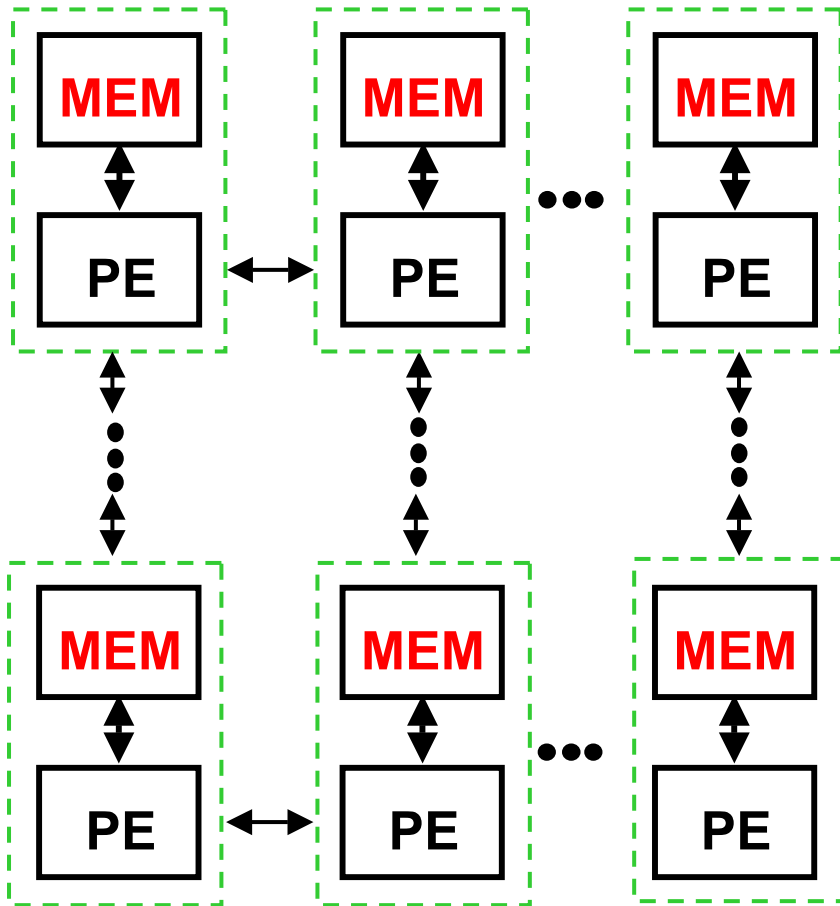


Cypress

Xilinx
(Courtesy of J. Rabaey)



Interconnect-Centric Architectures (Flexibility with Power Efficiency)



[Simon, JSSC '00]

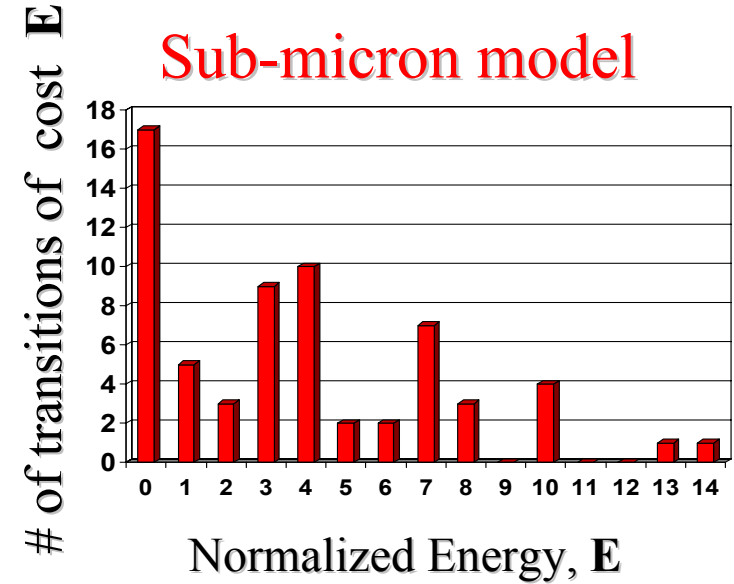
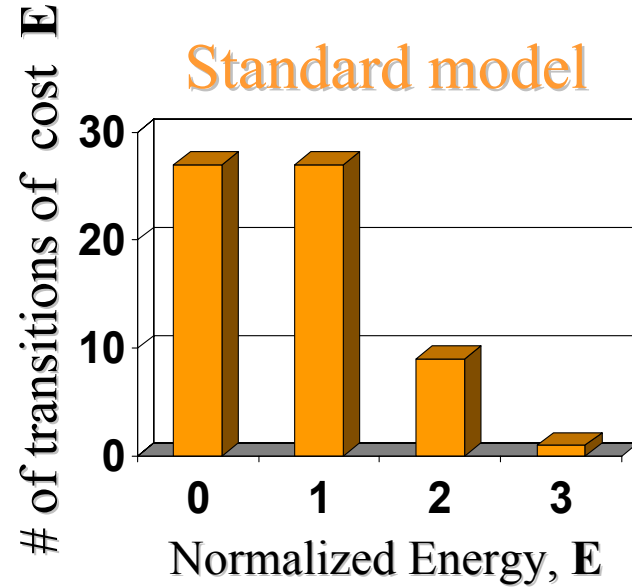
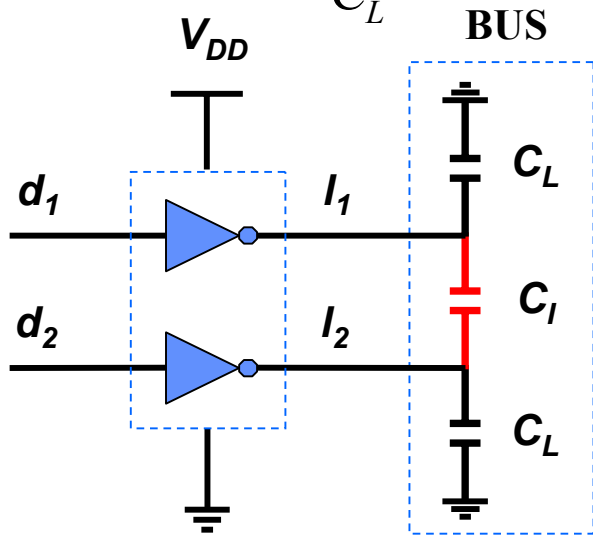
- Massively parallel, “slow” switching processors
- Exploits locality of reference, low interconnect costs
- Image Sensor Application: Wavelet based compression (3 Million Transistors, $0.6\mu\text{m}$ CMOS, $500\mu\text{W}$)



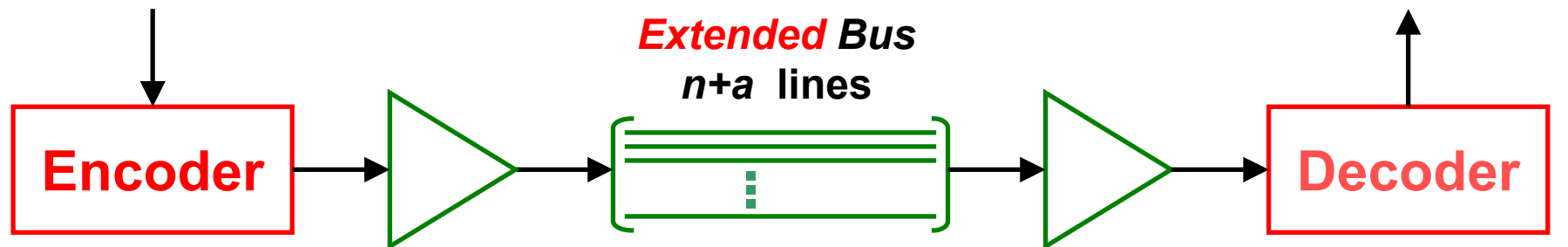
New Energy Metrics in DSM Interconnect



$$\lambda = \frac{C_I}{C_L} = 3$$



Input Data (n bits)



Minimizing Transition Activity is not the Right approach to Minimize Power



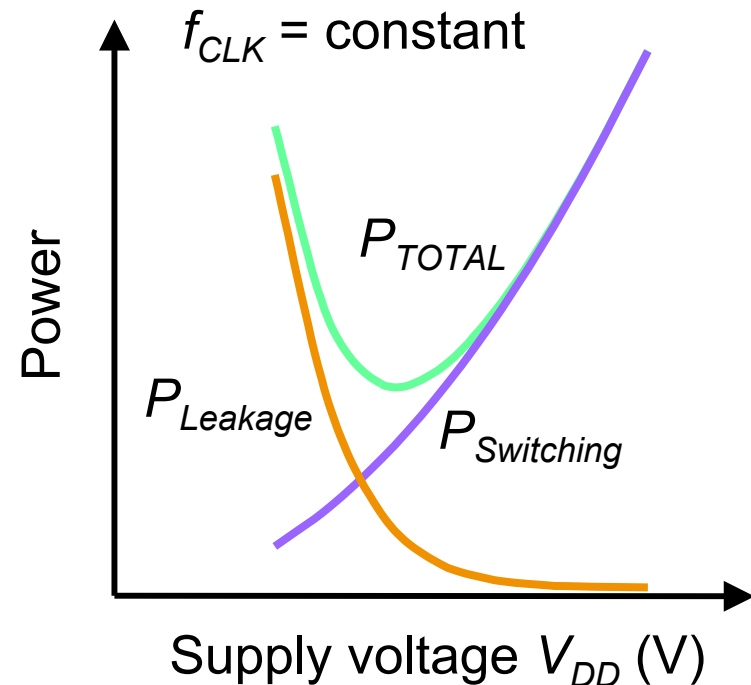
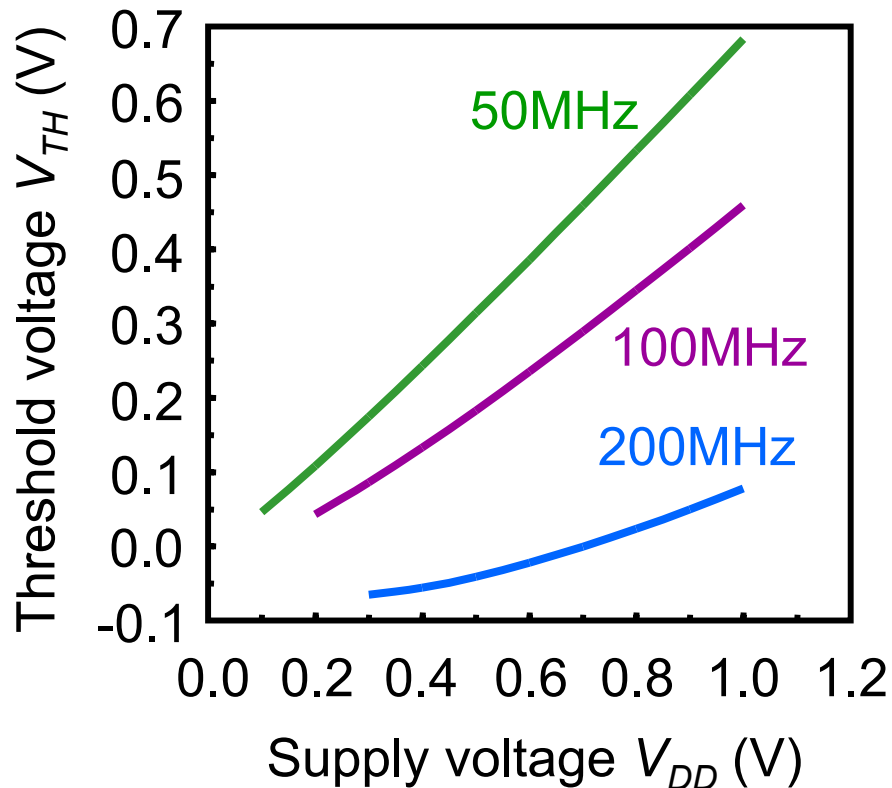
Optimal V_{DD} and V_{TH} Control



$$f_{CLK} = \frac{\beta}{C_L} \cdot \frac{(V_{DD} - V_{TH})^\alpha}{V_{DD}}$$

$$P_{Switching} = a \cdot f_{CLK} \cdot C_L \cdot V_{DD}^2$$

$$P_{Leakage} = I_{10} \cdot V_{DD} \cdot 10^{\frac{V_{TH}}{S}}$$



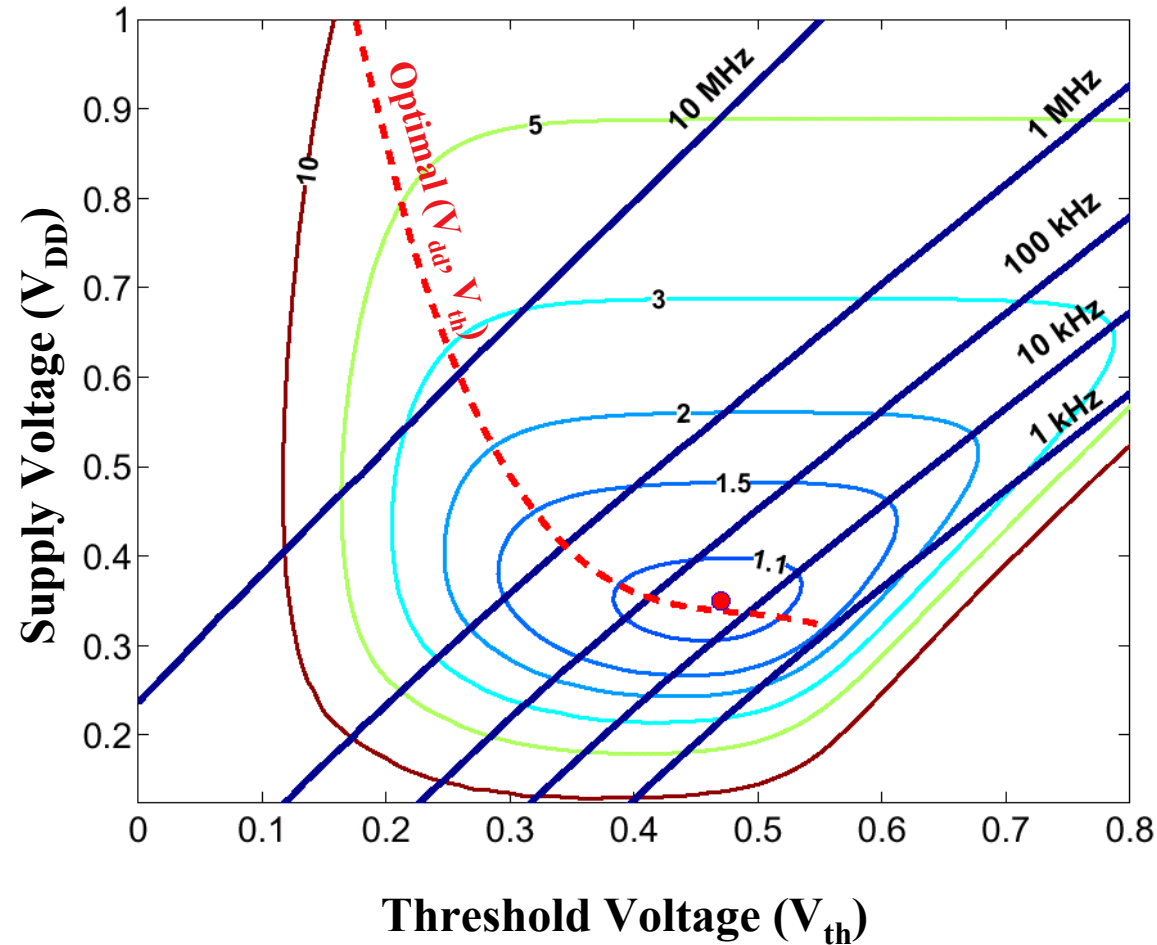
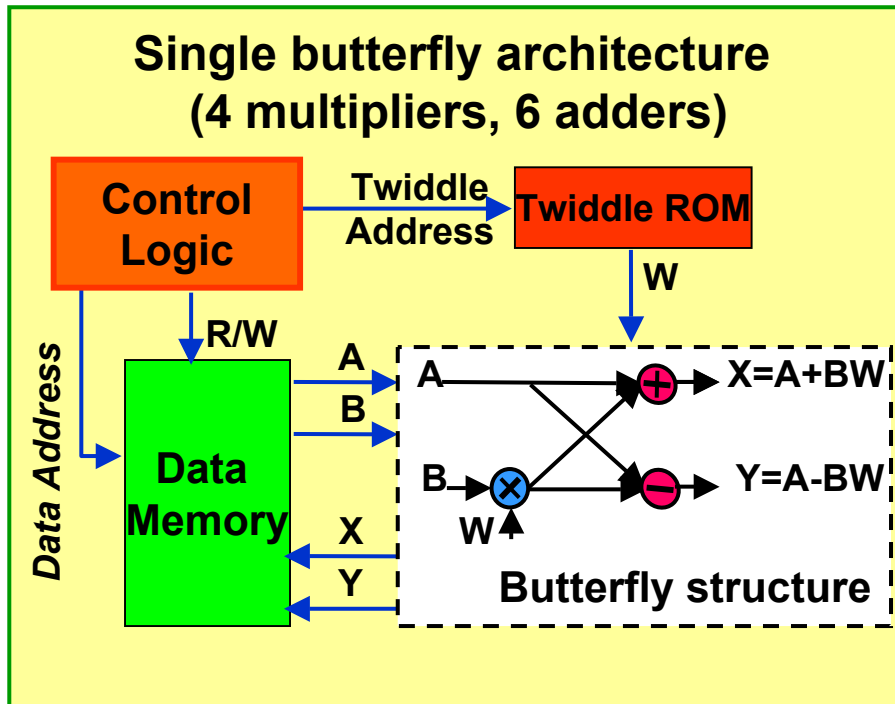
- V_{DD} and V_{TH} can be varied to keep a fixed performance



Energy Efficiency of Digital Computation



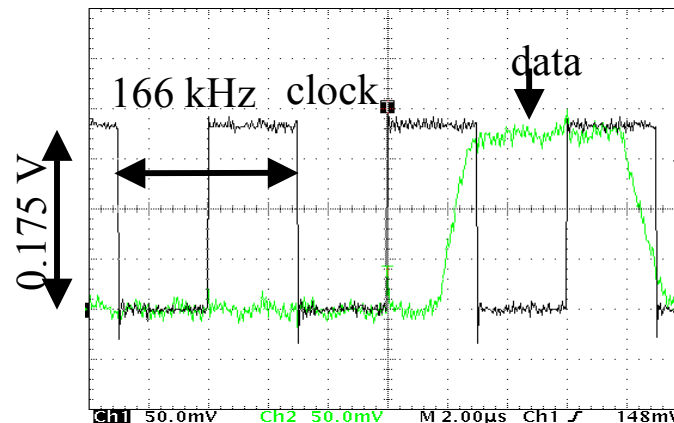
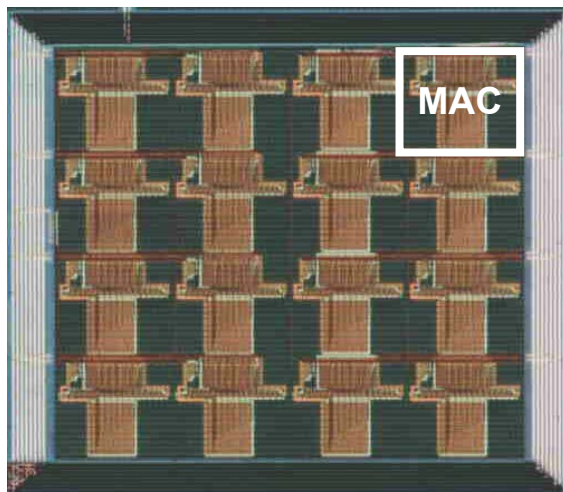
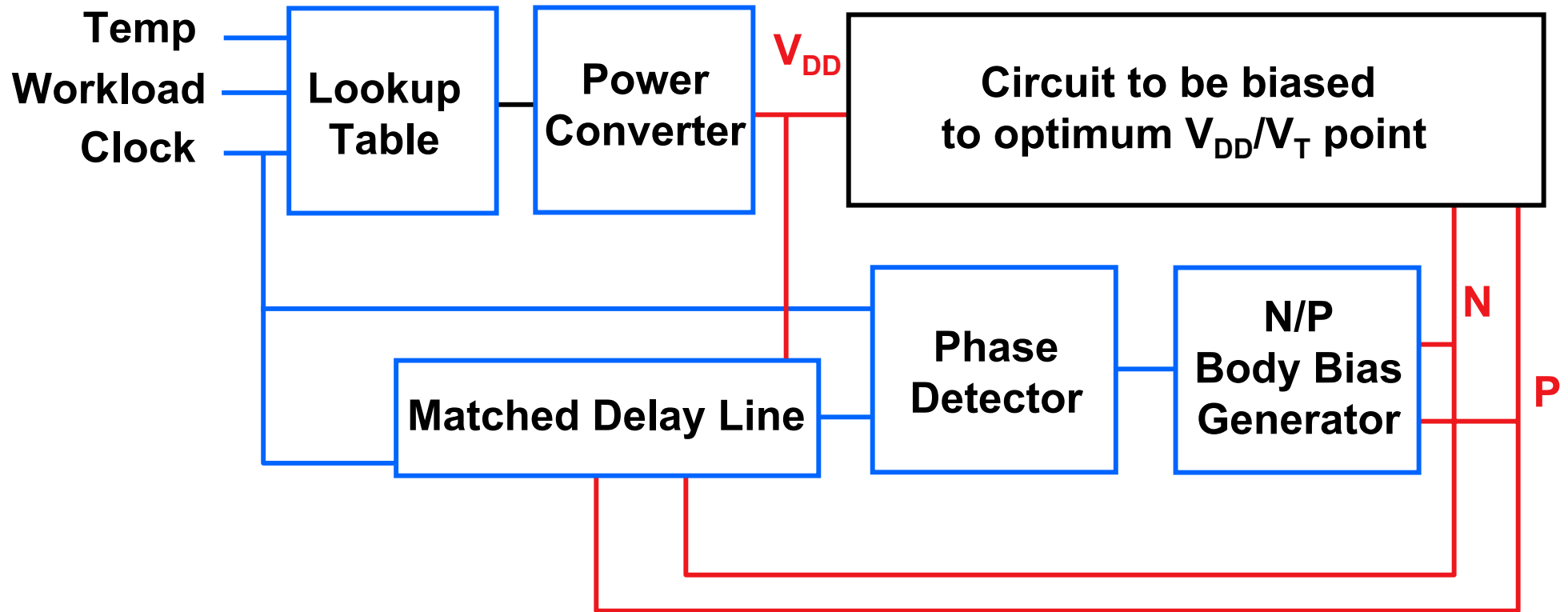
FFT Computation



Exploit Sub-threshold Operation for Sensor Circuits



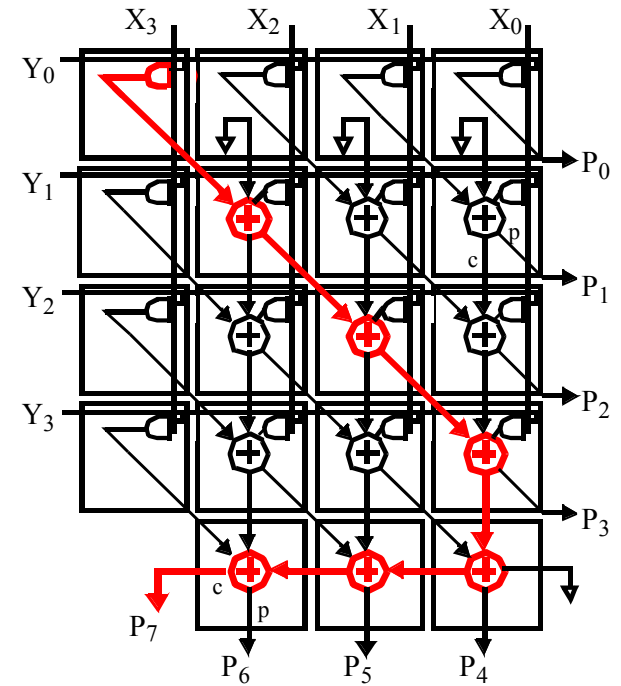
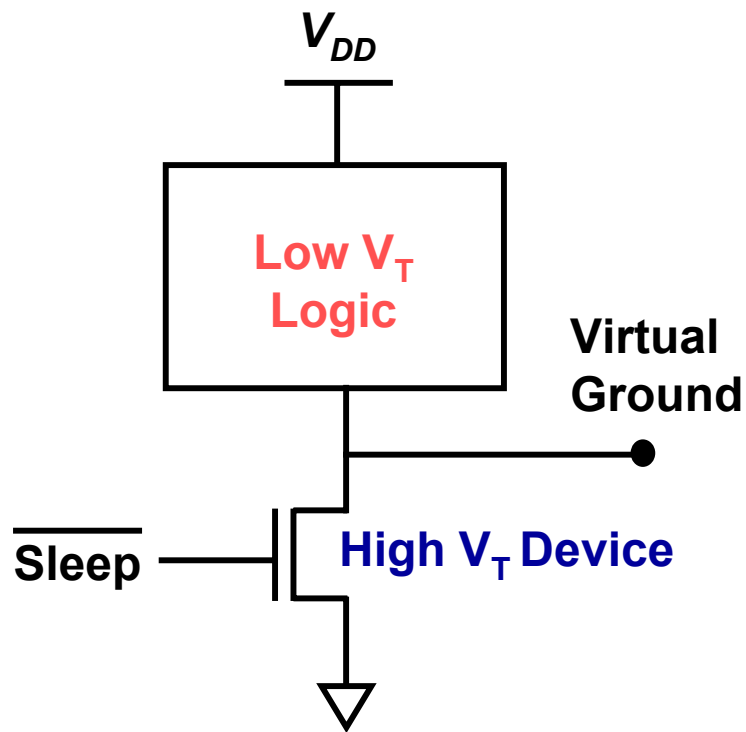
Adaptive V_{DD}/V_T Architecture



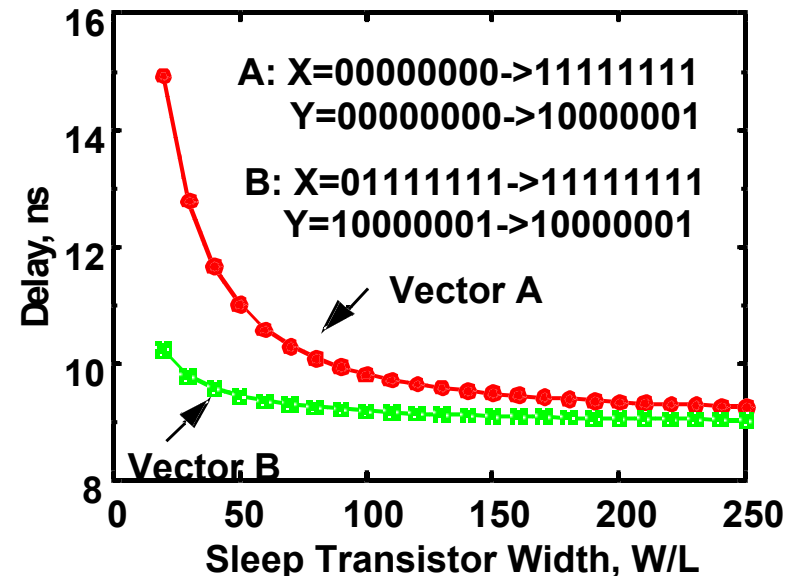
[Miyazaki, ISSCC '02]



Leakage Mitigation Using MTCMOS



Device Sizing is a Major Concern in Multiple Threshold CMOS

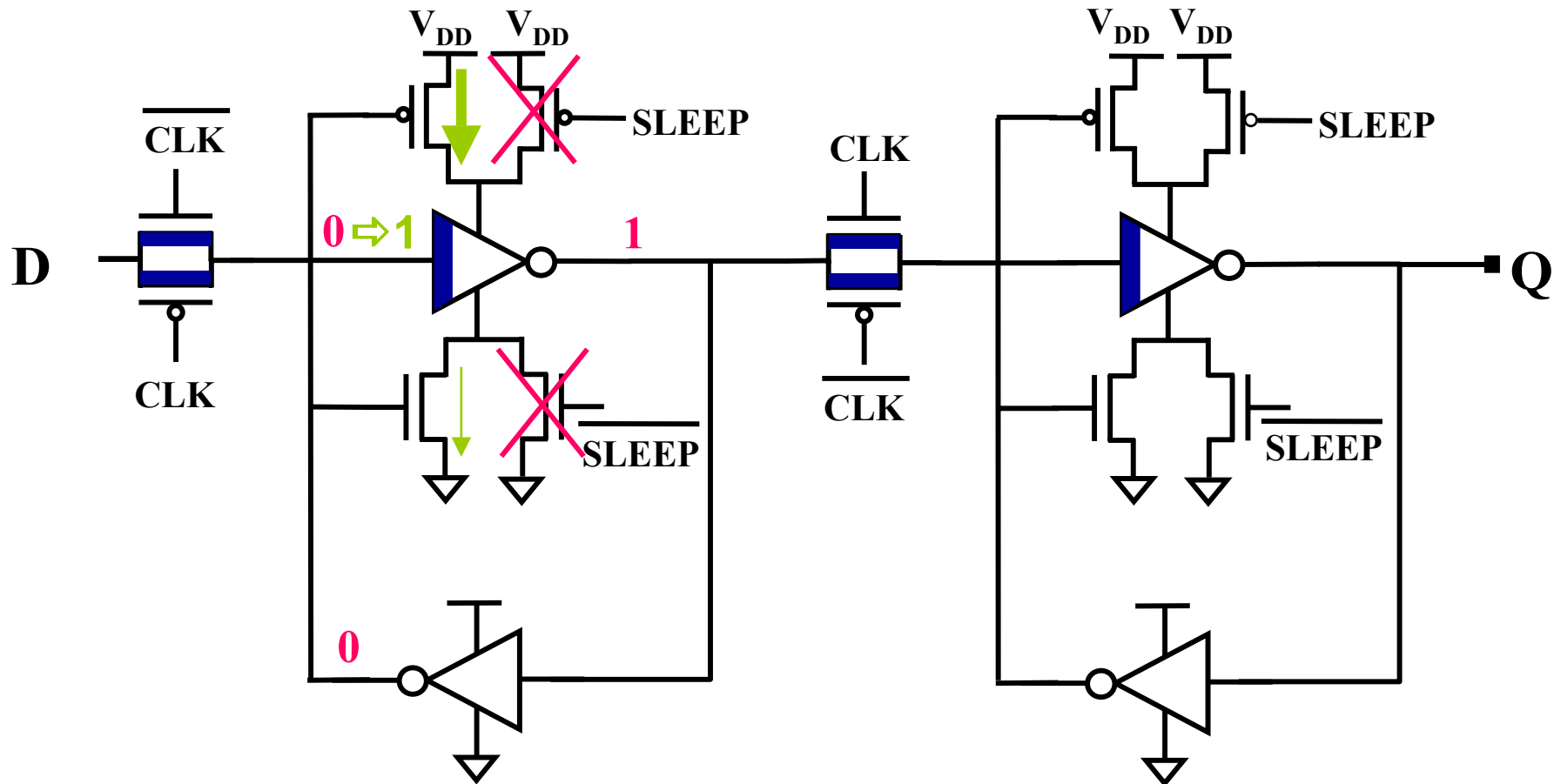




“Leakage Feedback” Flip-Flop



In the Idle Mode , with inputs drifting

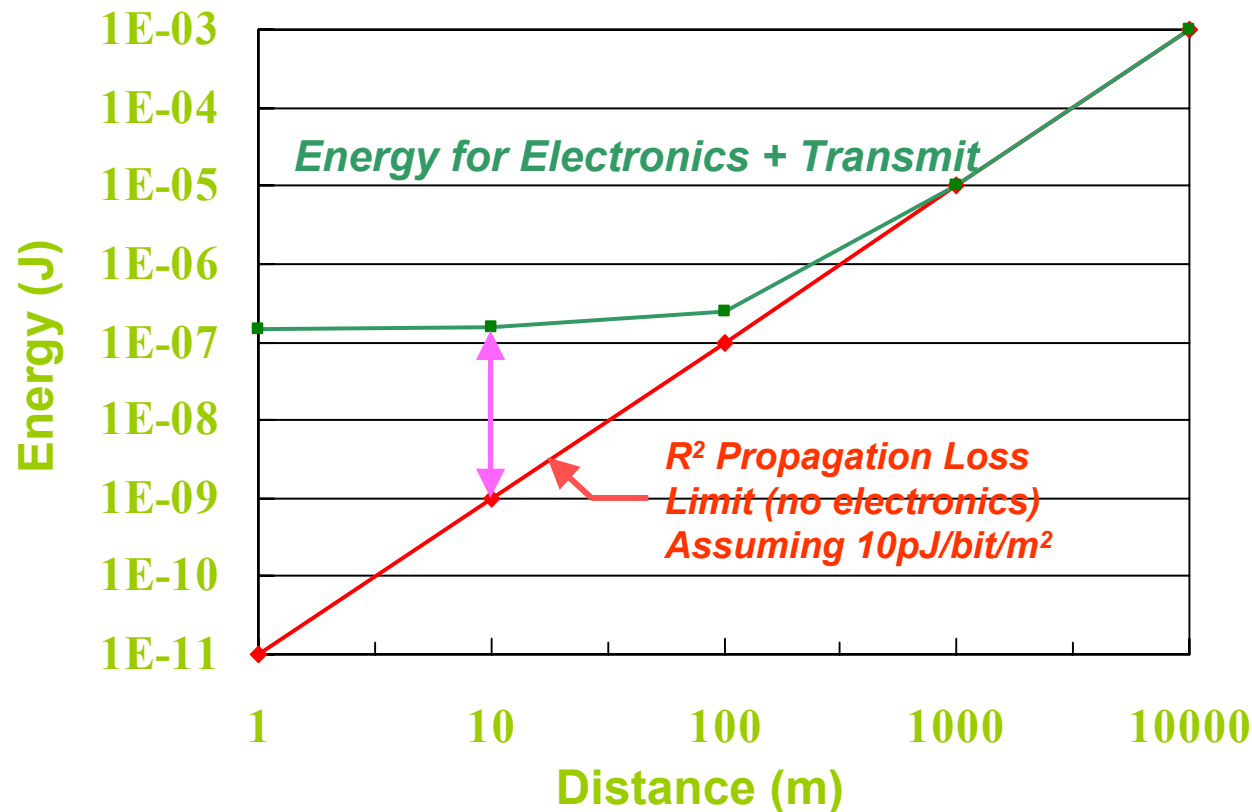


[Kao, ESSCIRC '01]

- Use leakage to hold state in the flip-flop – very low leakage in sleep mode, with high-performance in active mode



Computation vs. Communication

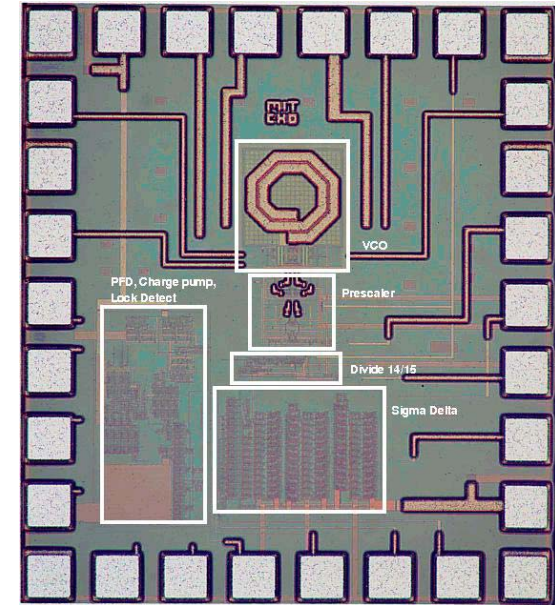
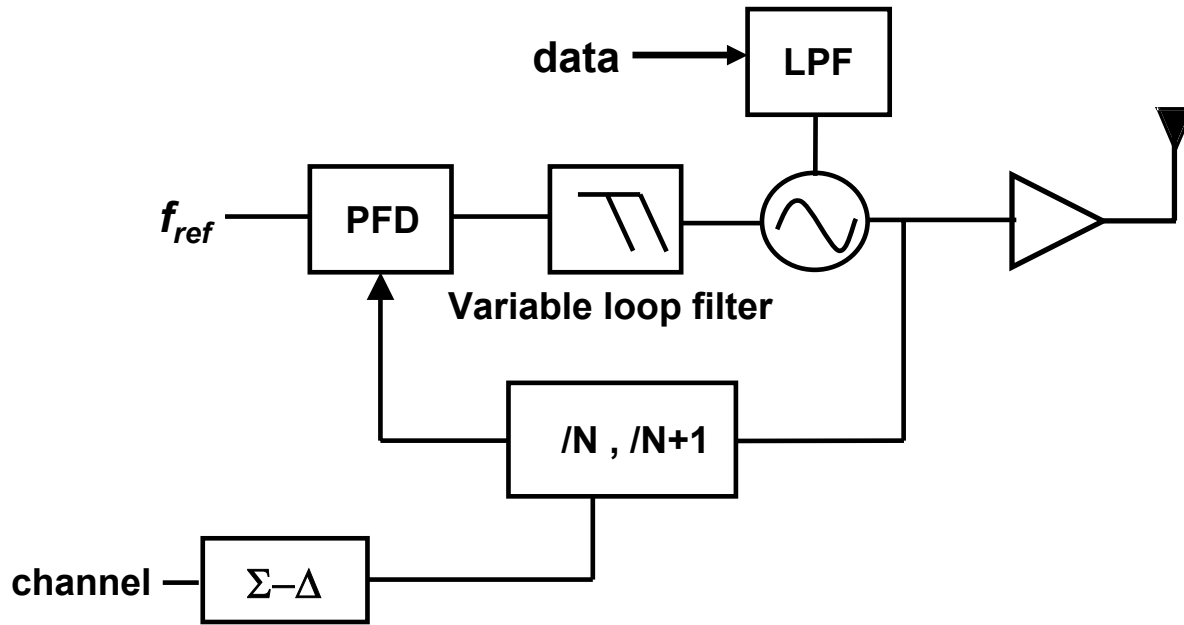


- Computation: 1nJ/op (μ -Processor) and Communication (@10m): 150nJ/bit
- @10 m: ~150 instructions/transmitted bit on a low-power processor
- @10m: > 1Million instructions/transmitted bit using dedicated hardware

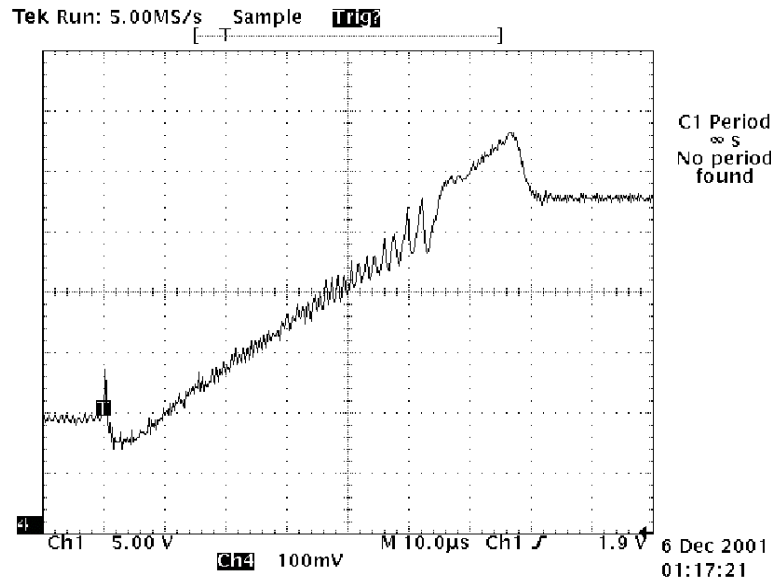
Compute, Don't Communicate



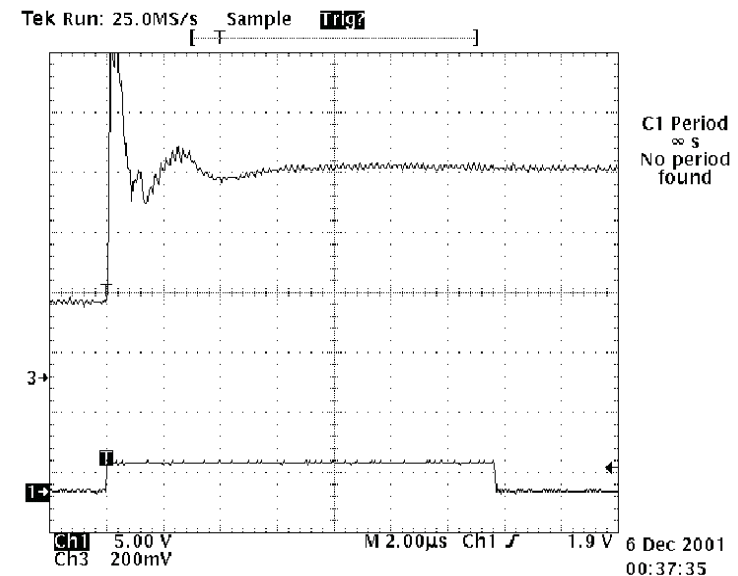
Fast Startup Transmitter



E/bit = 10nJ/bit



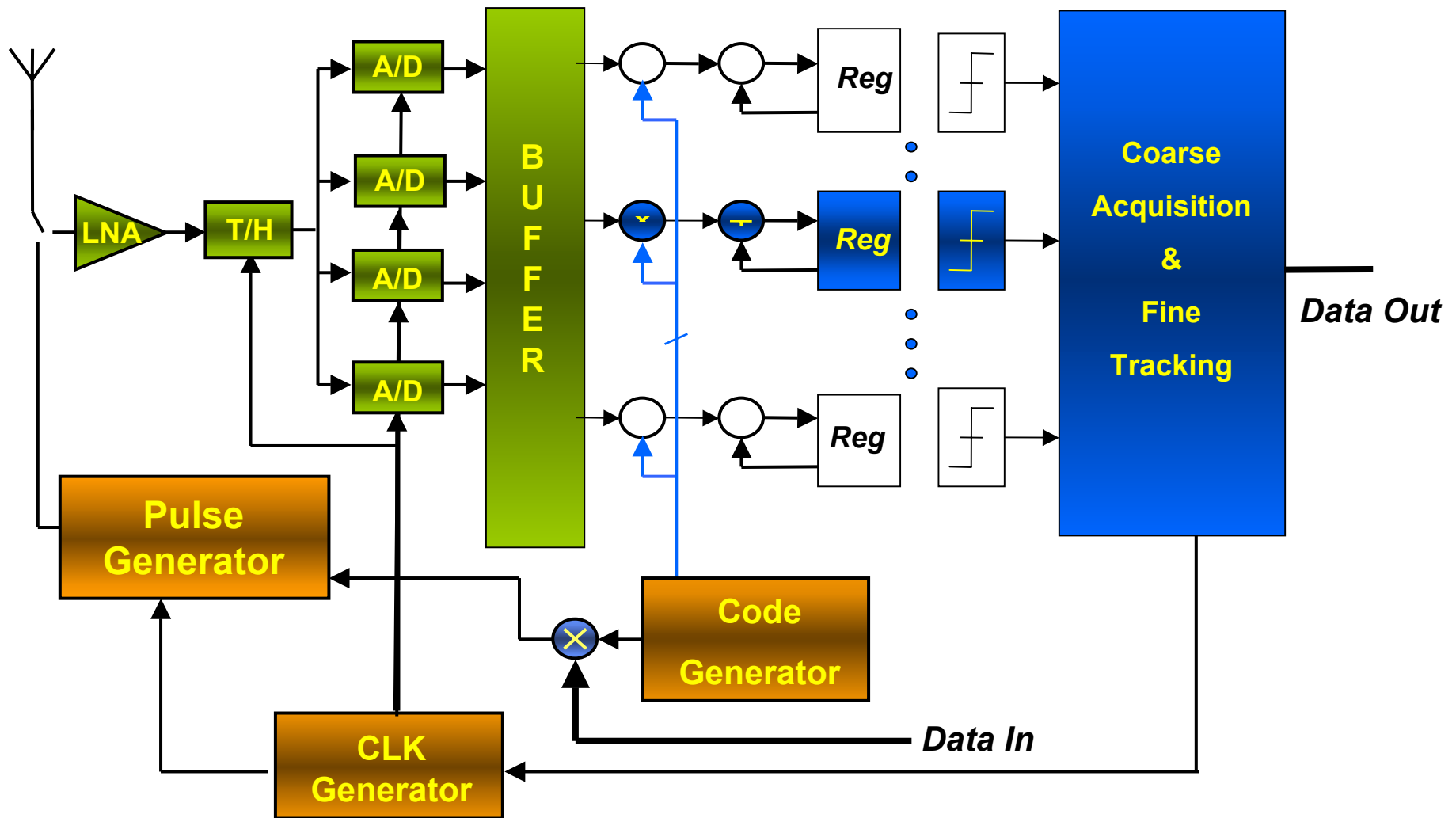
Fixed loop bandwidth



Variable loop bandwidth



New Opportunities: “Digital” UWB Radio



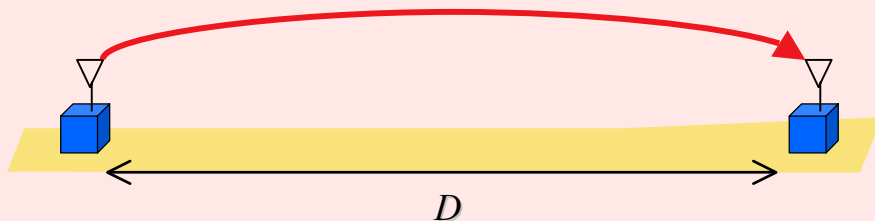
- Minimal Front-end components: leverage low-power digital circuits
- 3-4 bits A/D sufficient (Newaskar, Blazquez, Chandrakasan, SIPS '02)



Multihop and the Characteristic Distance



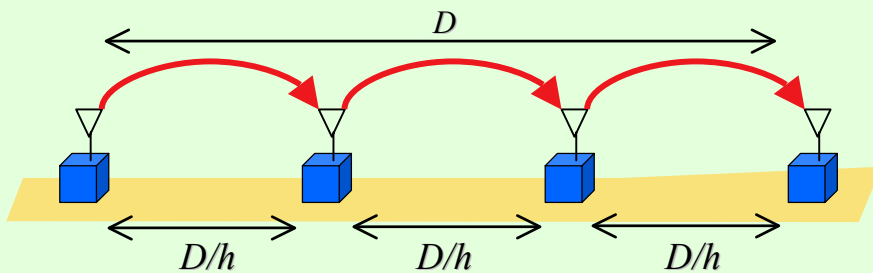
Direct Transmission



$$E = \alpha_1 + \alpha_2 D^2$$

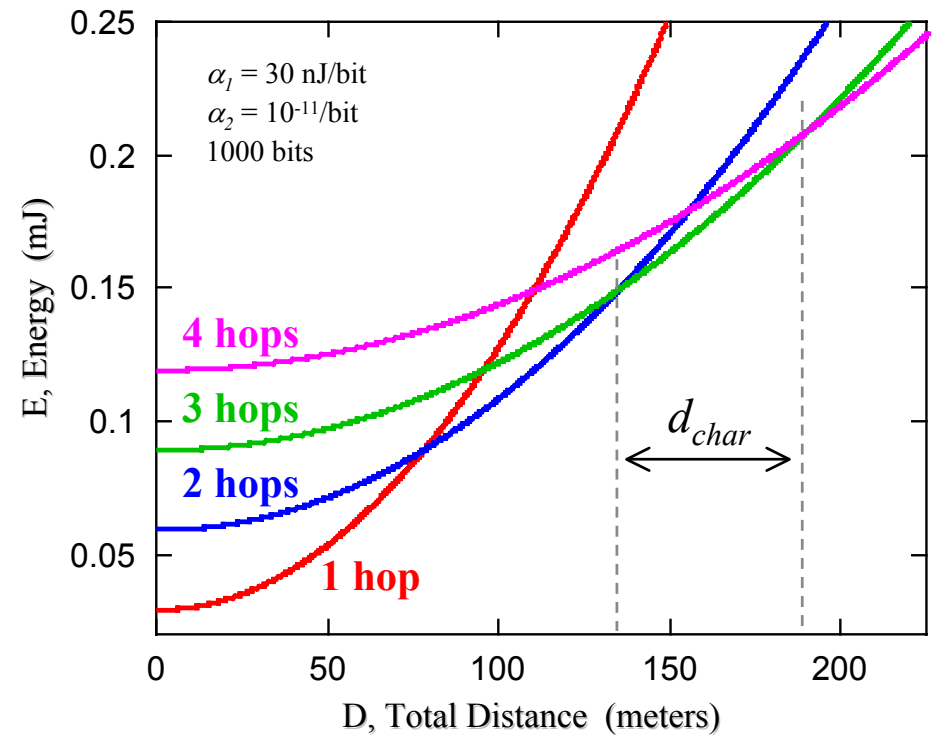
α_1 : Tx & Rx Radio Electronics
 α_2 : attenuation, power amp
 path loss exponent

Multihop Transmission



$$E = h \left[\alpha_1 + \alpha_2 \left(\frac{D}{h} \right)^2 \right]$$

h : number of hops
 $\frac{D}{h}$: per-hop distance



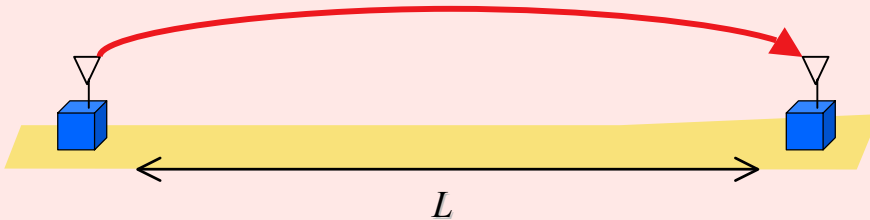
Characteristic Distance for Multihop Transmission

$$\min_h E = 2\alpha_1 \frac{D}{d_{char}}$$

$$\text{where } d_{char} = \sqrt{\frac{\alpha_1}{\alpha_2}}$$

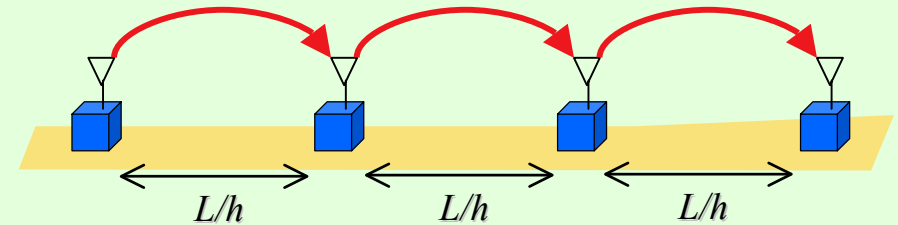


Analogy to Buffered Interconnect

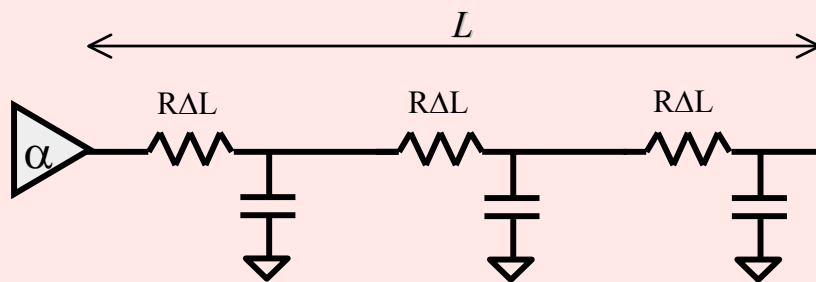


$$E = \alpha_1 + \alpha_2 L^2$$

$$d_{char} = \sqrt{\frac{\alpha_1}{\alpha_2}}$$

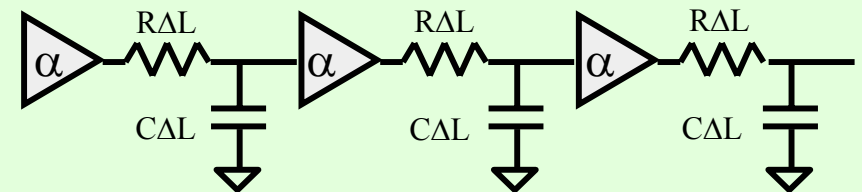


$$E = h \left[\alpha_1 + \alpha_2 \left(\frac{L}{h} \right)^2 \right]$$



$$T = \alpha + RCL^2$$

$$d_{char} = \sqrt{\frac{\alpha}{RC}}$$



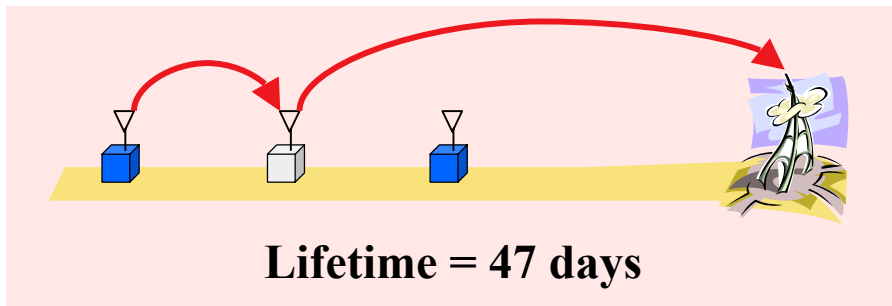
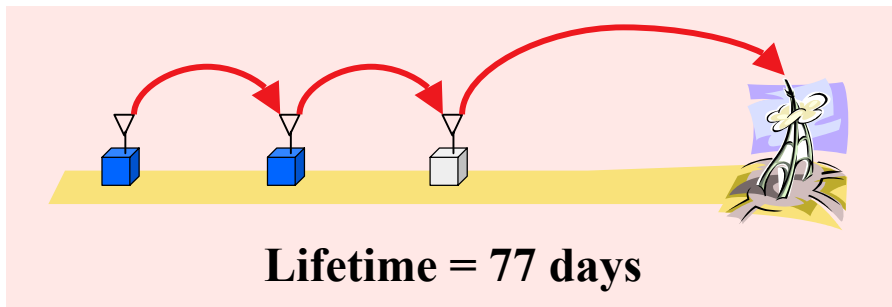
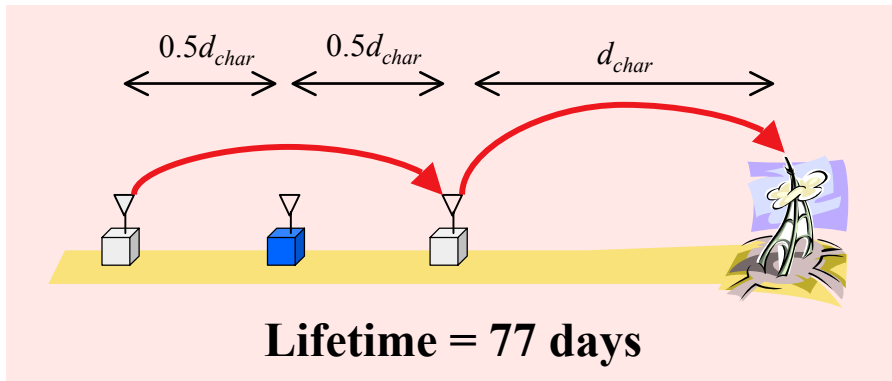
$$T = k \left[\alpha + RC \left(\frac{L}{k} \right)^2 \right]$$



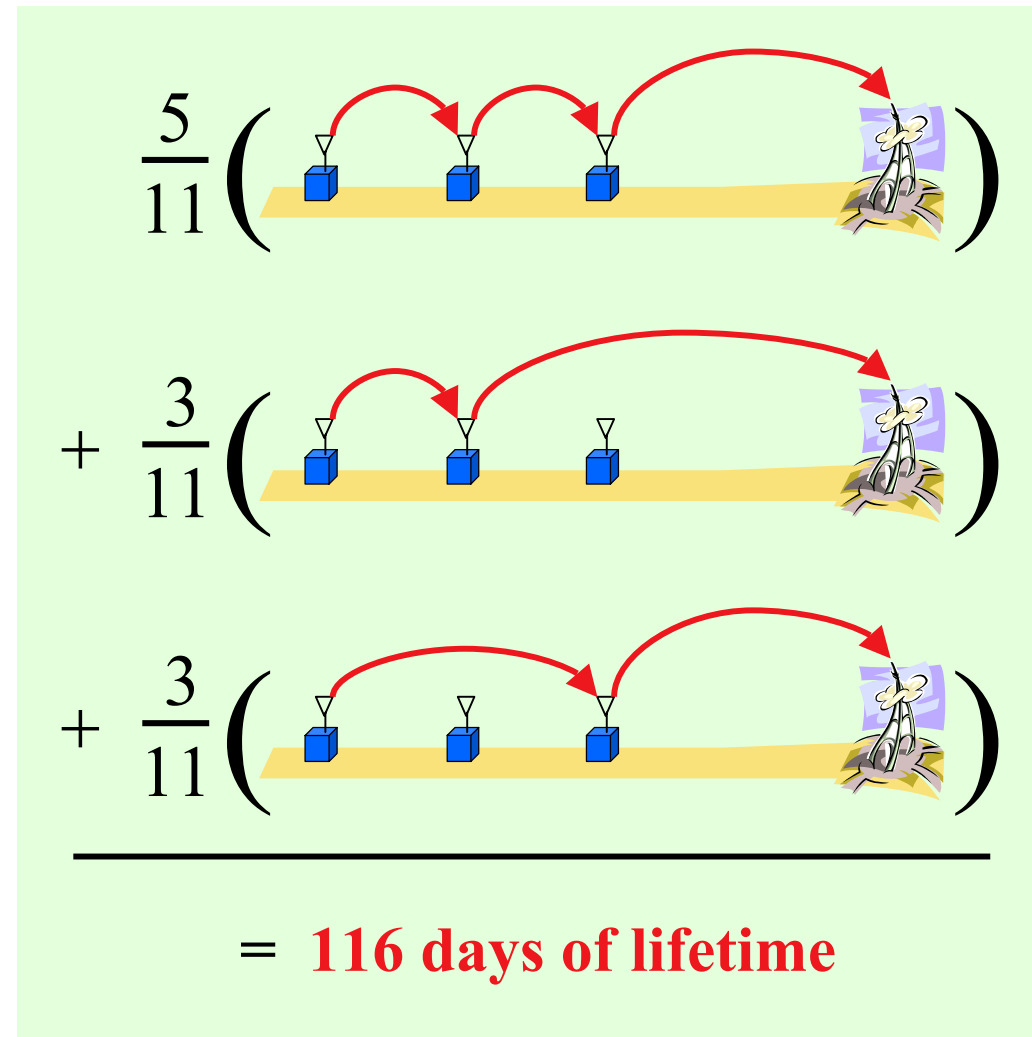
Dithering of Characteristic Distance



Fixed Multihop Routes



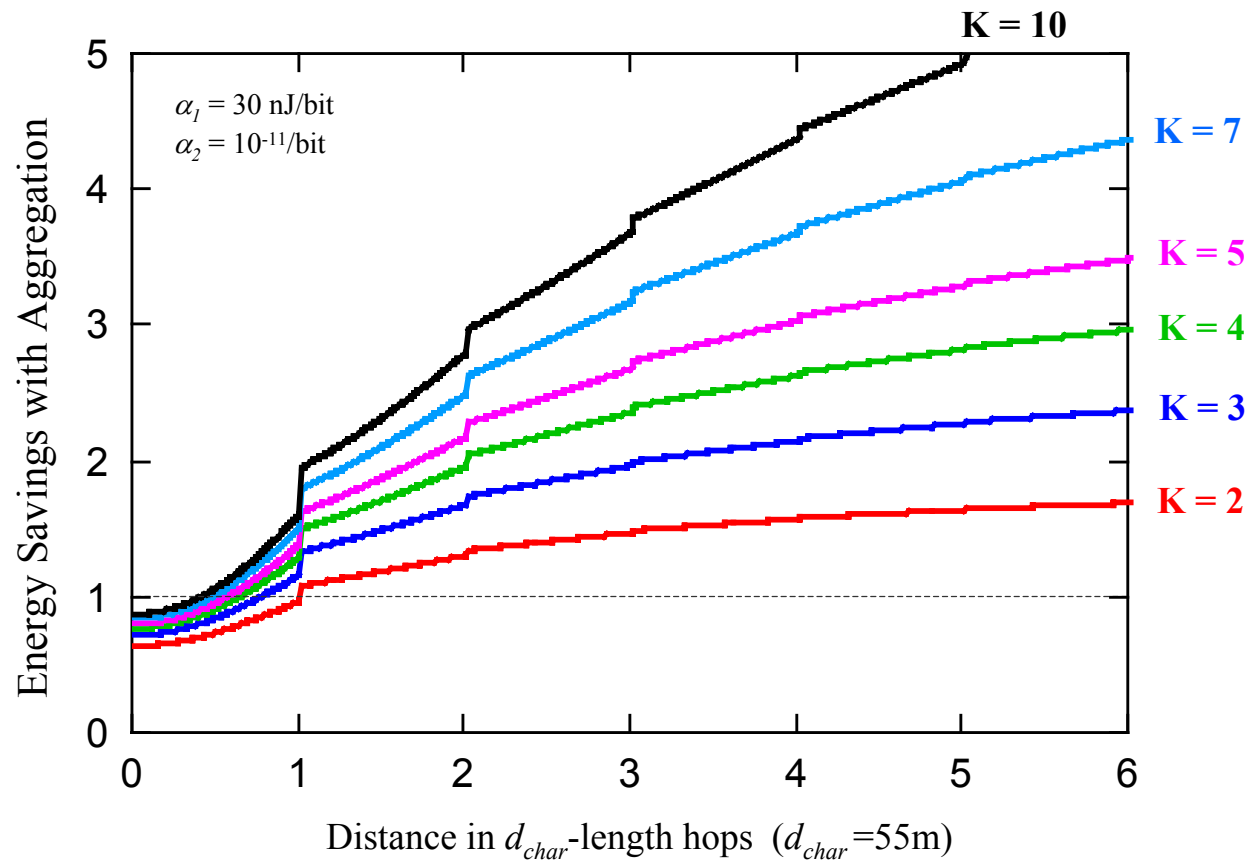
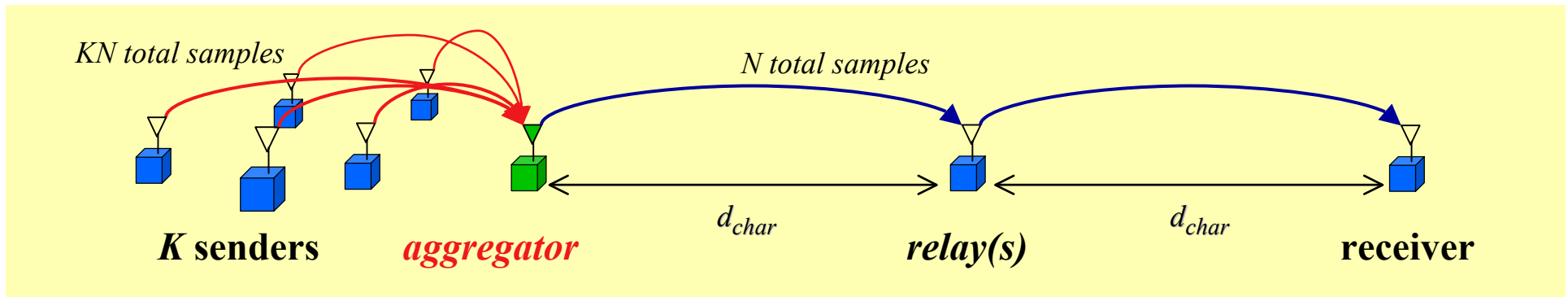
Rotated Routes



Even spatial distribution of energy burden

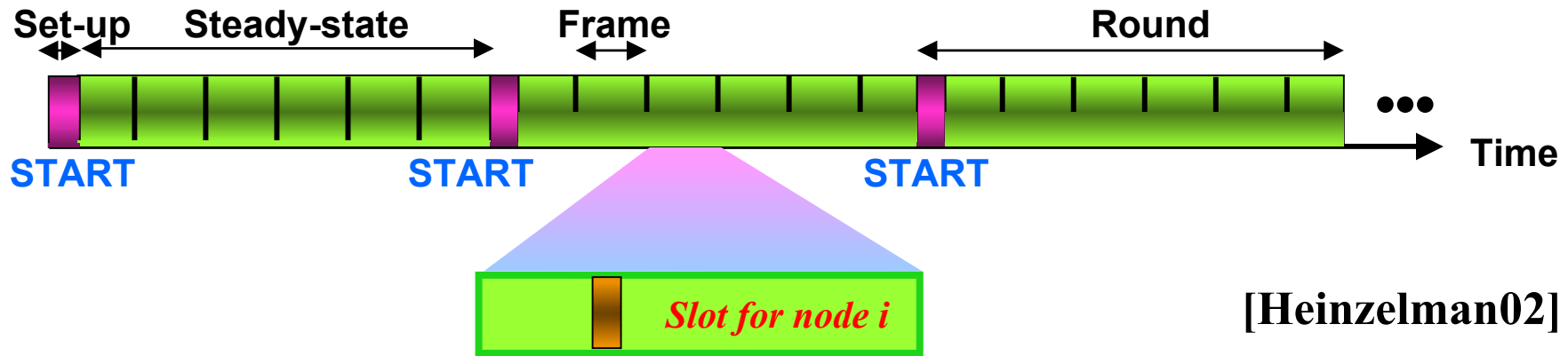


Signal Processing in the Network

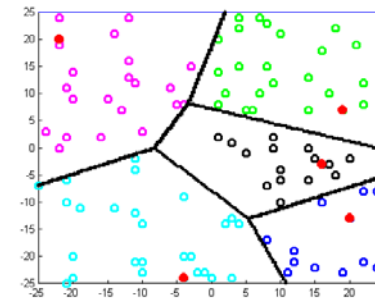




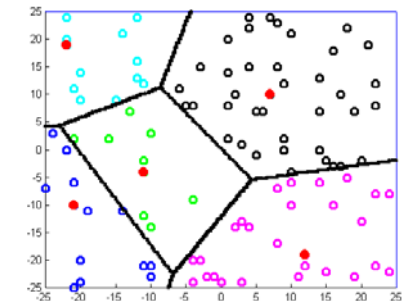
Clustering Protocols



- **Clustering**
 - Localized control (through the “cluster head”)
 - Local data aggregation
- **Randomized Rotation of cluster-heads**
 - Clusters formed during set-up
 - Data transfers during steady-state
- **TDMA in steady state**
 - Node i transmits once per frame
 - No collisions \Rightarrow low energy
 - Maximum sleep time



Round n

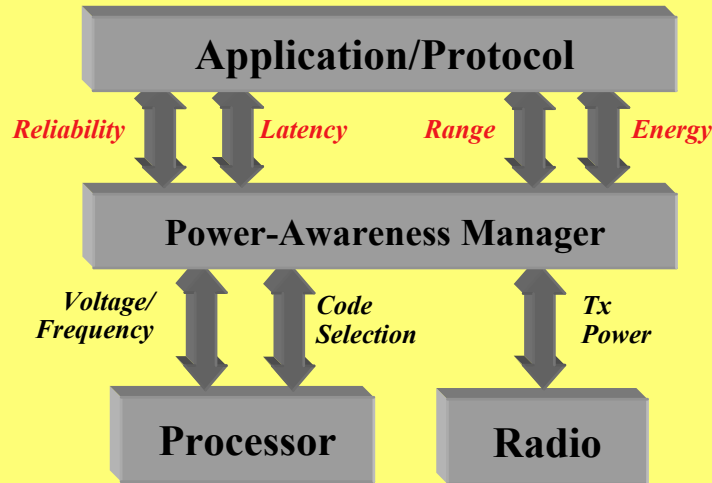


Round $n+1$

Opportunity: Reactive Radios [Rabaey, ISSCC02]



API and Middleware Layer



Power Aware API: performance of communication defined and exposed as a basis for trade-offs

- `set_max_energy`(Energy energy)
- `set_max_latency`(Time latency)
- `set_min_reliability`(Prob probReception)
- `set_range`(int nearestNodes, Node[] who, float meters)

Quality of communication defined along four axes:

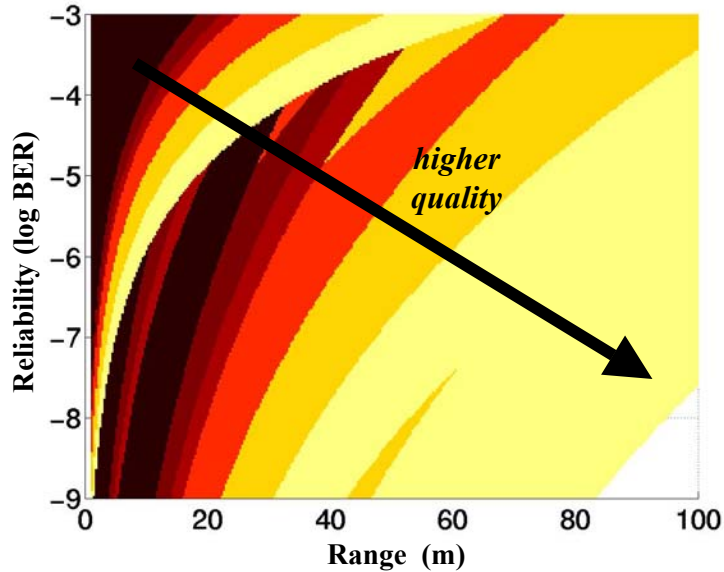
Concern	Metric
“To whom?”	Range (m)
“How soon?”	Latency (ms)
“How reliably?”	Reliability (BER)
“How much energy?”	Energy (μ J)



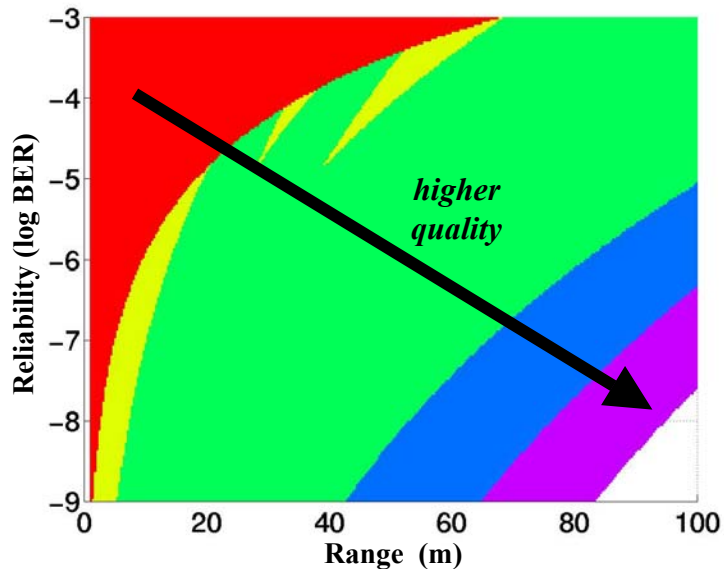
API-Controlled Operational Policy



Radiated Power

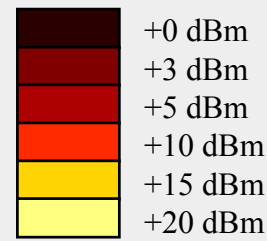


Convolutional Code

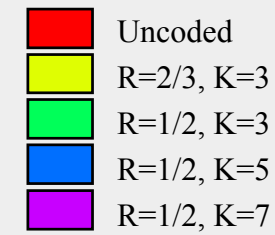


Operational Policies

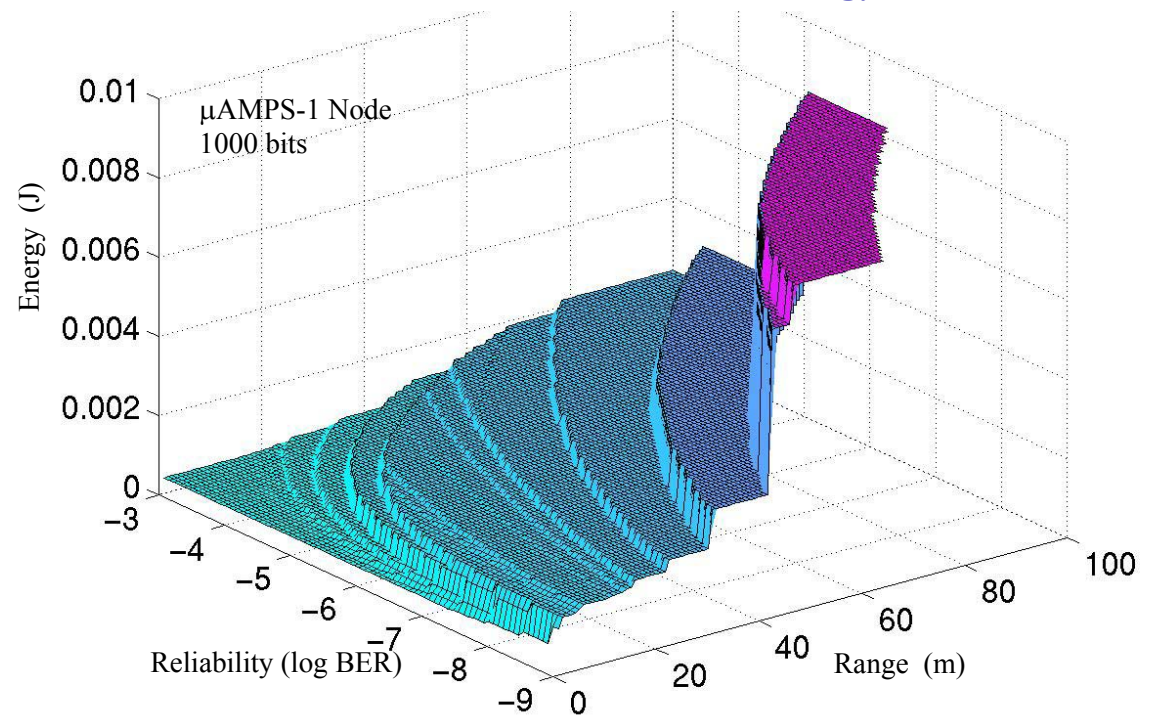
Radiated Power



Convolutional Code



Total Communication Energy



Energy scales gracefully with communication quality



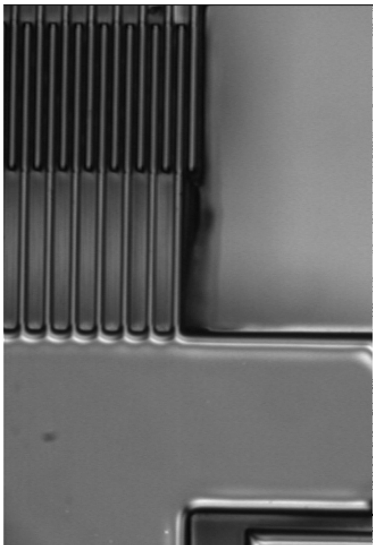
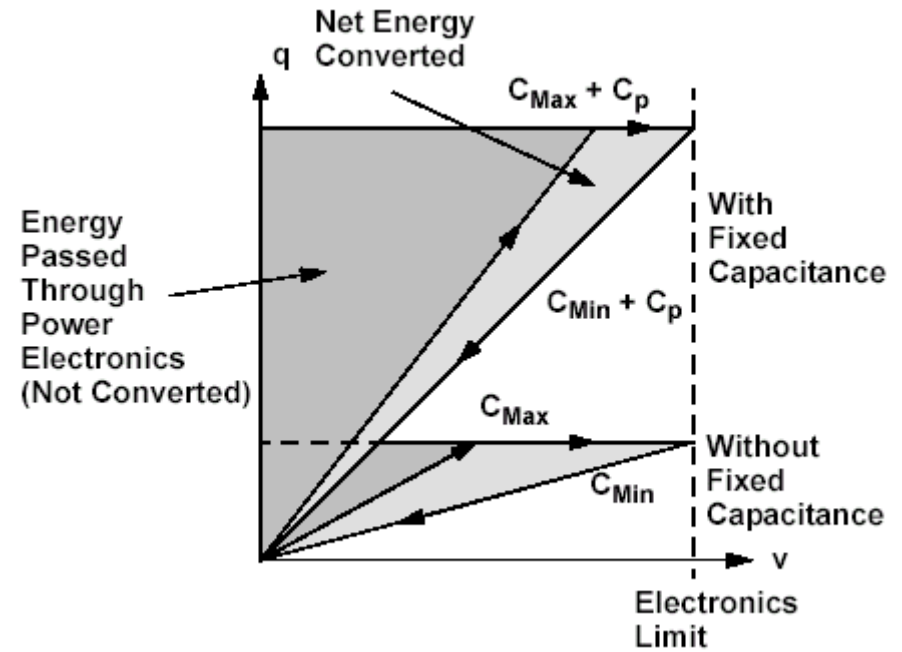
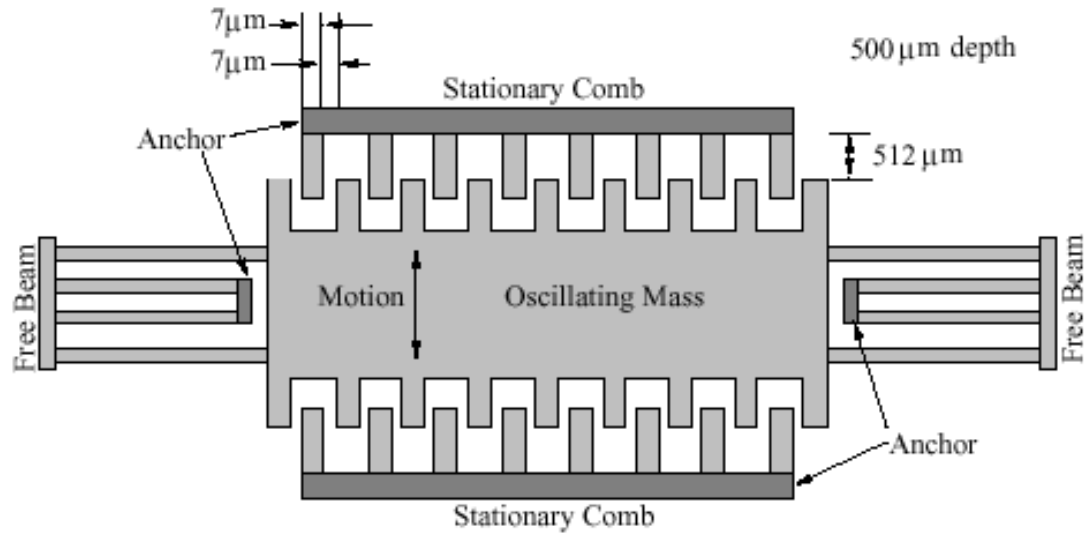
Energy Scavenging



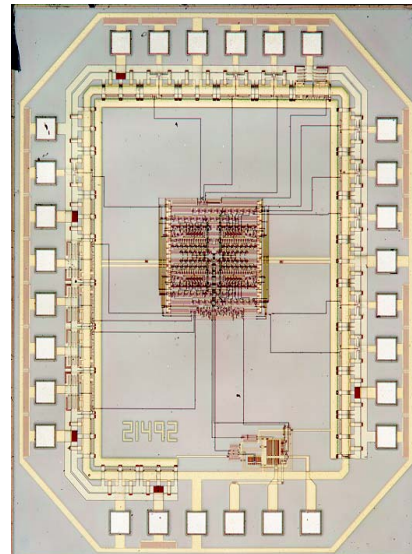
- Self-powered operation is a real option if the power dissipation can be scaled to 10's - 100's of μW
 - Mechanical vibration (e.g., machine mounted sensors)
 - Electromagnetic fields (RF)
-
- A major opportunity exists in developing **energy scavengers** (generator and associated electronics) for extracting useful energy from ambient sources



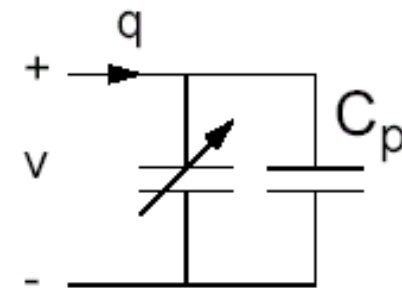
Vibration-to-Electric Energy



MEMS Generator



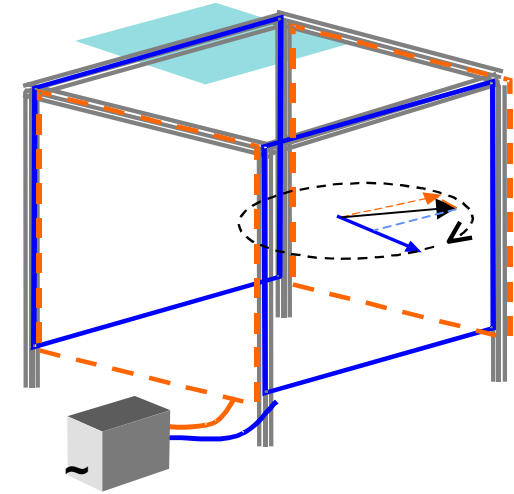
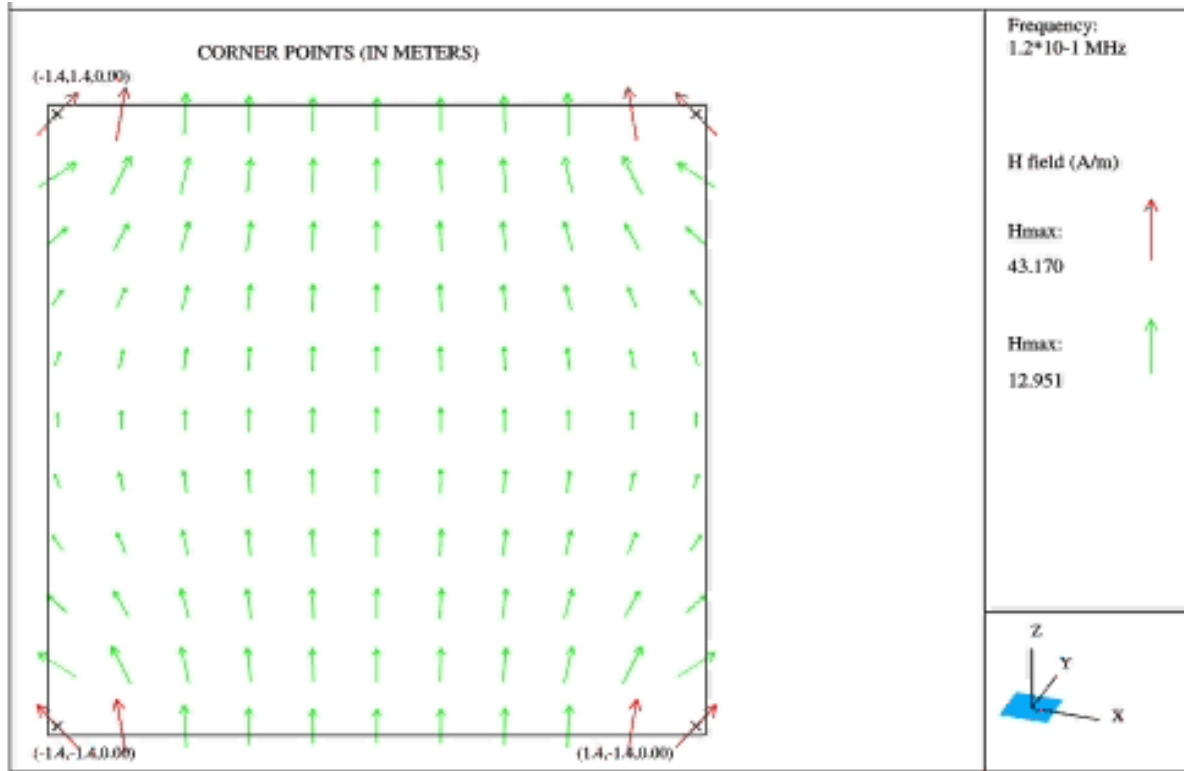
Controller



Hardwired Fabrics enable No Power Signal Processing (10µW from generator)

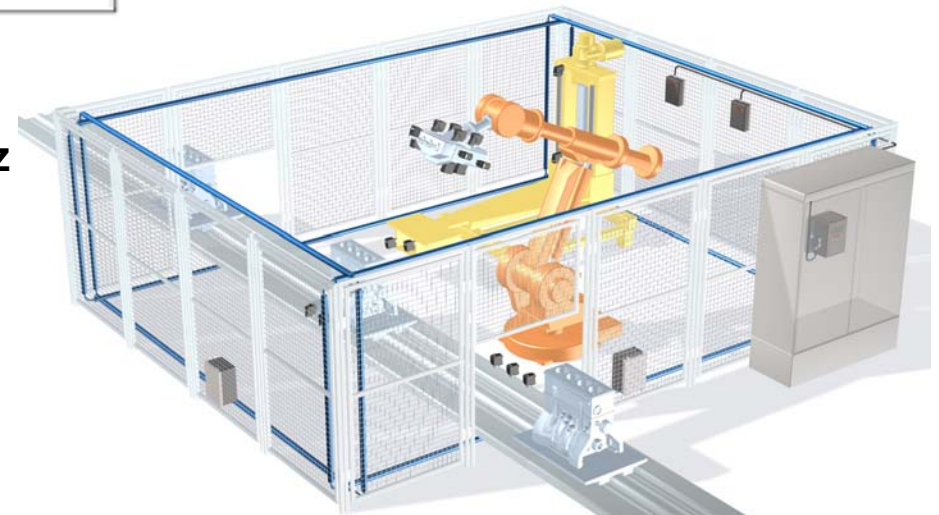


Proximity Sensor: Wireless Power Supply



Simulation of rotating field over one period at 120kHz
(in middle of 2D arrangement and supplied plane xy)

Courtesy of Snorre Kjesbu, ABB

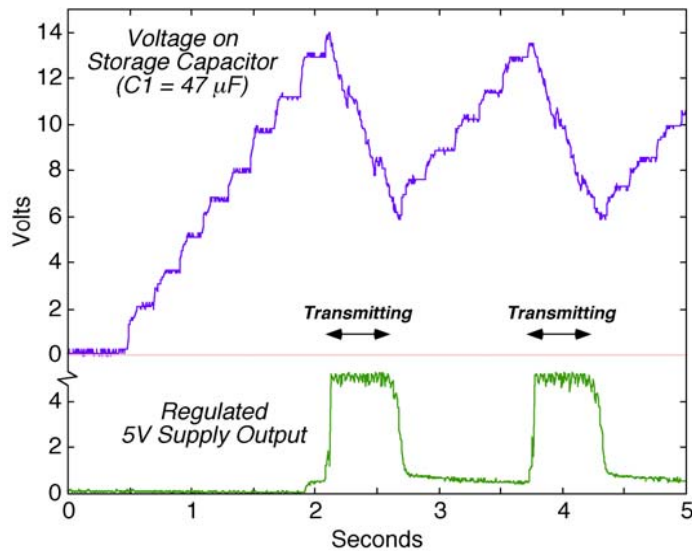




Heel-Strike Energy Harvesting

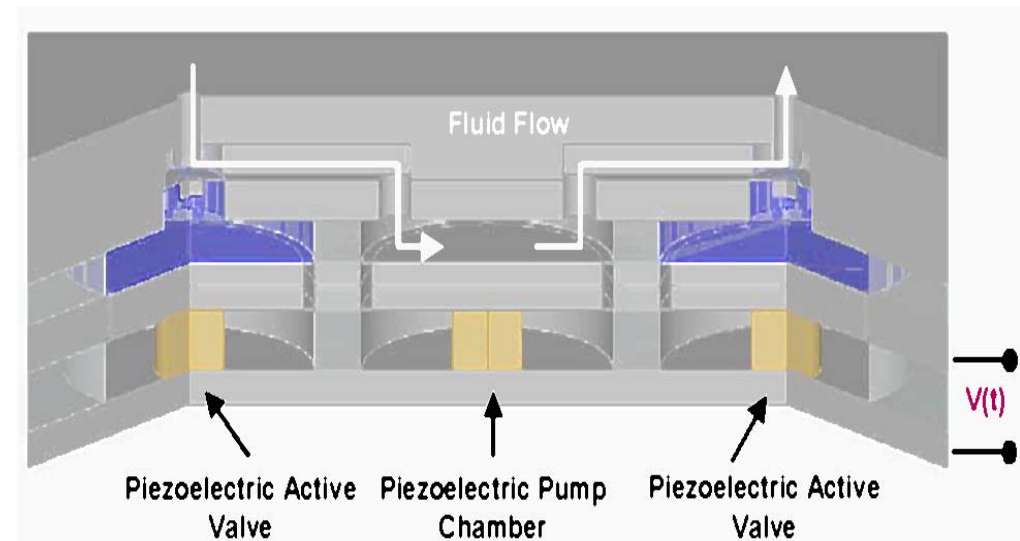
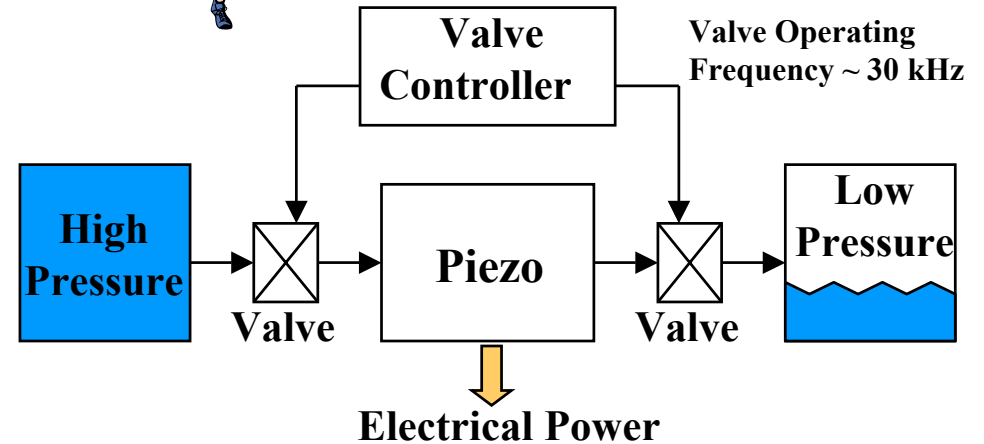
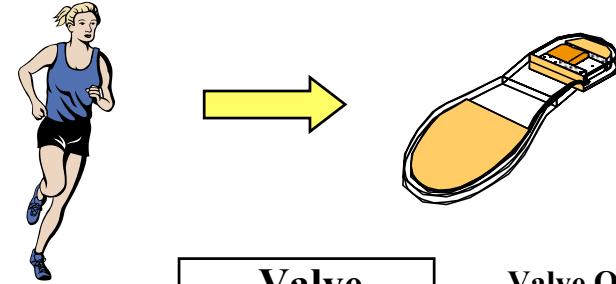


Joe Paradiso (MIT Media Lab)



After 3-6 steps, it provides 3 mA for 0.5 sec $\sim 10\text{mW}$

Hagood, Spearing, Schmidt (MIT)

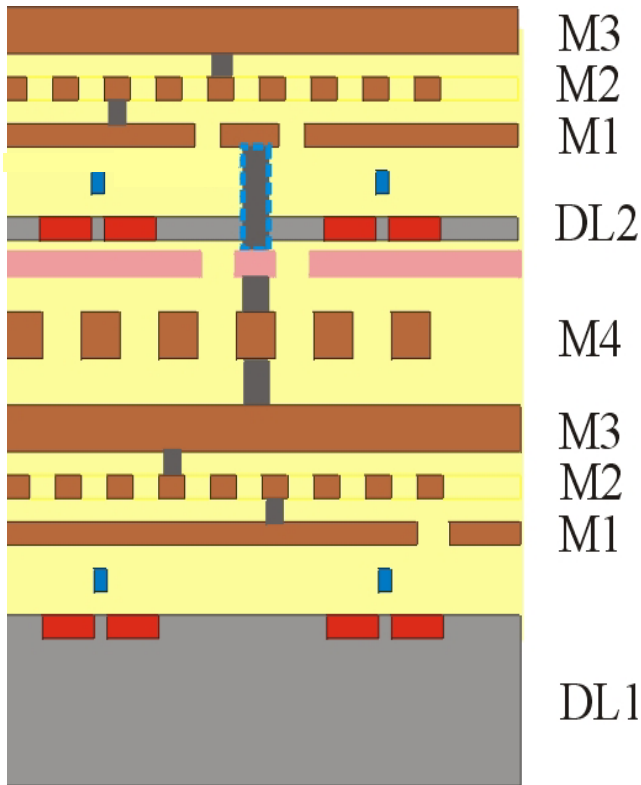




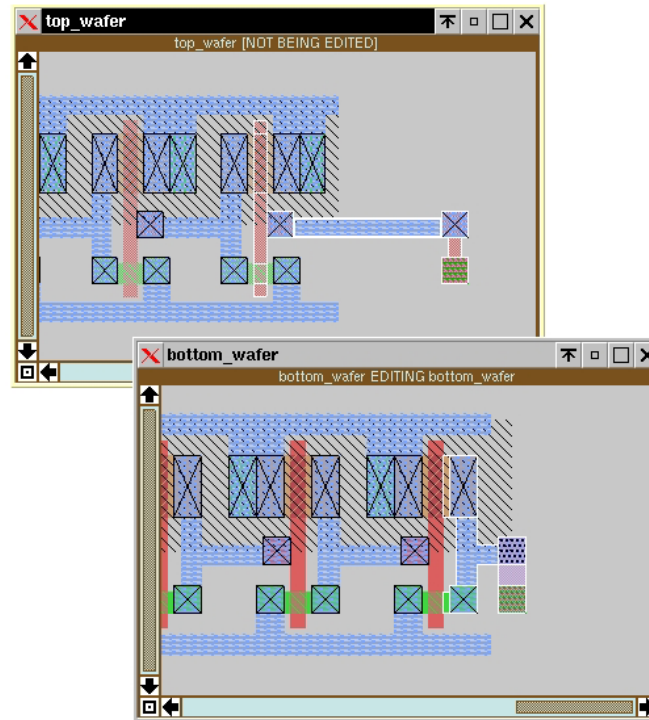
3D Integration



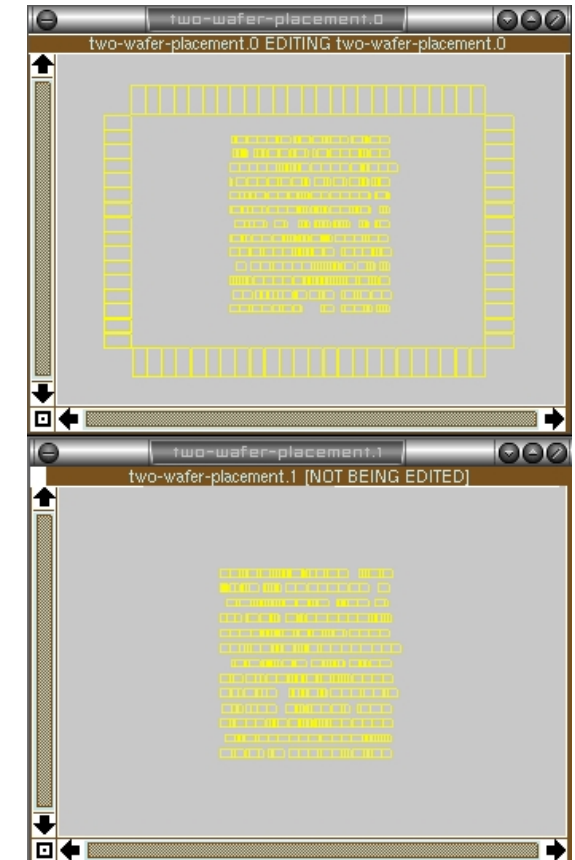
3-D Integration



3-D Layout Editor



3-D Standard Cell Placement and Routing



Compact Interconnection of Heterogeneous Technologies



Conclusions



- Exciting new applications enabled by a network of low-power wireless sensing devices
- Power Aware Design Methodology supersedes Energy Efficient Design
- ***Slower is Better*** – exploit sub-threshold operation as fastest switching speed is not needed
- ***Communication-centric design***
 - Energy per operation (mW/MIPS) will scale with technology
 - Communication costs (nJ/bit) will not scale at the same rate

Low Energy Sensor Design Requires a System-level Approach – Tight Coupling Between Fabrics, Algorithms and Protocols