Ultra-Dynamic Voltage Scaling Using Sub-threshold Operation and Local Voltage Dithering in 90nm CMOS

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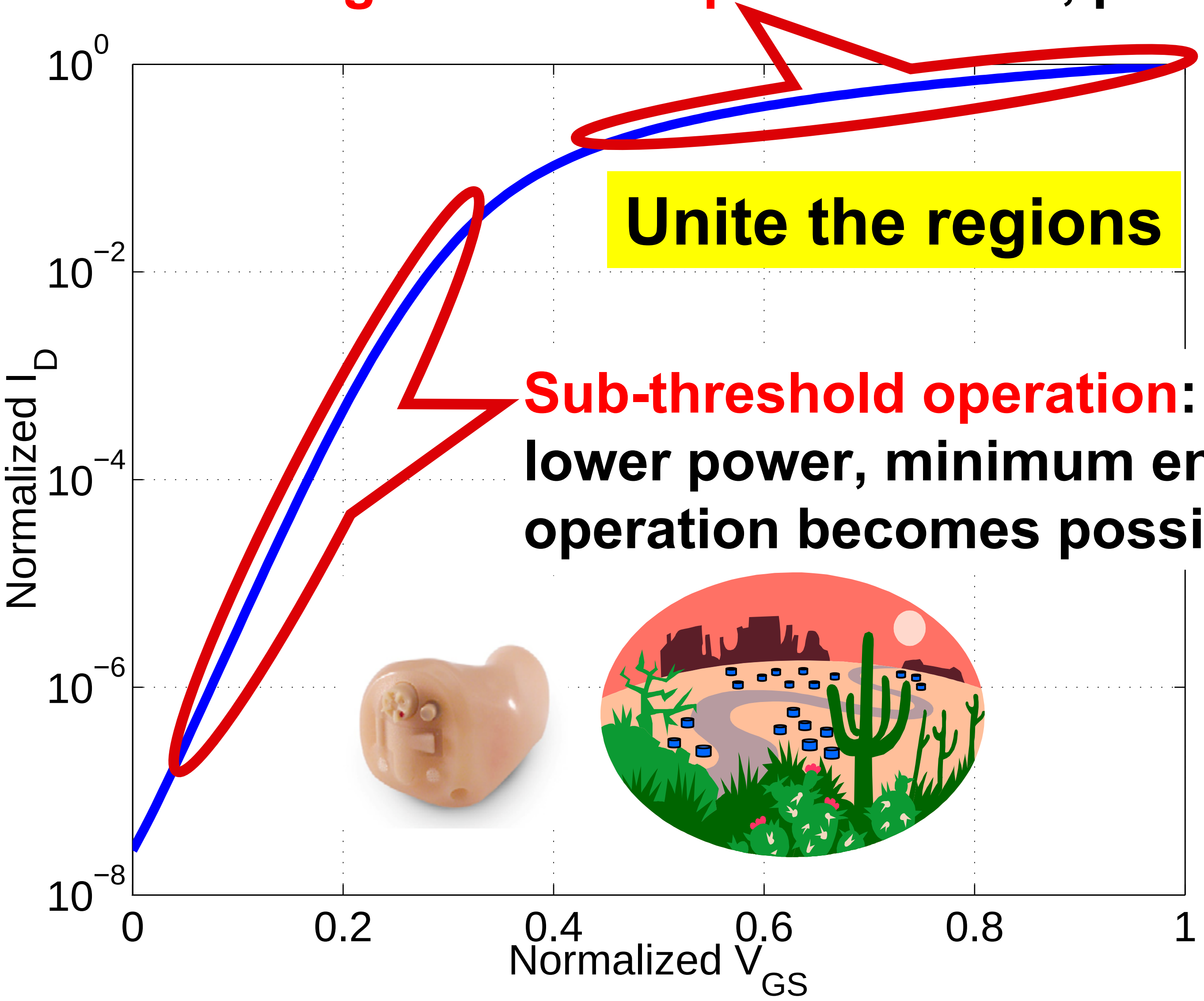
Ultra-DVS Motivation

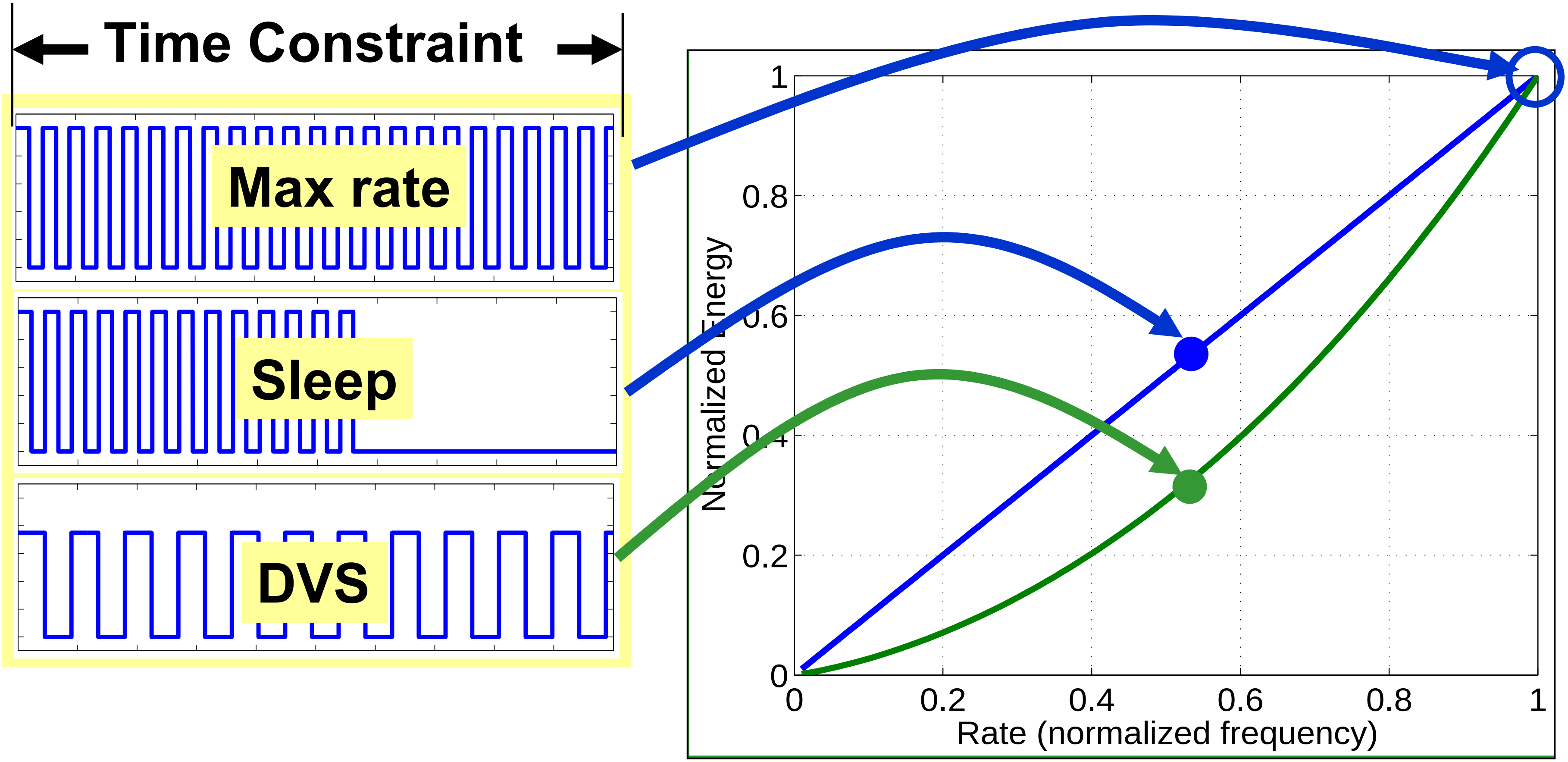
Strong Inversion Operation: fast, power-hungry



Unite the regions

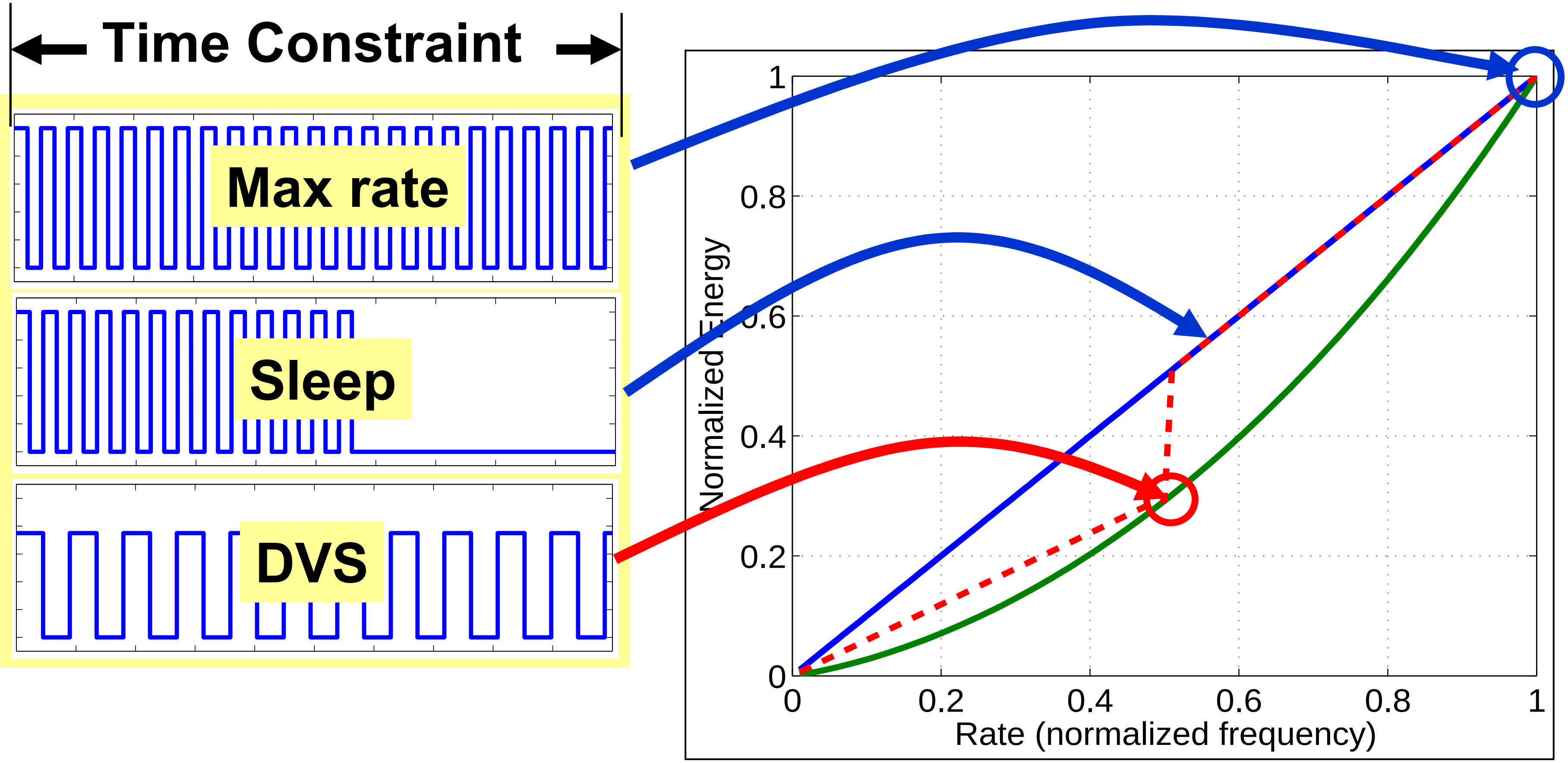
Sub-threshold operation: Slow, lower power, minimum energy operation becomes possible

Dynamic Voltage Scaling (DVS)



Dynamic Voltage Scaling with infinite levels saves energy per sample when the workload varies

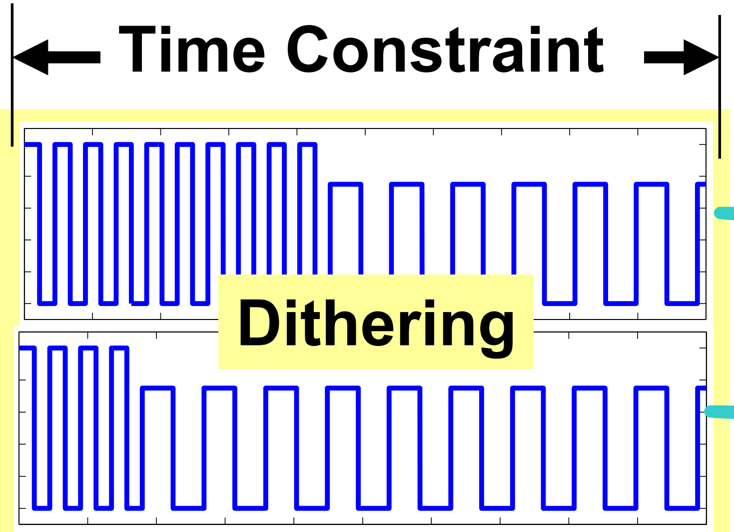
Quantized DVS

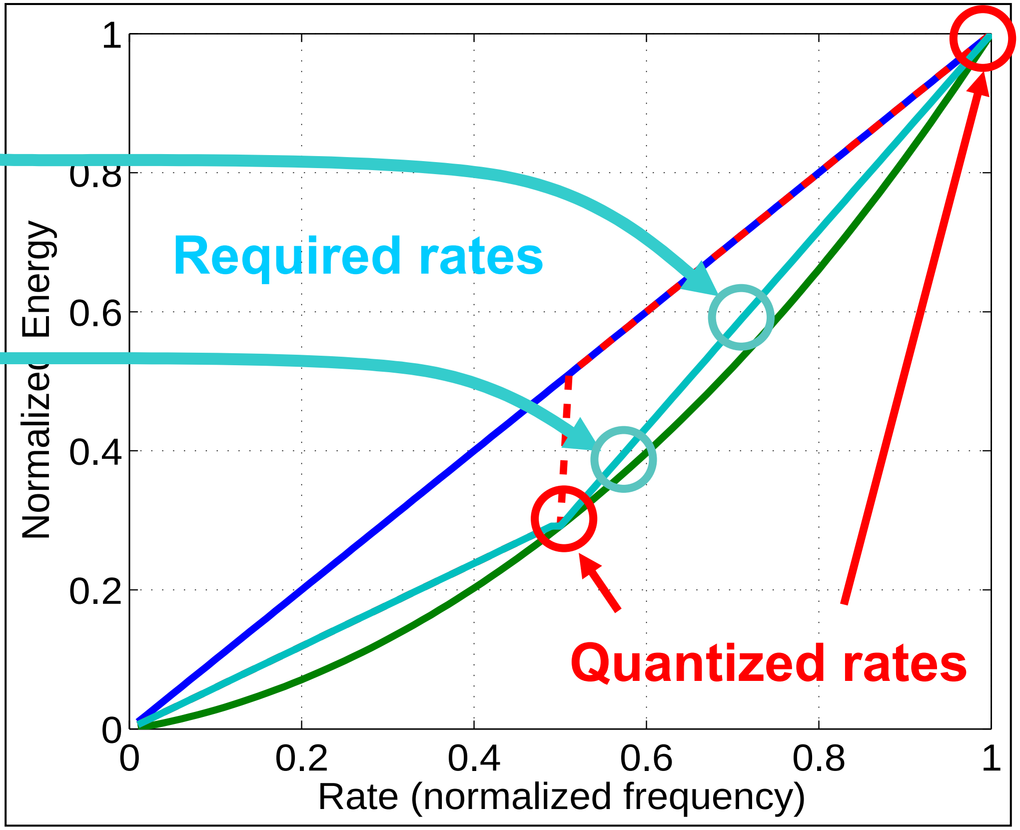


Quantizing the voltages decreases complexity, but reduces savings if V_{DD} is constant for time constraint

Gutnik and Chandrakasan, *An Efficient Controller for Variable Supply-Voltage Low Power Processing*, Symposium on VLSI Circuits, 1996

Voltage Dithering





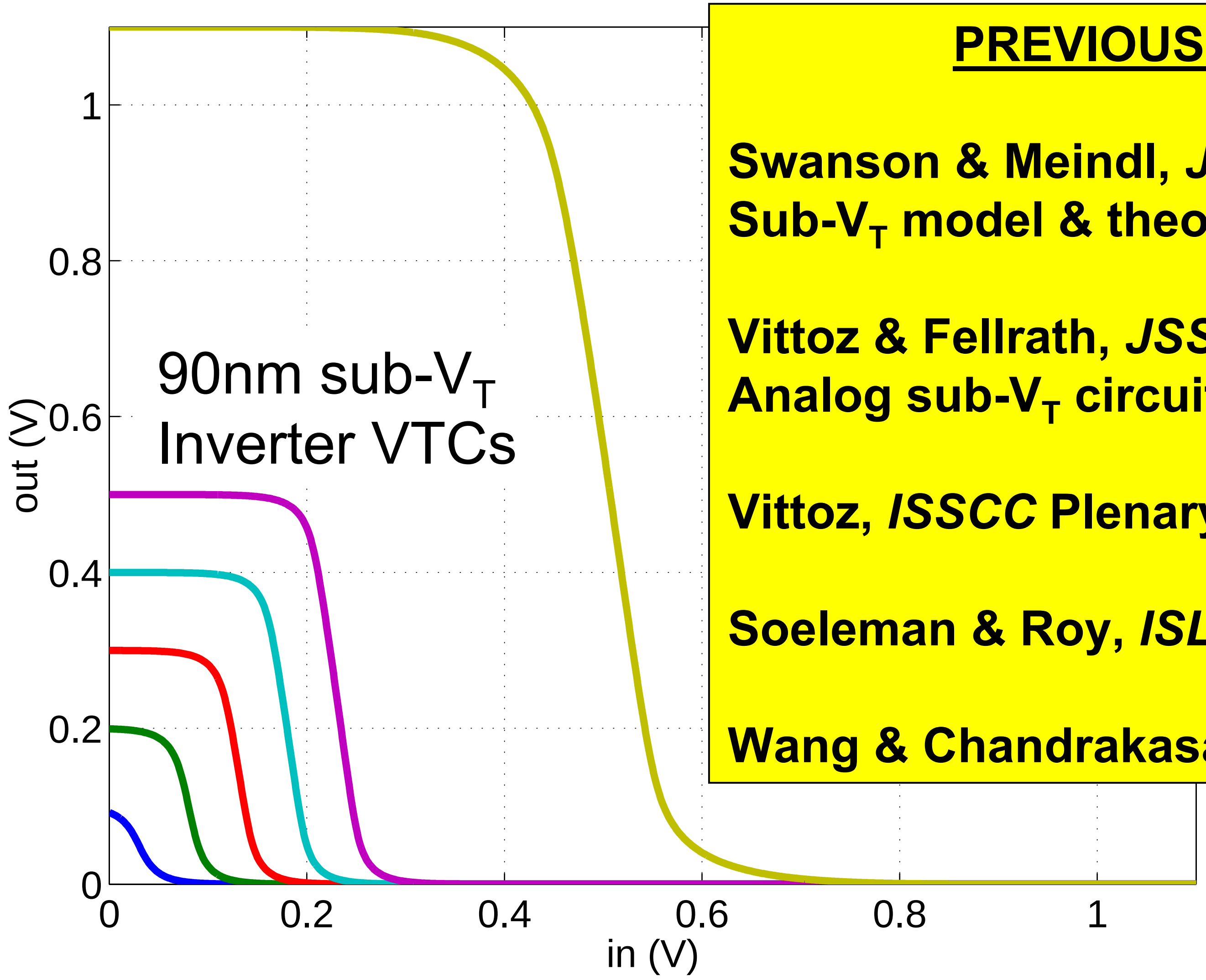
Need to switch V_{DD} in the timescale of the changing workload:

Existing approaches use 100s of μsecs to switch

Dithering within the time constraint gives average energy close to the optimum

Gutnik and Chandrakasan, *An Efficient Controller for Variable Supply-Voltage Low Power Processing*, Symposium on VLSI Circuits, 1996

Sub-V_T Operation



<u>PREVIOUS WORK</u>:

Swanson & Meindl, *JSSC*,1972
Sub-V_T model & theoretical limits

Vittoz & Fellrath, *JSSC*,1977
Analog sub-V_T circuits

Vittoz, *ISSCC* Plenary Talk, 1994

Soeleman & Roy, *ISLPED*, 1999

Wang & Chandrakasan, *ISSCC*, 2004

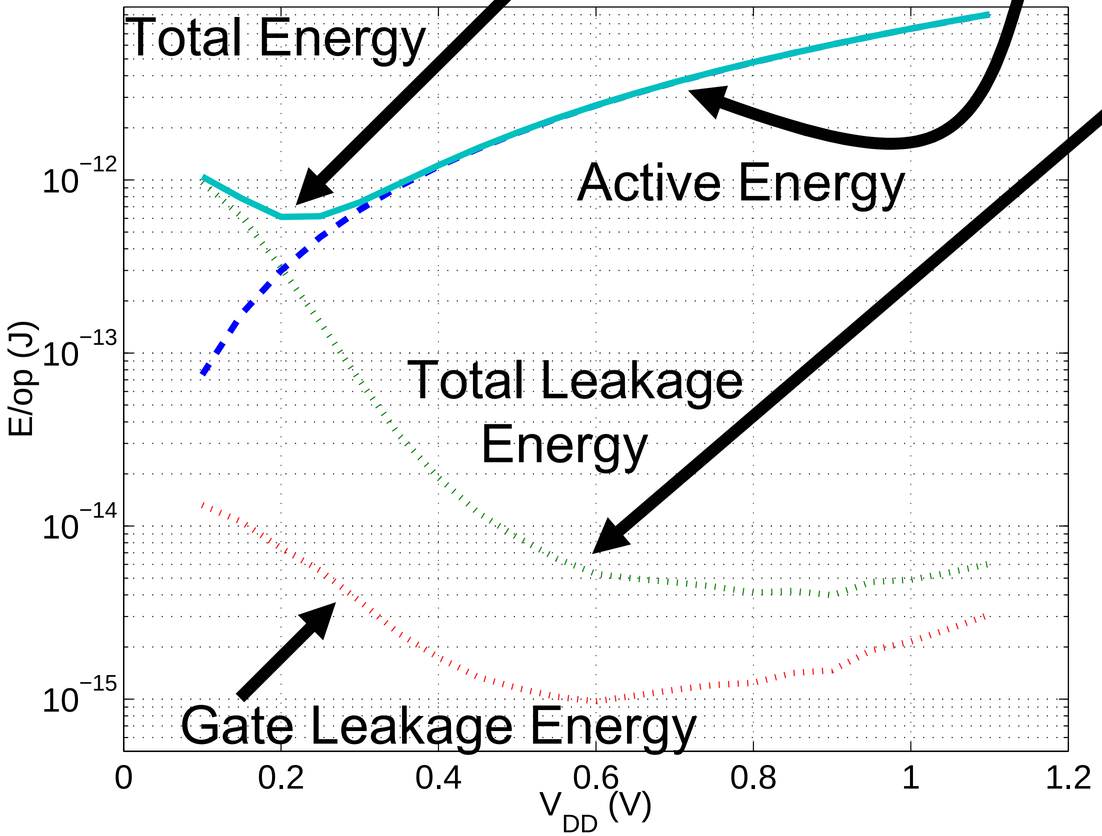
Sub-V_T Minimum Energy Operation

$$E_{TOTAL} = E_{ACTIVE} + E_{LEAKAGE}$$

$$E_{TOTAL} = C \cdot V_{DD}^2 + I_{OFF} V_{DD} T_D$$

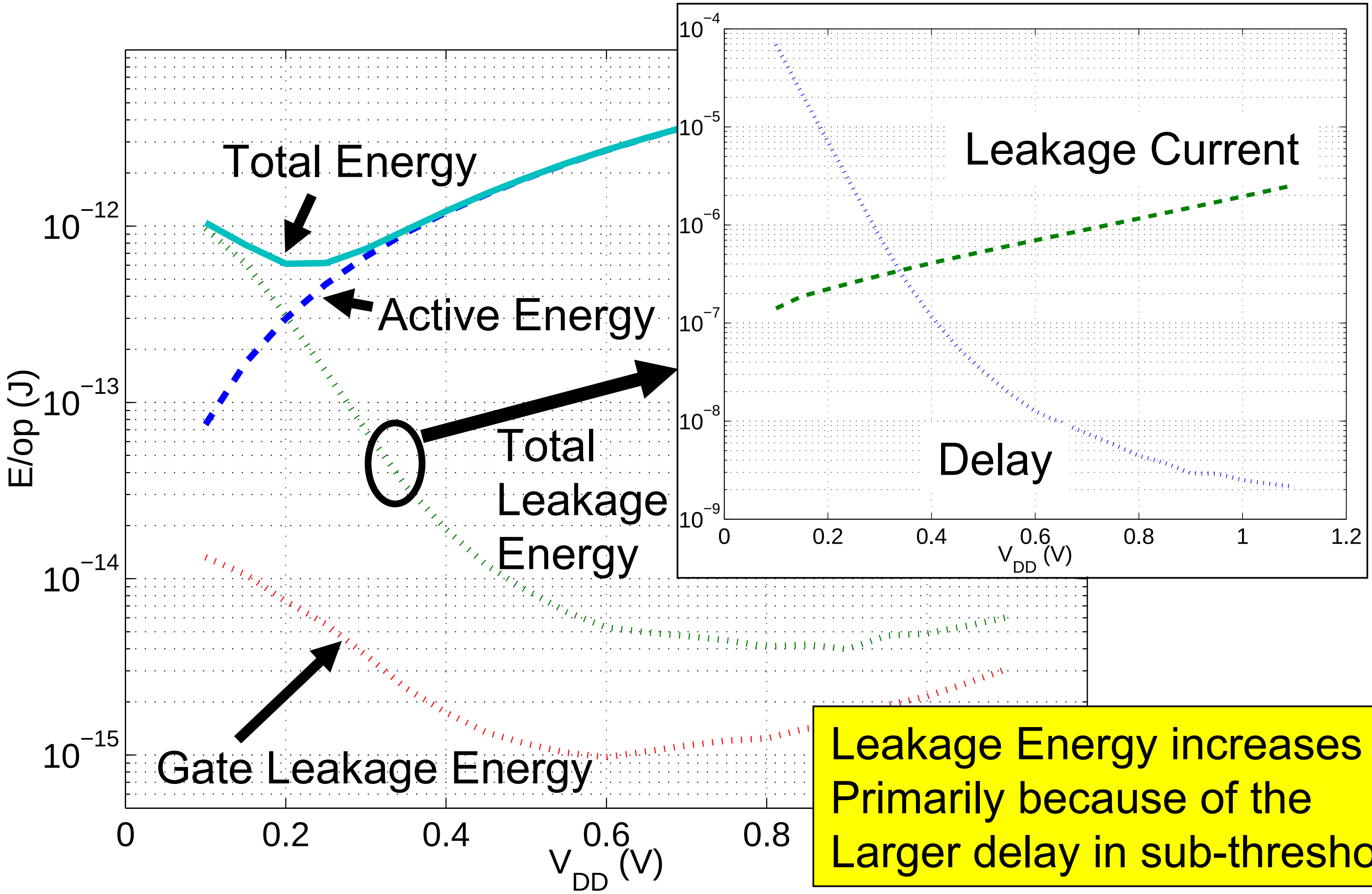
$$E_{Total} = C_{eff} V_{DD}^2 + W_{eff} L_{DP} K C_g V_{DD}^2 e^{-\frac{V_{DD}}{nV_{th}}}$$

$$= V_{DD}^2 \left(\underbrace{C_{eff}}_{} + \underbrace{W_{eff} K C_g L_{DP} e^{-\frac{V_{DD}}{nV_{th}}}}_{} \right)$$



90nm simulation
for 32-bit CLA adder
showing minimum
energy per operation

Reason for Min. Energy Point



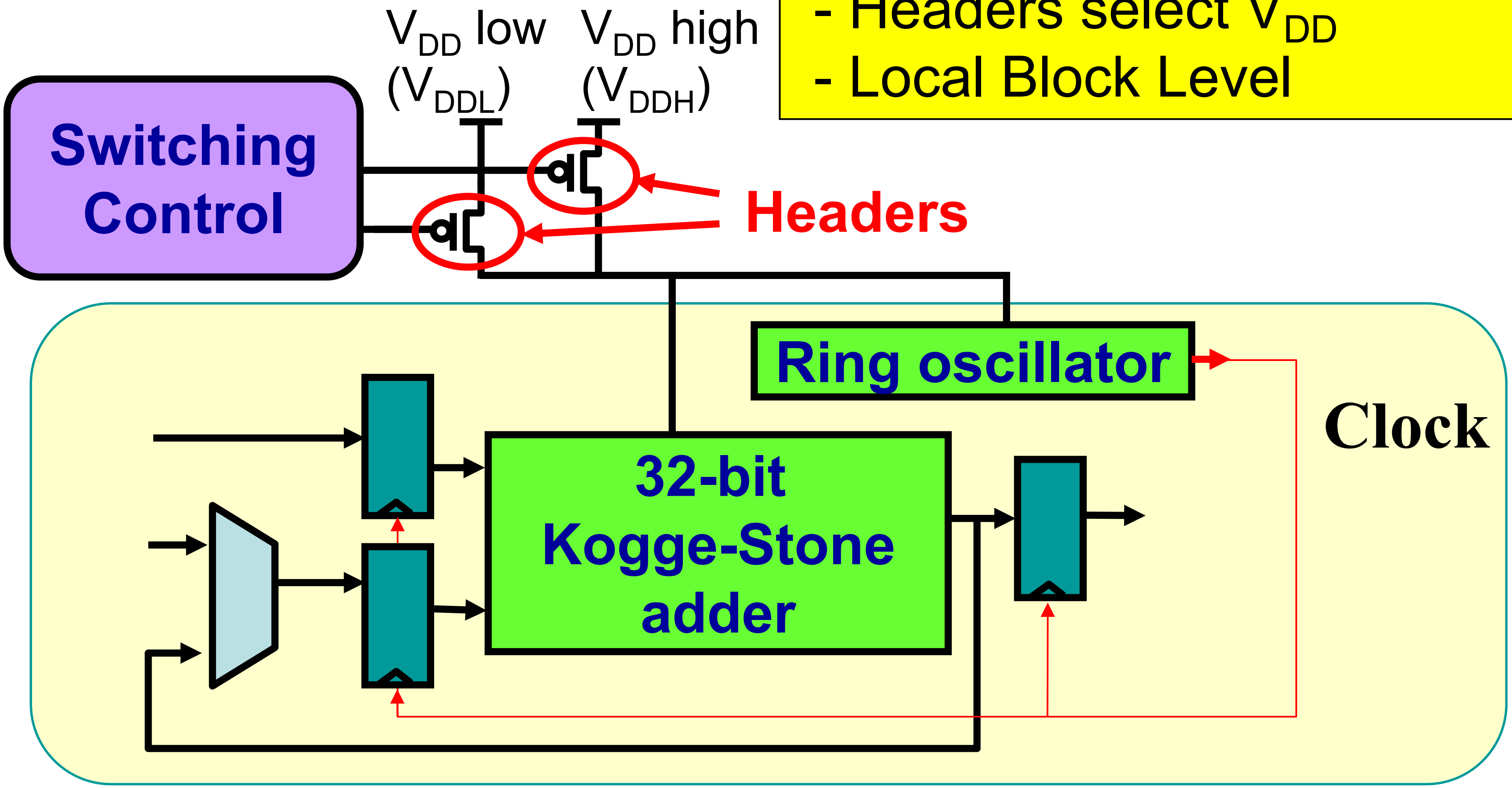
Leakage Energy increases Primarily because of the Larger delay in sub-threshold

Demonstrating UDVS

- Test chip to show combination of sub-threshold operation with DVS
  - Sub-threshold Circuit Considerations
  - Local Voltage Dithering (LVD)
  - Ultra-Dynamic Voltage Scaling

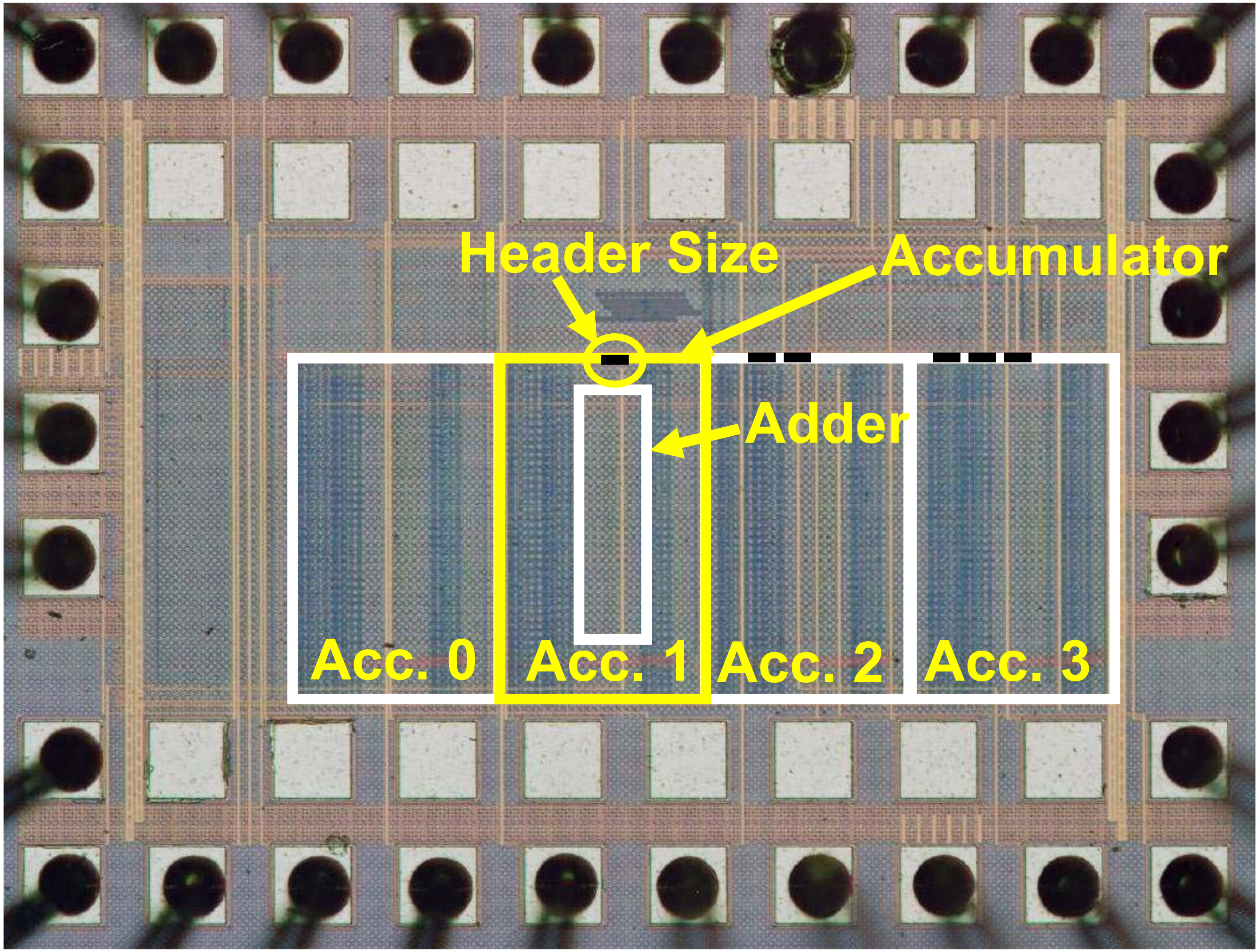
90nm Test Chip Circuit

Local Voltage Dithering (LVD)
- Headers select V_{DD}
- Local Block Level

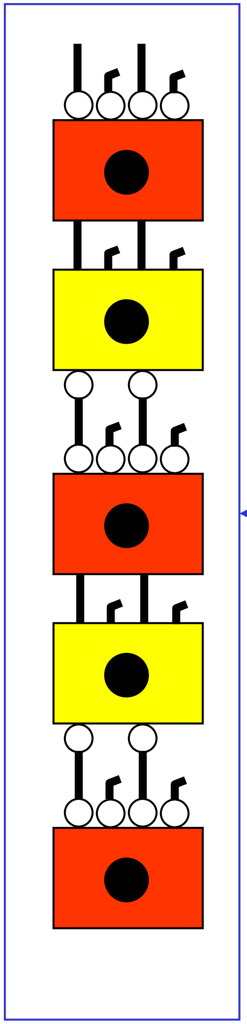


Test Chip Die Photo

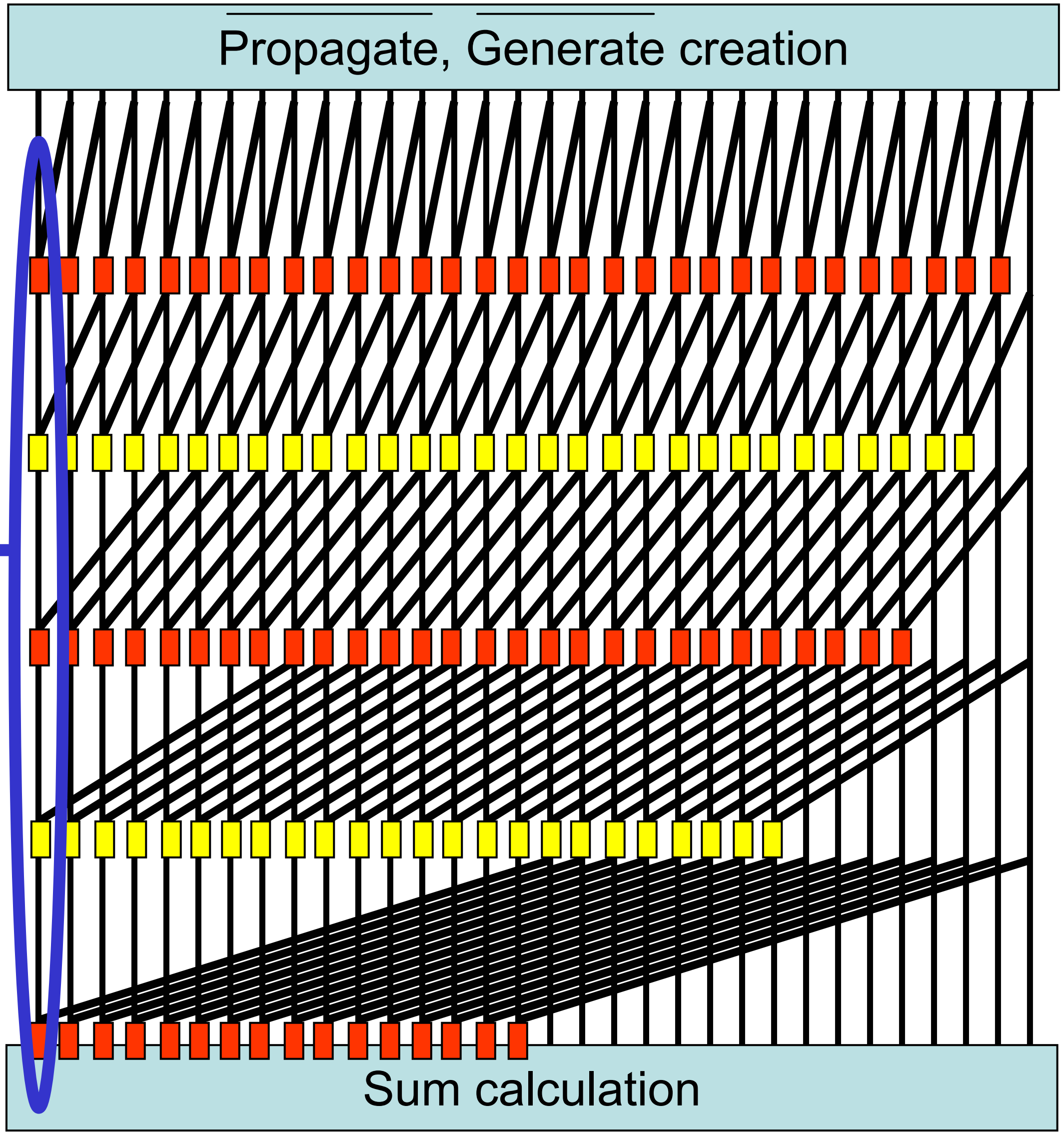
90nm
6LM



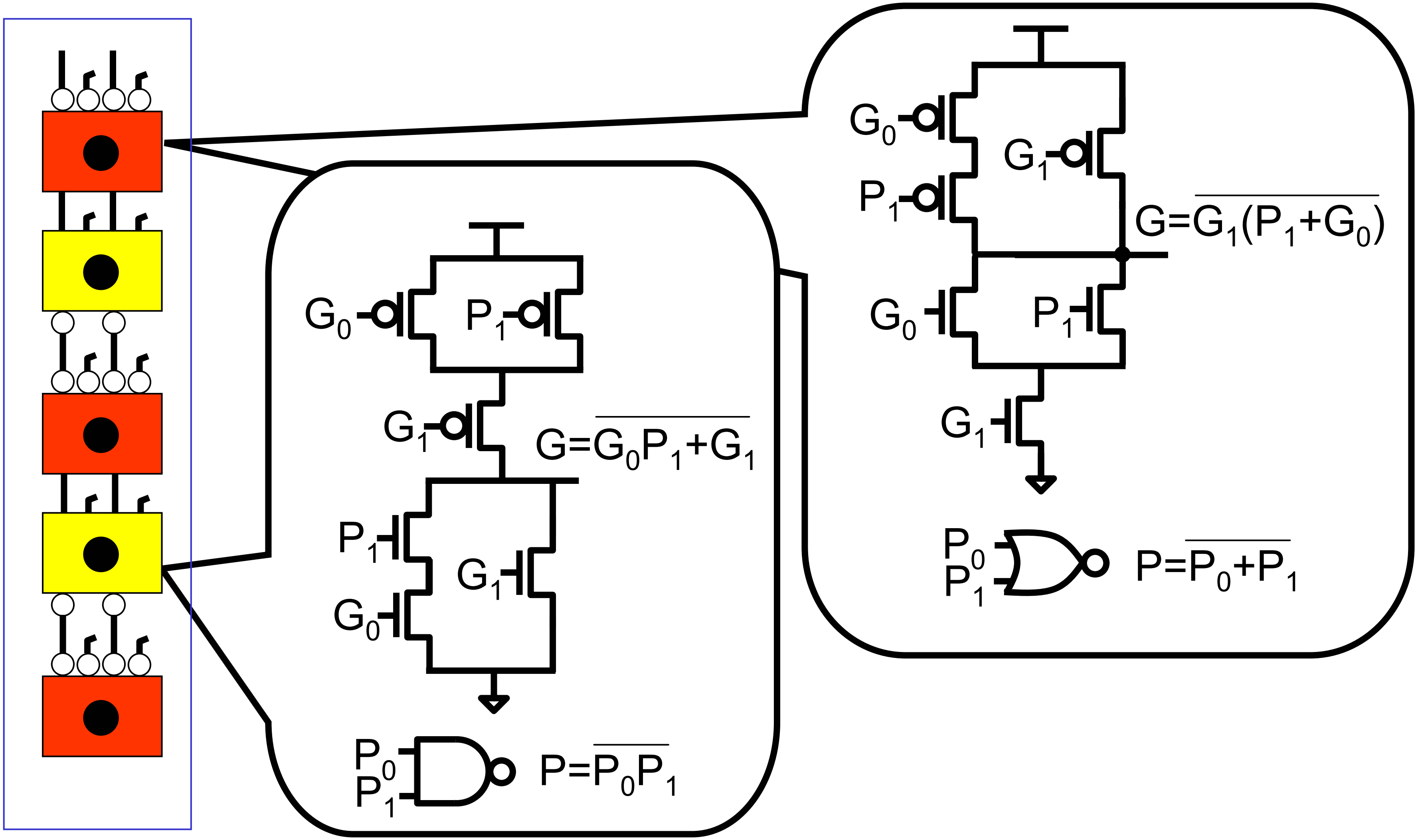
32-bit Kogge-Stone Adder Block



Path through adder tree has inverting stages of dot operators



Kogge-Stone Adder Circuits



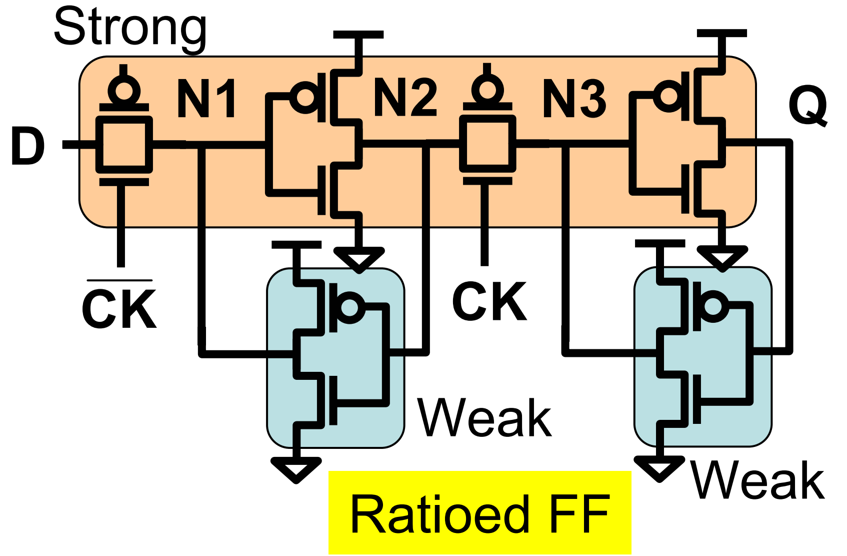
$G=\overline{G_0P_1+G_1}$

$P=\overline{P_0P_1}$

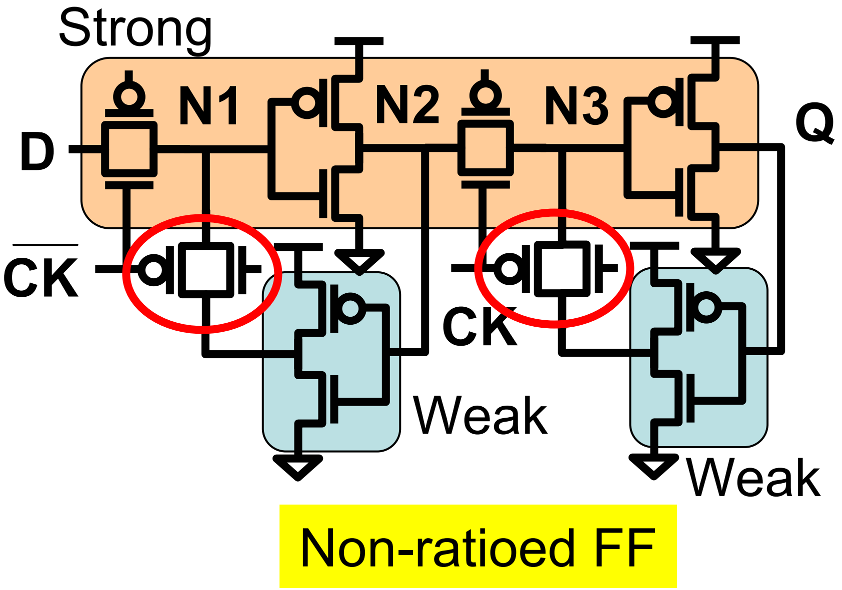
$G=\overline{G_1(P_1+G_0)}$

$P=\overline{P_0+P_1}$

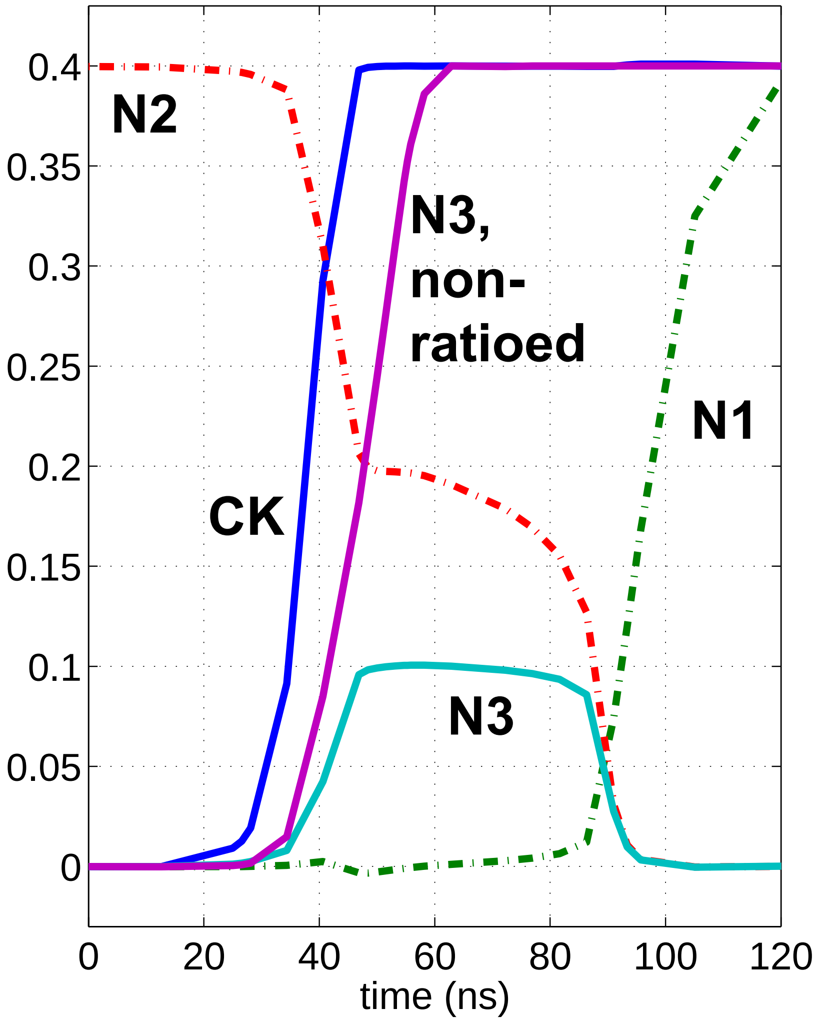
Sub-V_T Sizing Considerations



Ratioed FF

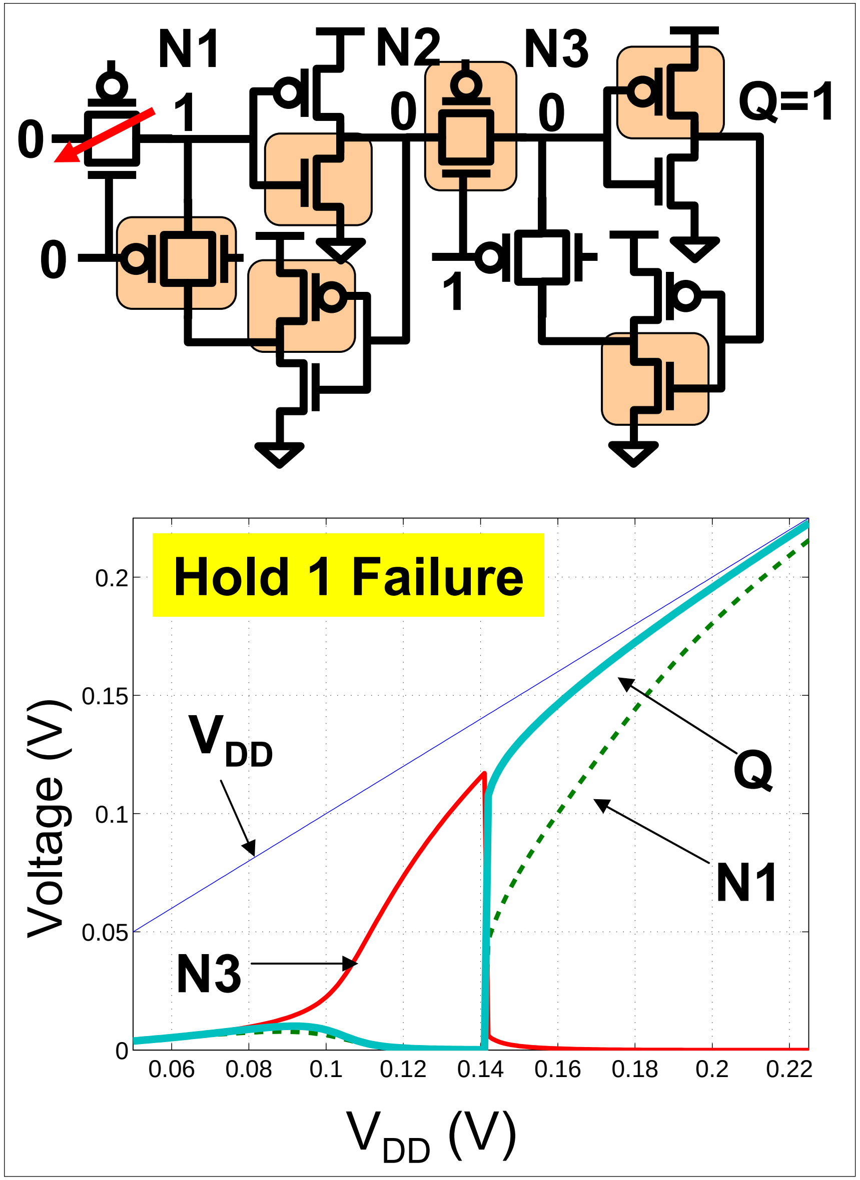


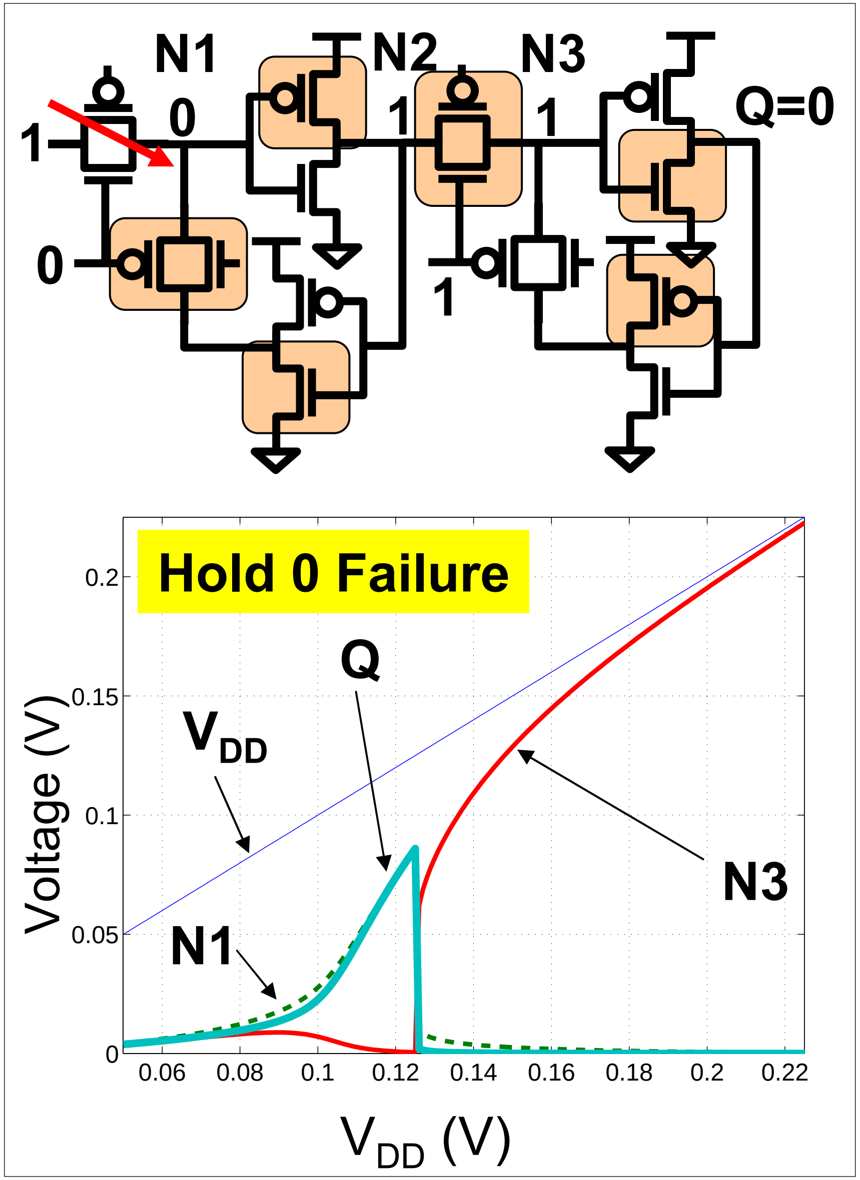
Non-ratioed FF



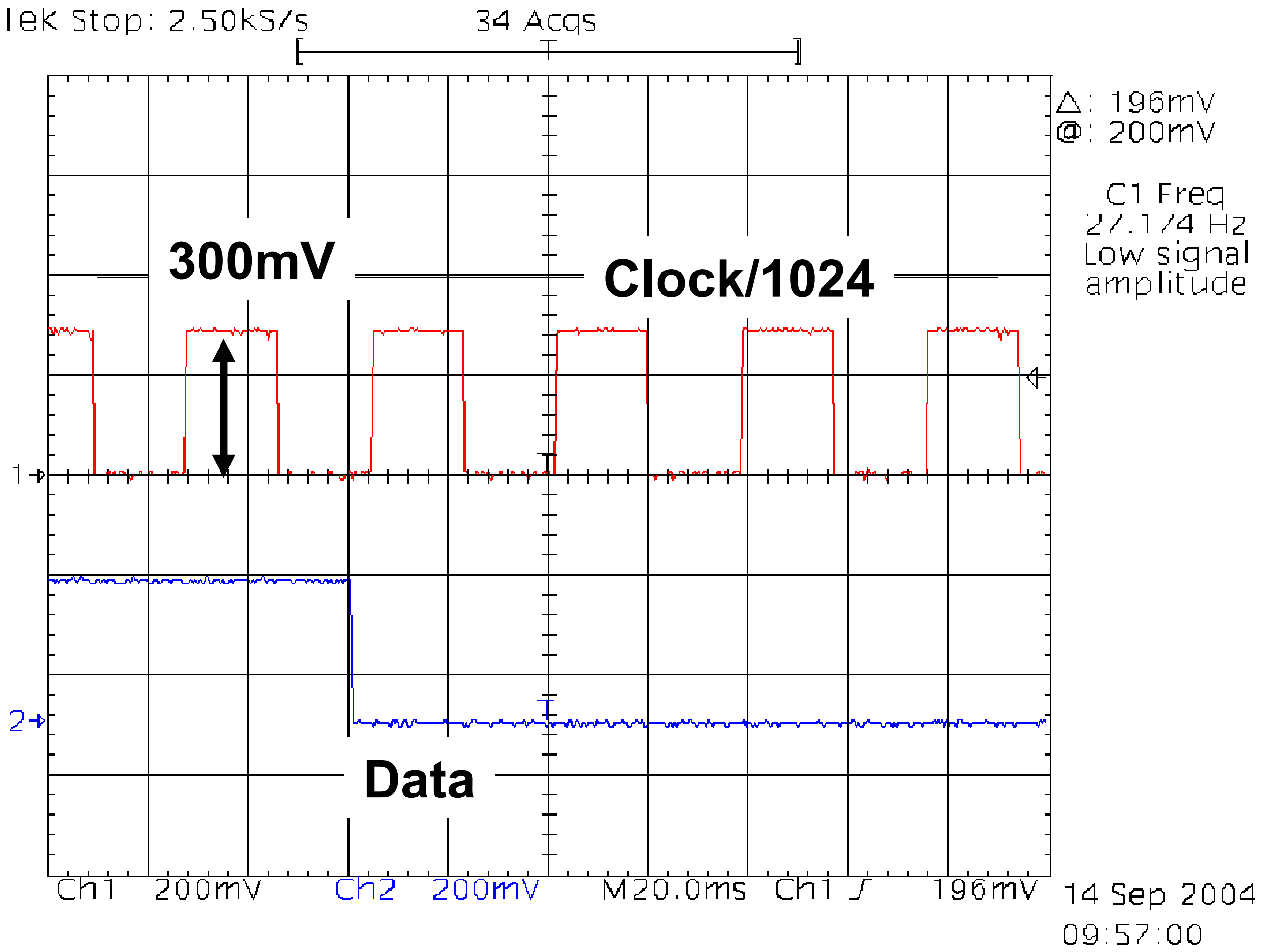
Ratioed FF fails to write a 1 at strong N, weak P corner at 400mV

Preserving State in Sub-V_T





Measured Sub-V_T Operation

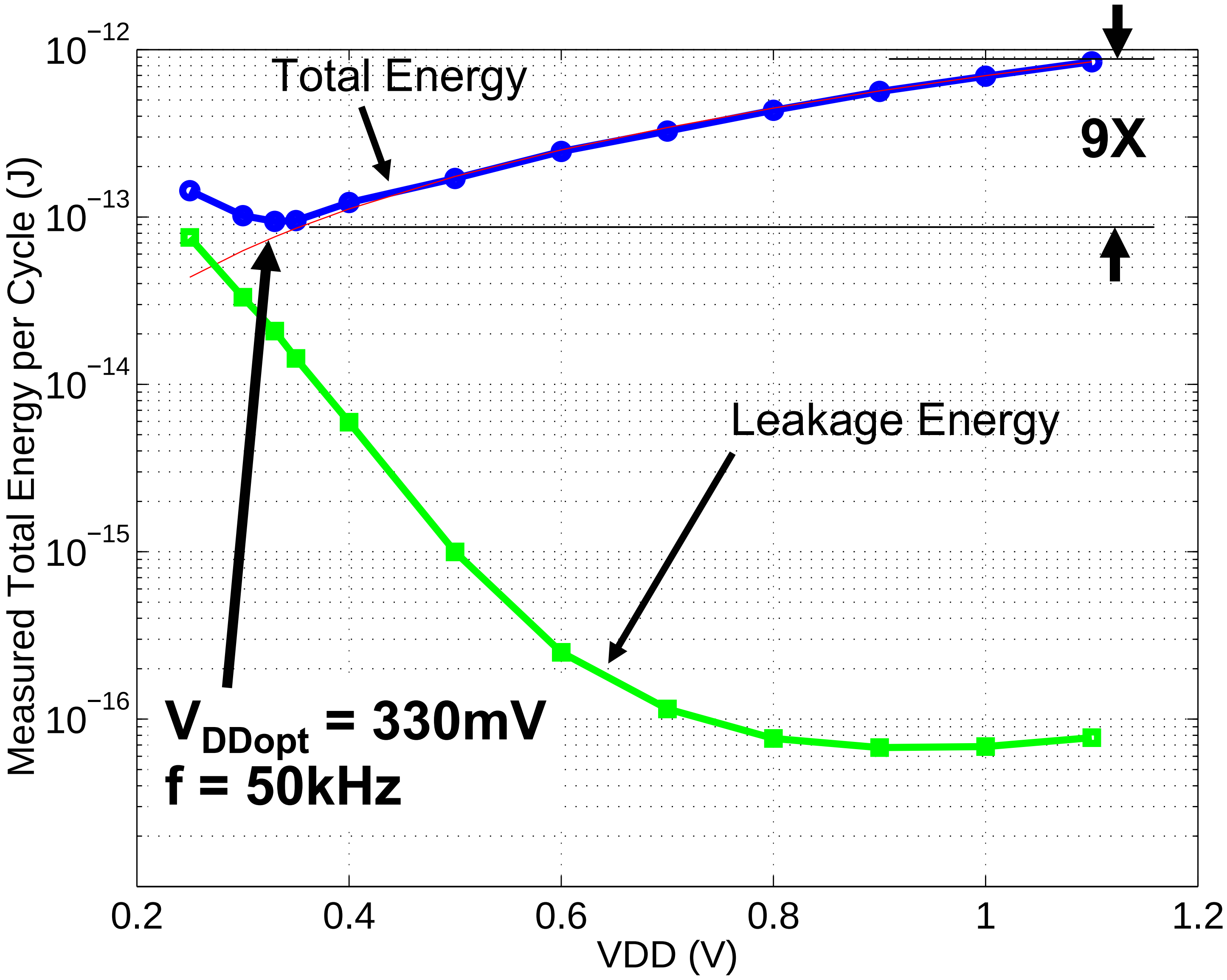


300mV

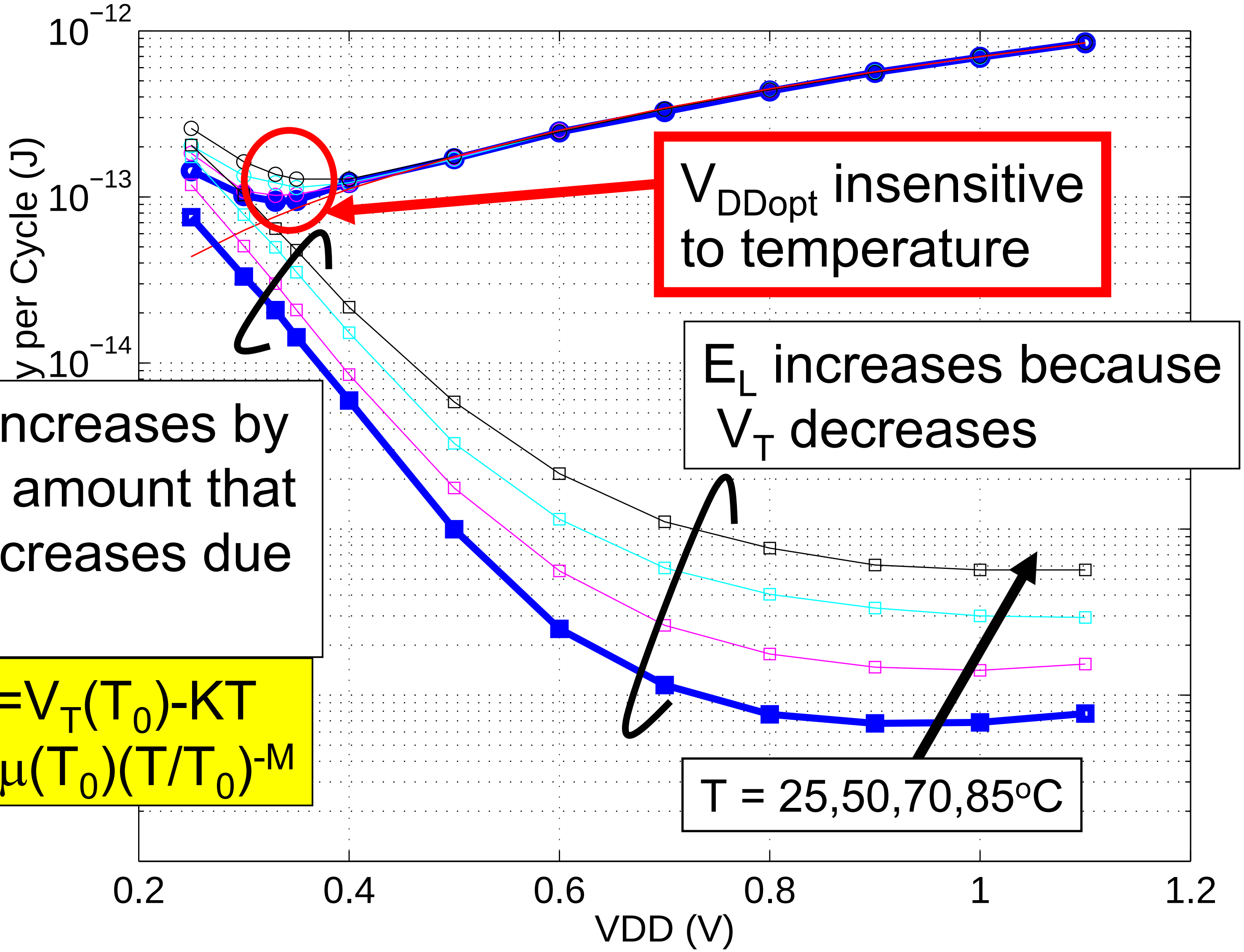
Clock/1024

Data

Minimum Energy Measurements



Minimum Energy & Temperature



V_{DDopt} insensitive to temperature

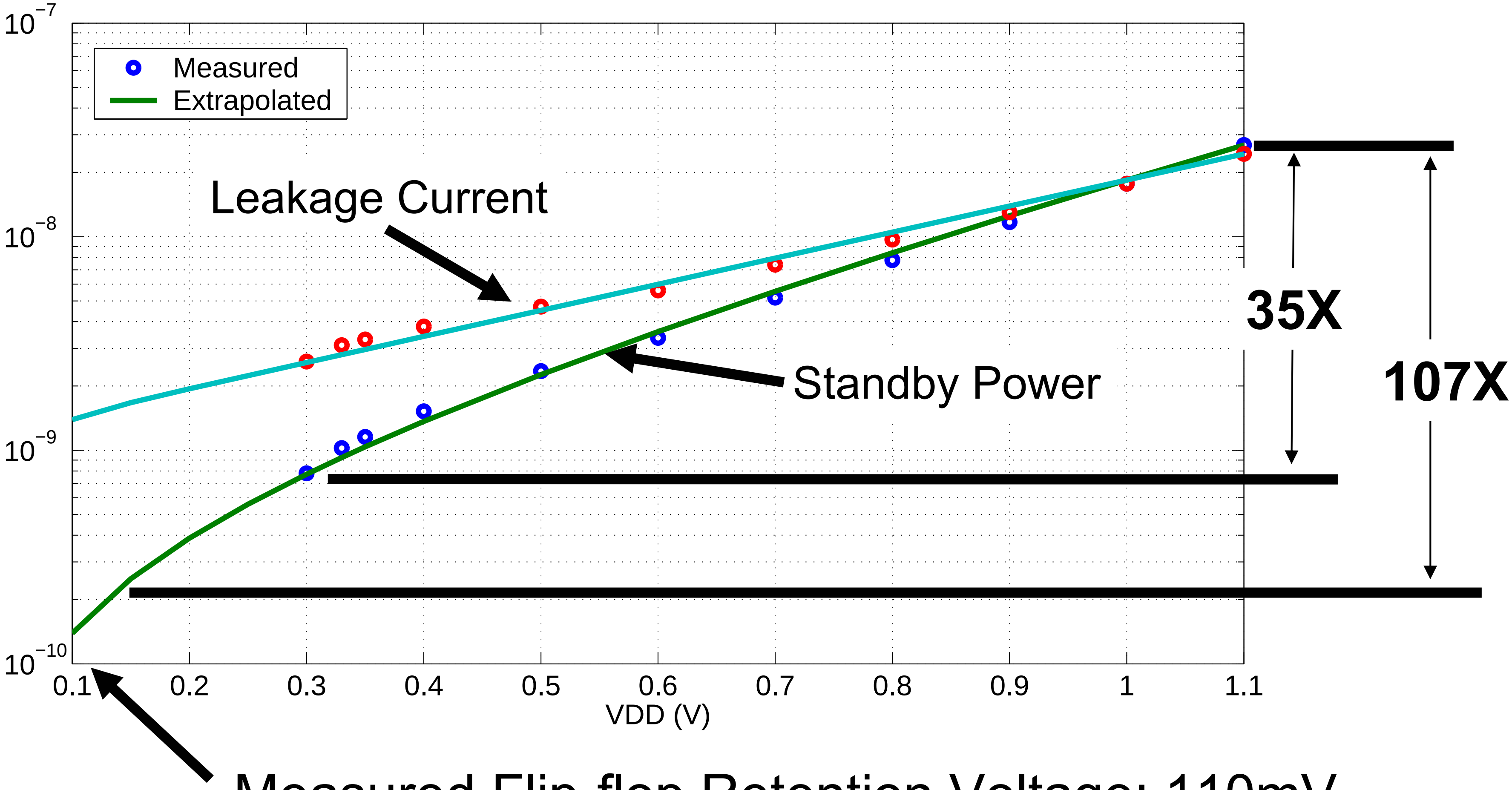
E_L increases because V_T decreases

I_{LEAK} increases by same amount that T_D decreases due to V_T

$V_T(T)=V_T(T_0)-KT$
$\mu(T)=\mu(T_0)(T/T_0)^{-M}$

T = 25,50,70,85°C

Measured Standby Power Savings



Leakage Current

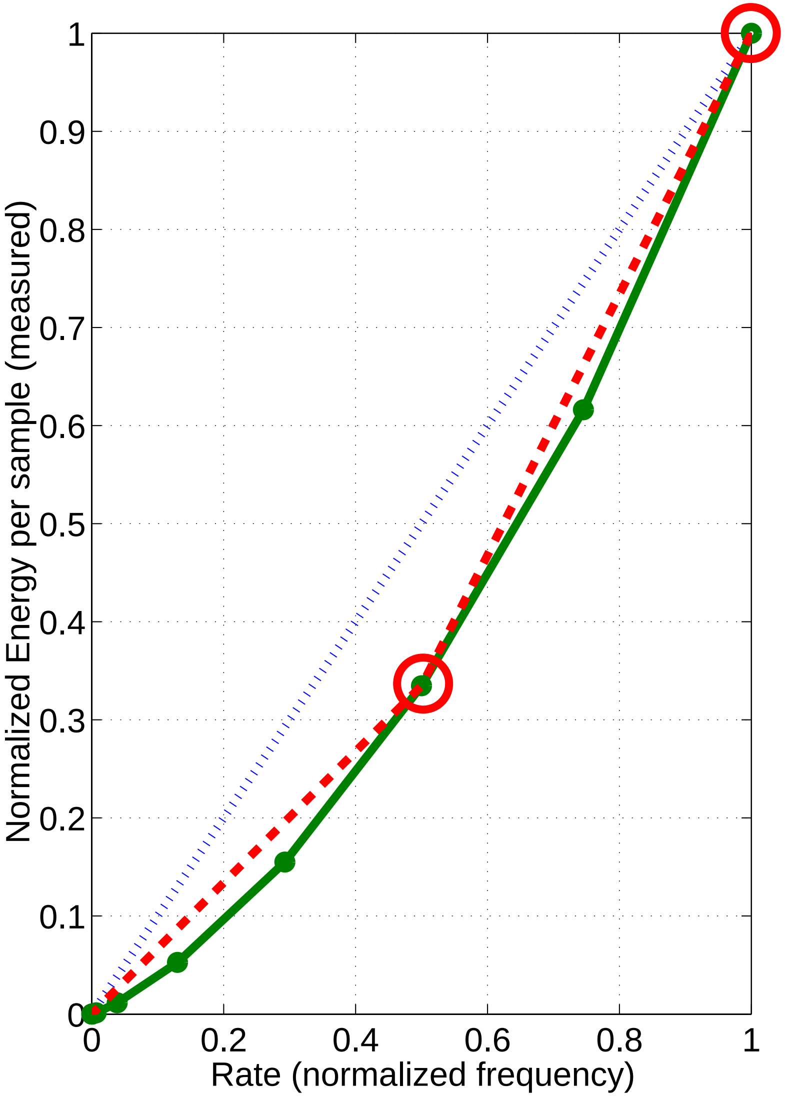
Standby Power

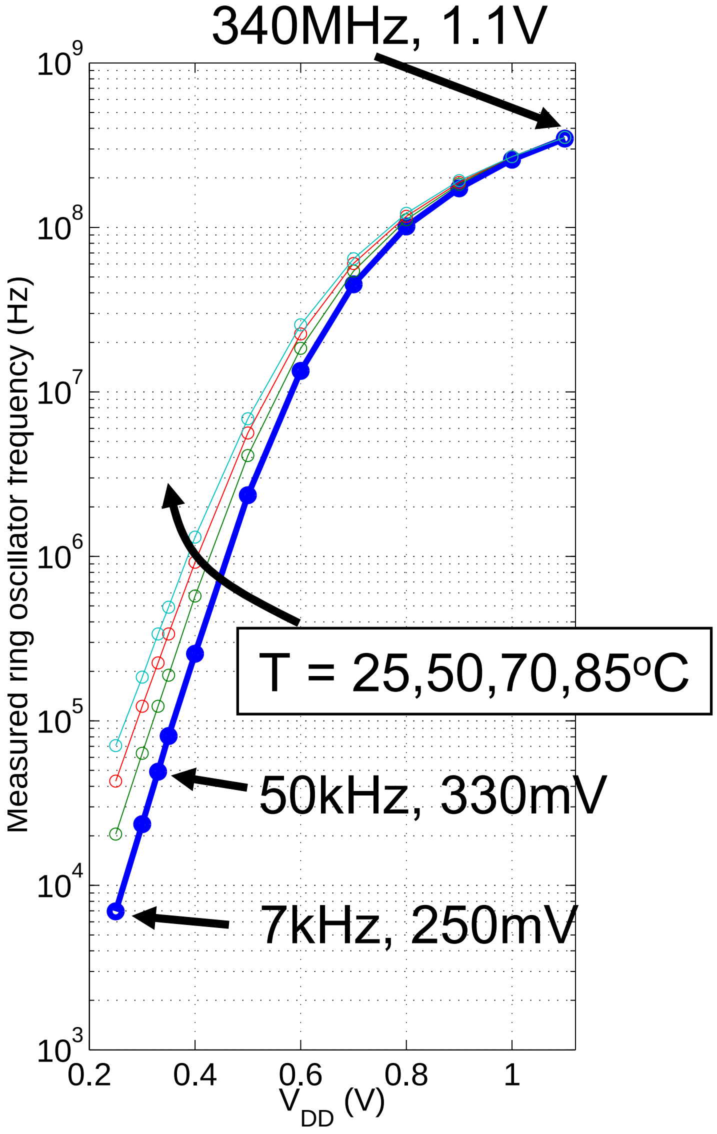
35X

107X

Measured Flip-flop Retention Voltage: 110mV

Local Voltage Dithering (LVD)



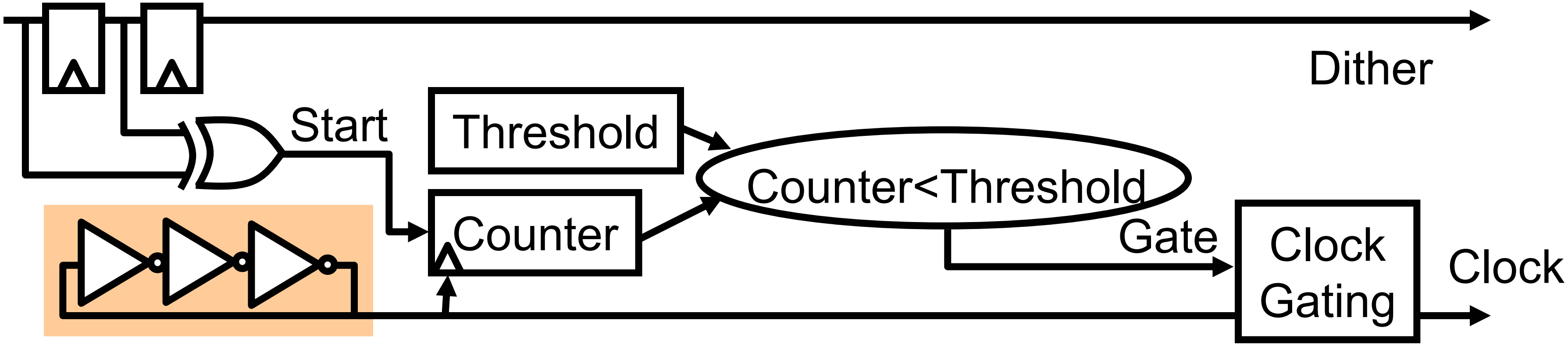

340MHz, 1.1V

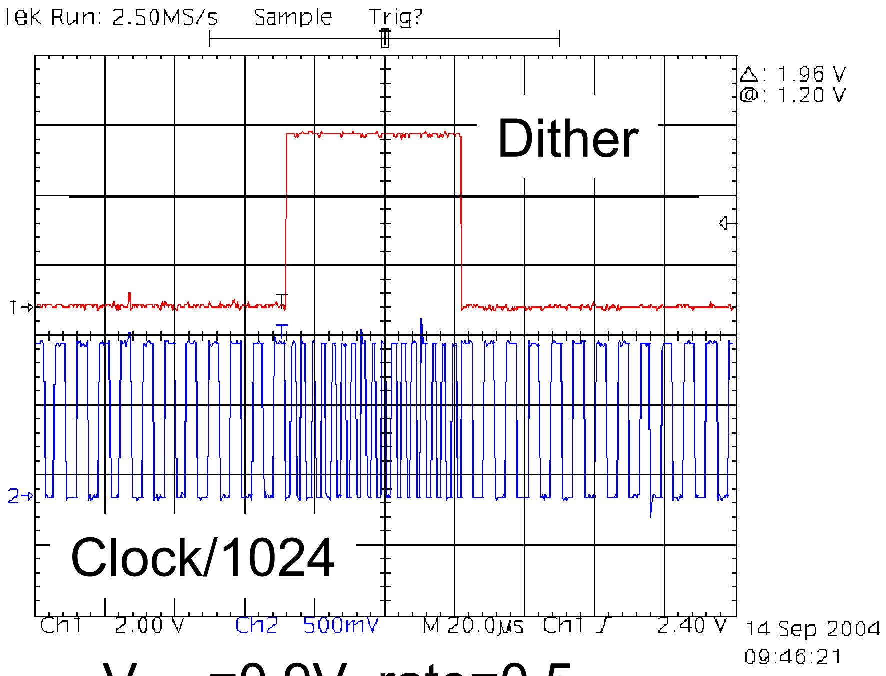
T = 25,50,70,85^{o}C

50kHz, 330mV

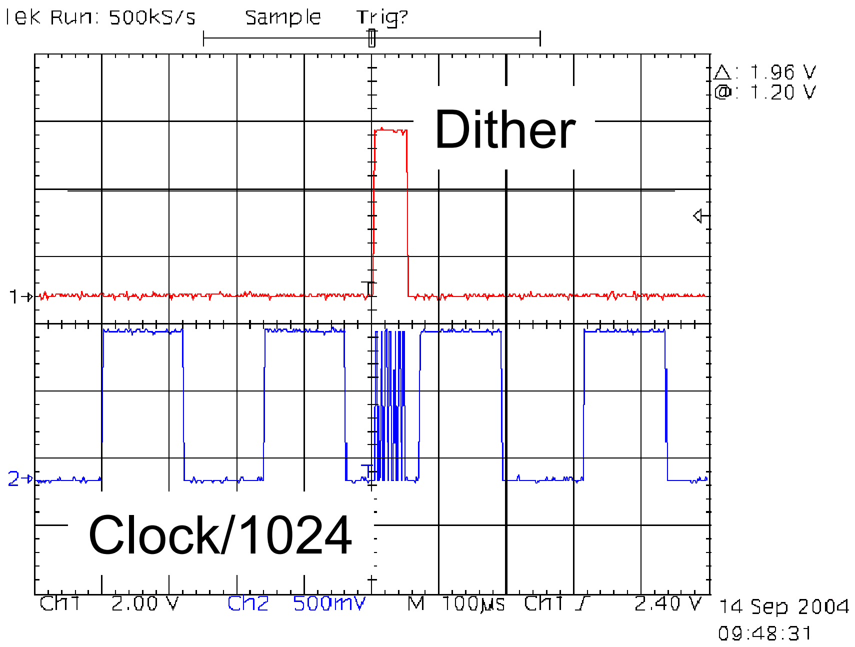
7kHz, 250mV

Timing Overhead for LVD



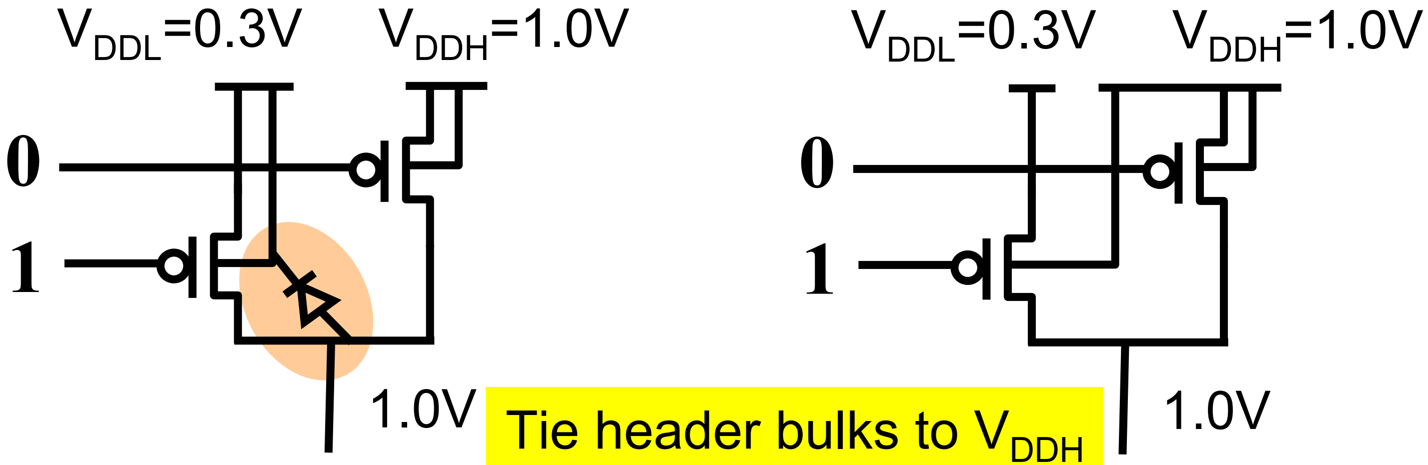


V_{DDL}=0.9V, rate=0.5



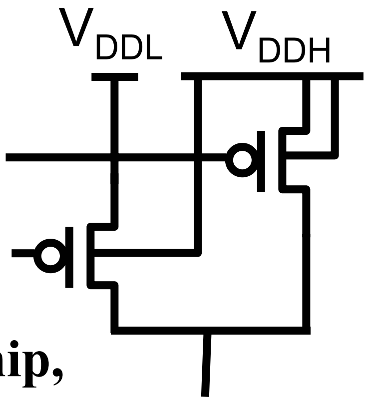
V_{DDL}=0.6V, rate=0.04

LVD Circuit Issues



Tie header bulks to V_{DDH}

Switching Energy



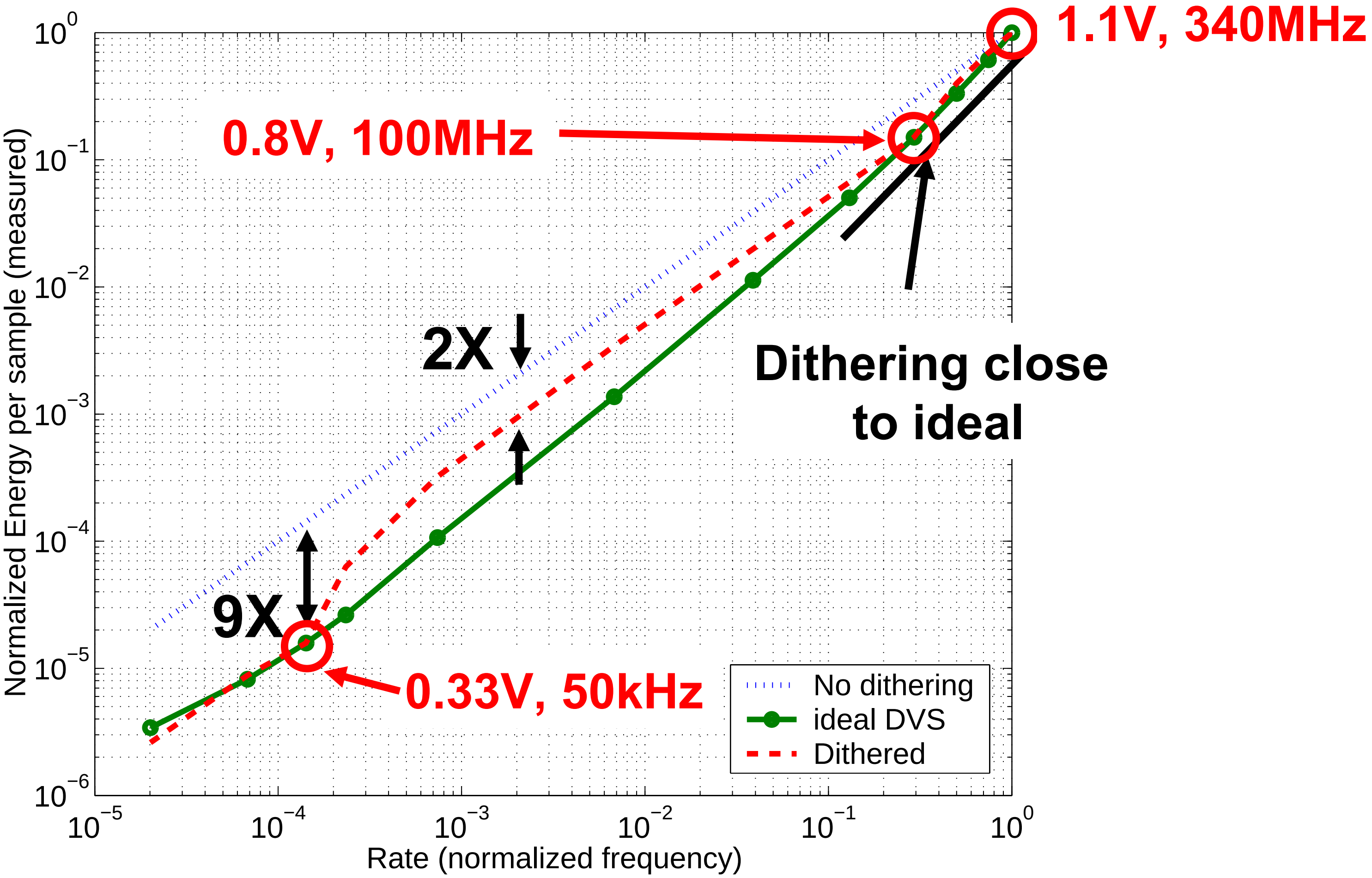
For test chip, C_{NORM}=3.7

C_{NORM} normalizes E_{SW} to E of circuit at V_{DDH}

N is number of cycles spent at V_{DDL} to break-even: $NV_{DDH}^2 \geq NV_{DDL}^2 + C_{NORM}V_{DDH}^2$

$$N \geq \frac{C_{NORM}V_{DDH}^2}{(V_{DDH}^2 - V_{DDL}^2)}$$

UDVS Results



1.1V, 340MHz

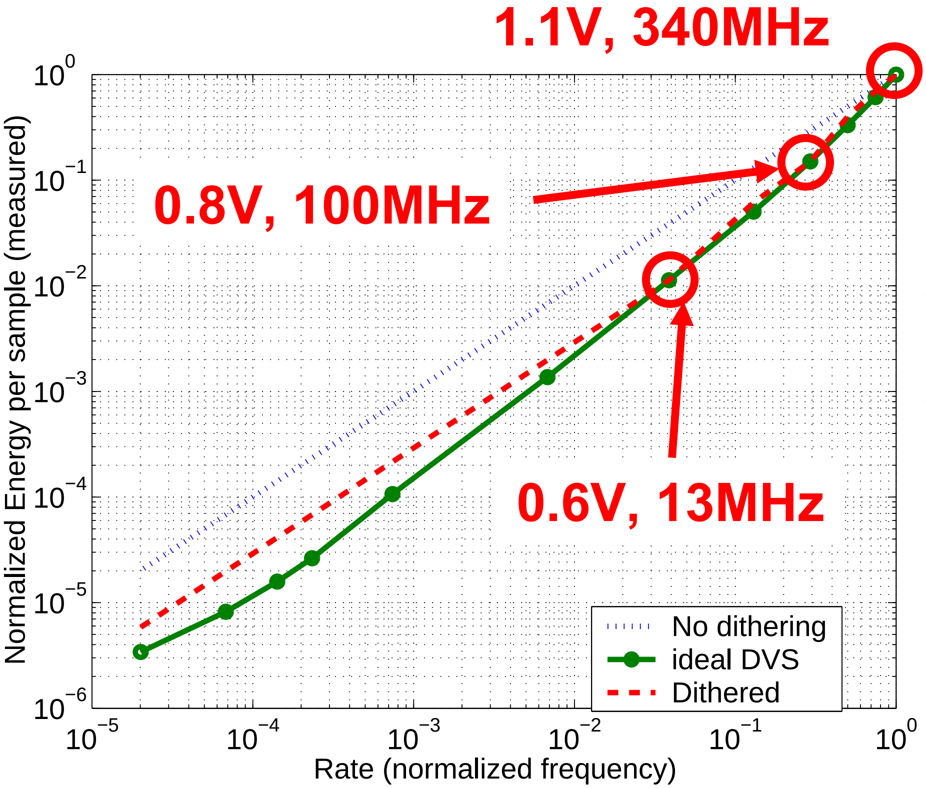
0.8V, 100MHz

0.33V, 50kHz

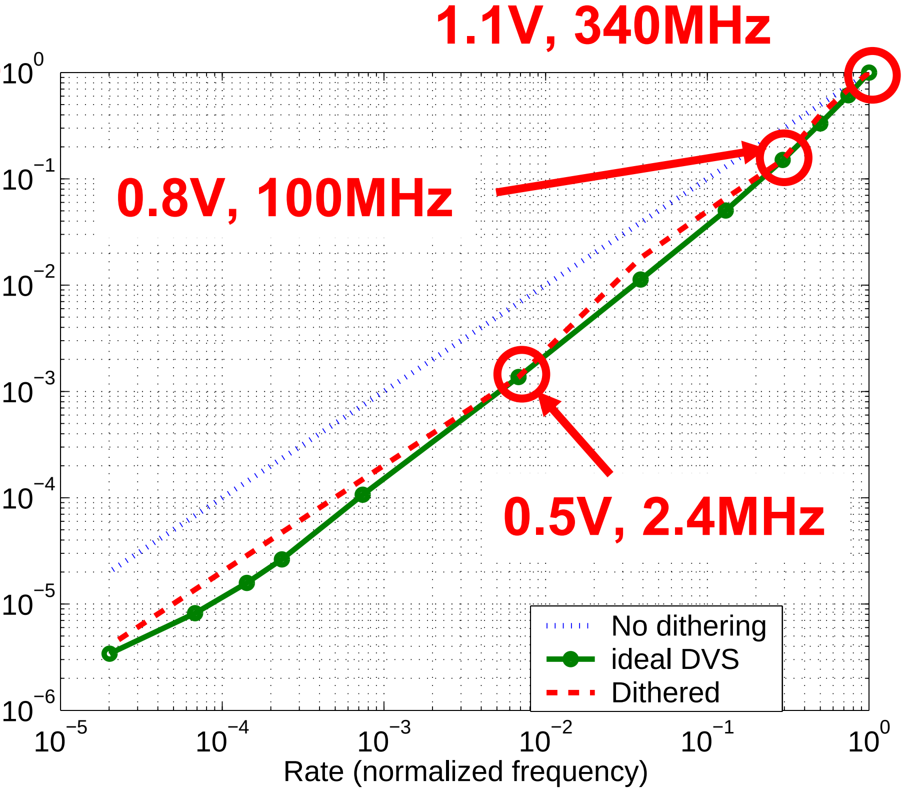
Dithering close to ideal

Dither during high performance operation and switch to sub-threshold minimum energy operation when speed is not important

UDVS Flexibility



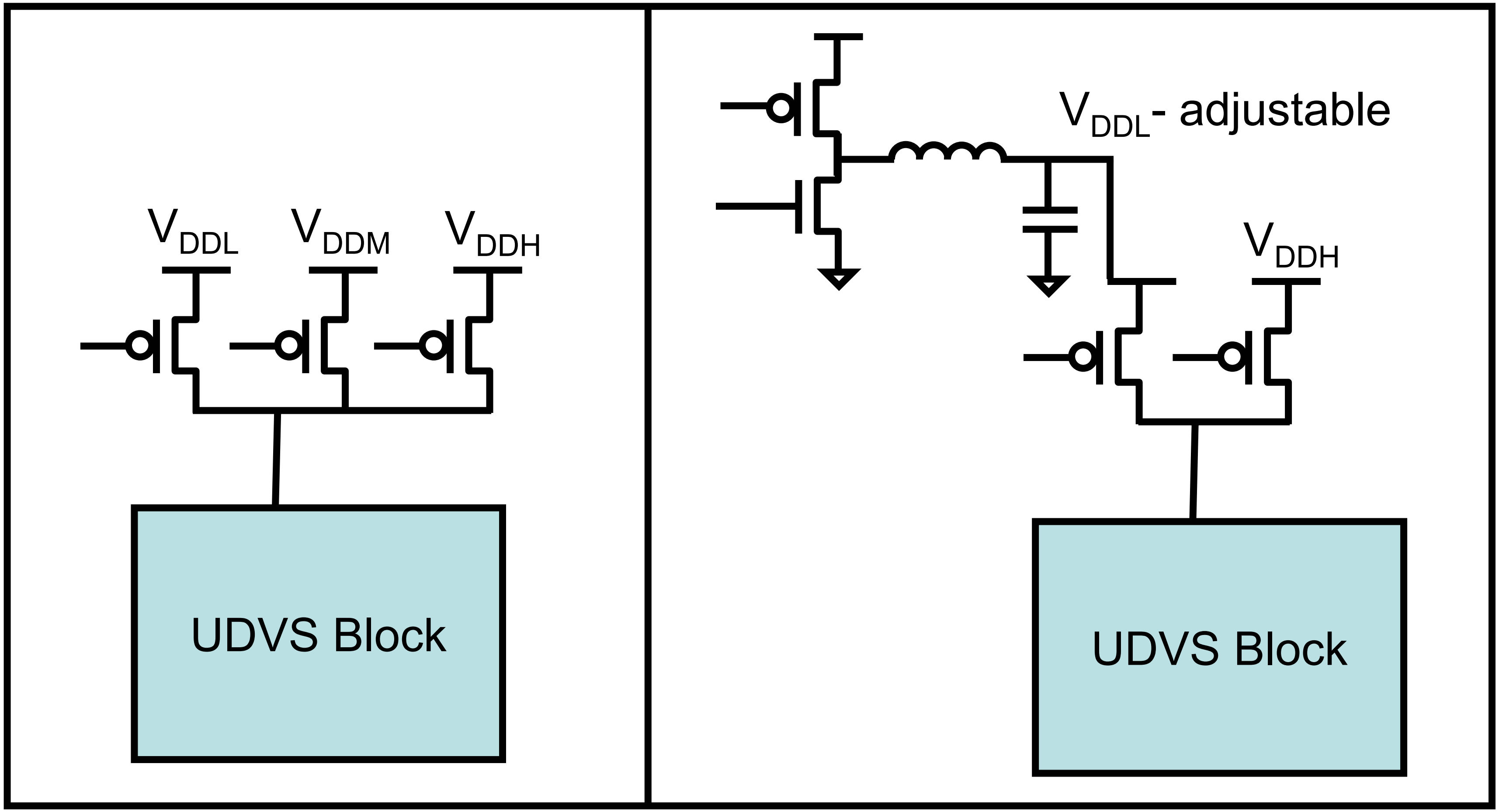
Closer to ideal over high performance range



Closer to ideal over full range

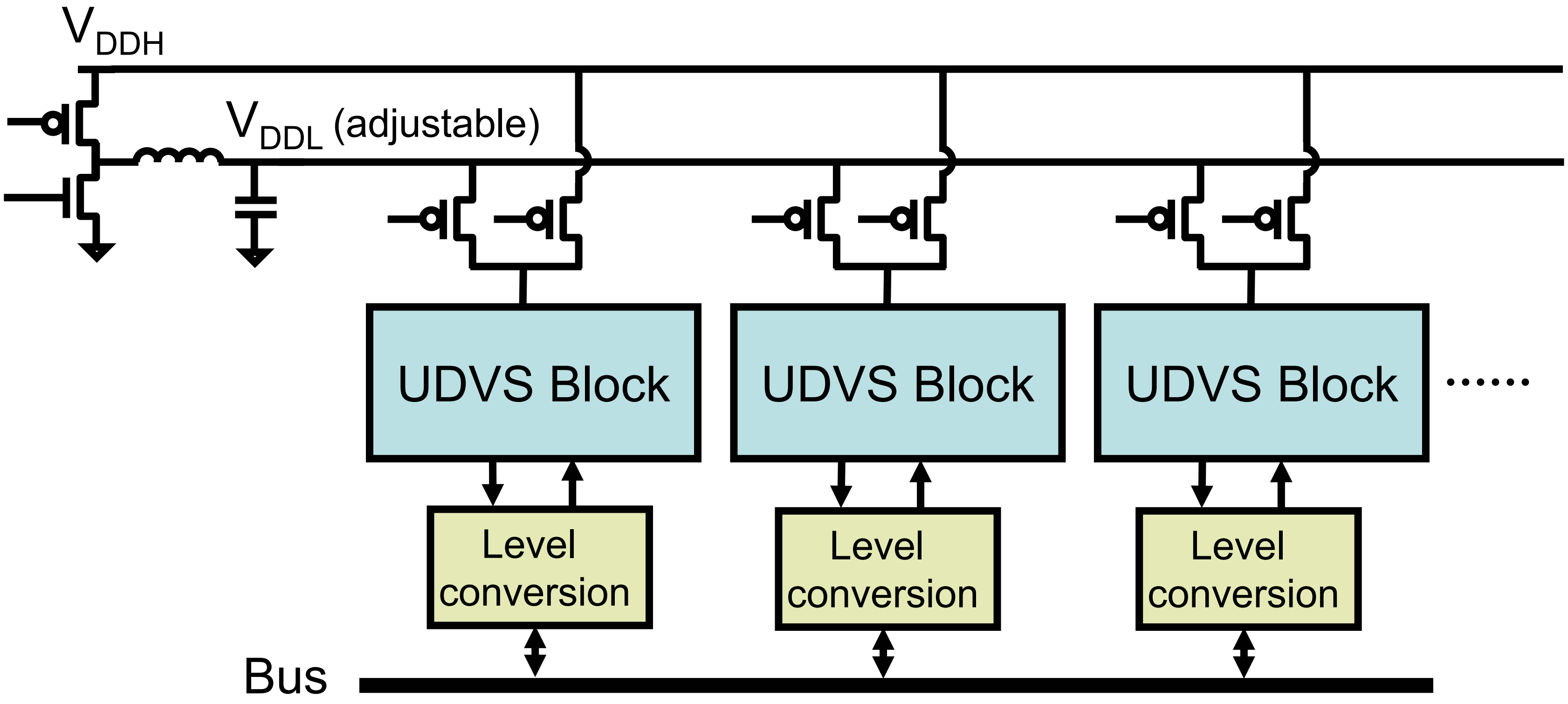
Choose dithered voltages to match application of interest

Providing UDVS Voltages



Can implement UDVS with 3 headers OR two headers and an adjustable voltage supply

UDVS System Example



Different blocks can voltage dither based on their own workload for optimal efficiency

Conclusions

- Local voltage dithering allows near-optimum savings for high performance, variable rate systems
- Sub-threshold allows minimum energy operation
- UDVS allows performance and energy scaling over the full operational range of V_{DD}

Acknowledgements: Funded by Texas Instruments and DARPA through a subcontract with MIT Lincoln Labs