A 256kb Sub-threshold SRAM in 65nm CMOS

by

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Benefits of Sub-threshold

- Sub-threshold benefits: V_{DD} from [1.8,1.0]V to [0.4,0.2]V

Leakage Power ↓ : P=VI

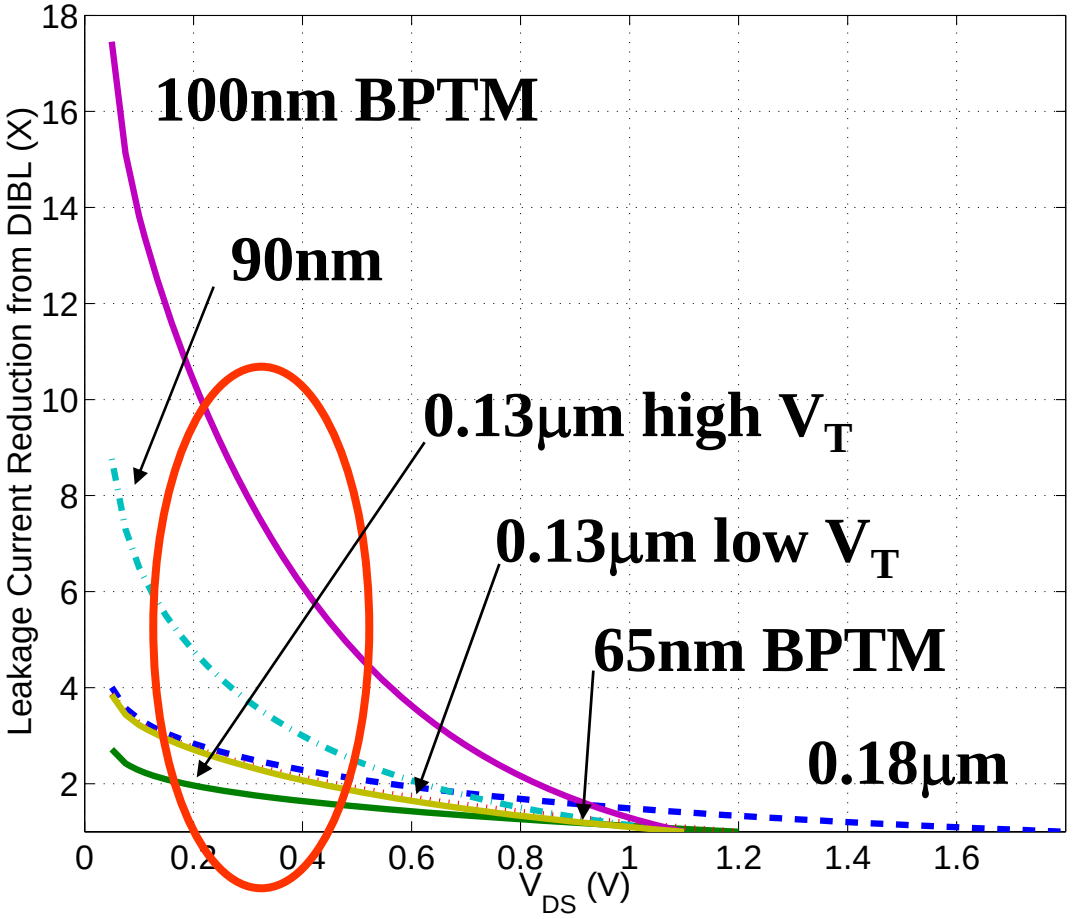
V_{DD} gives: 2.5X to 9X

DIBL gives: 2X to 10X

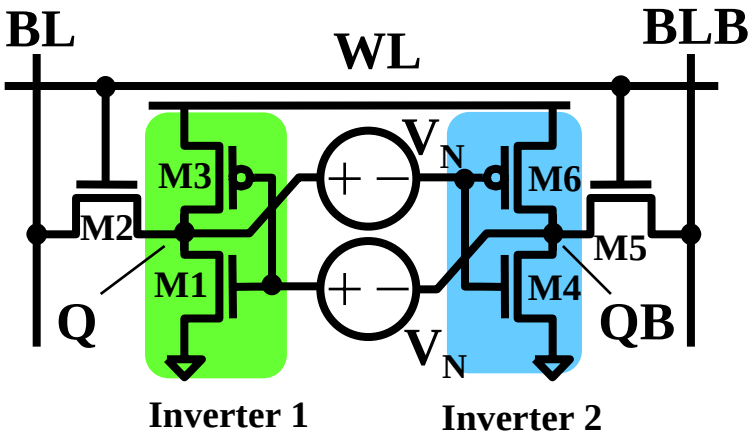
Pleak: 5X to 90X

Energy ↓

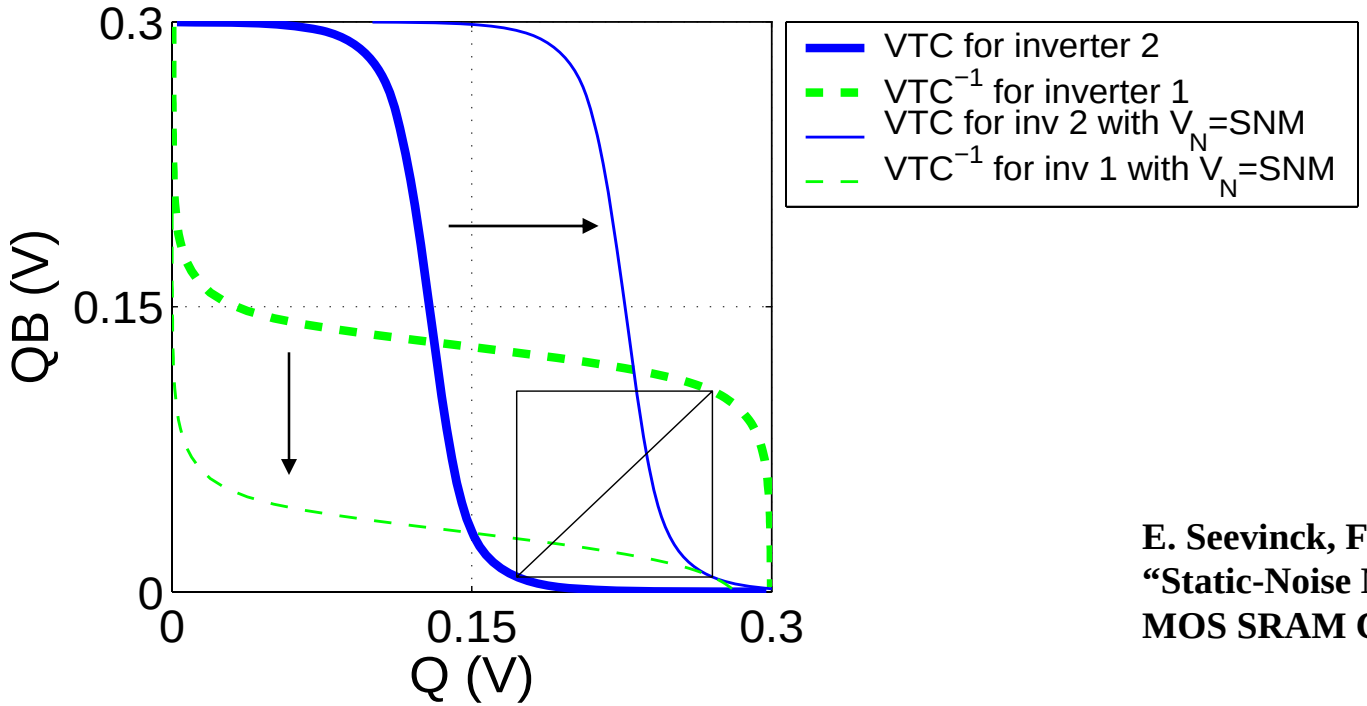
$E = CV_{DD}^2$



Static Noise Margin

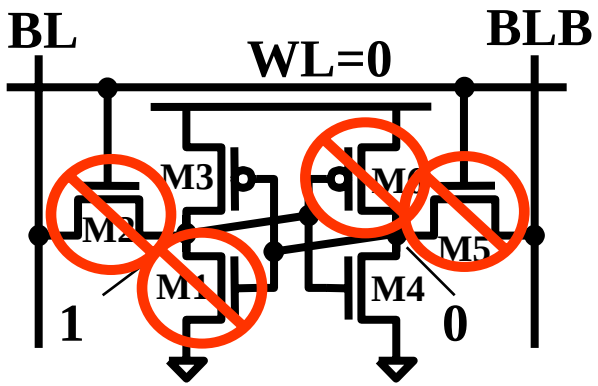


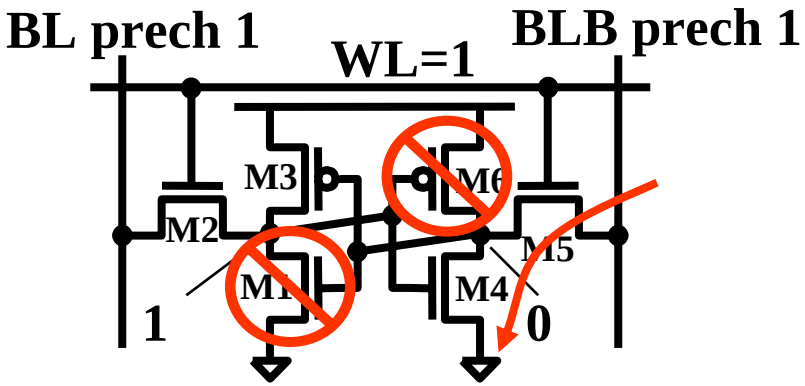
SNM is length of side of the largest embedded square on the butterfly curve

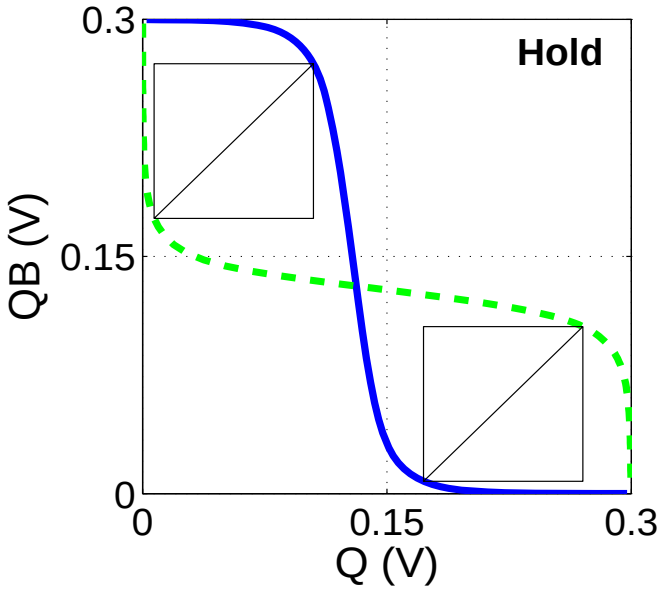


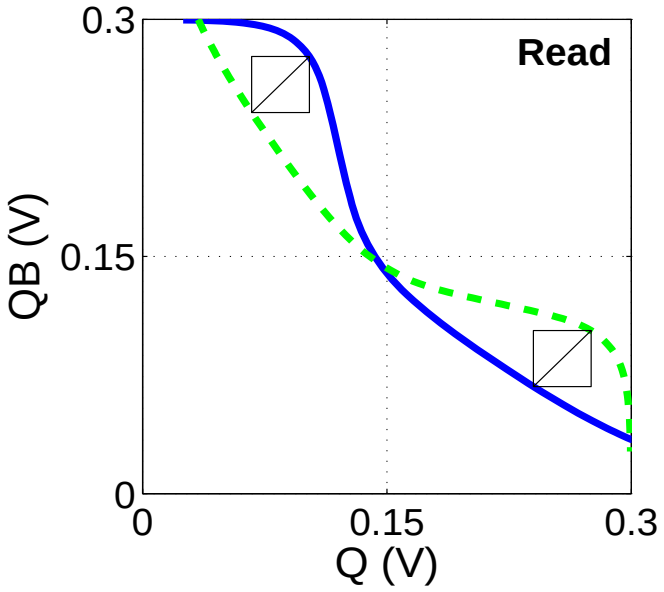
E. Seevinck, F. List, J. Lohstroh, "Static-Noise Margin Analysis of MOS SRAM Cells" JSSC, Oct '87.

SNM during Hold and Read





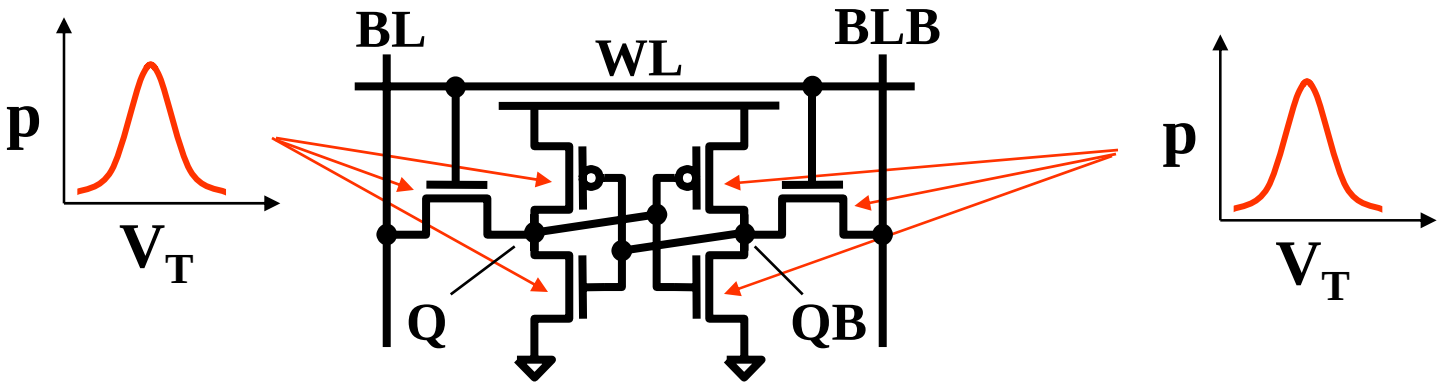


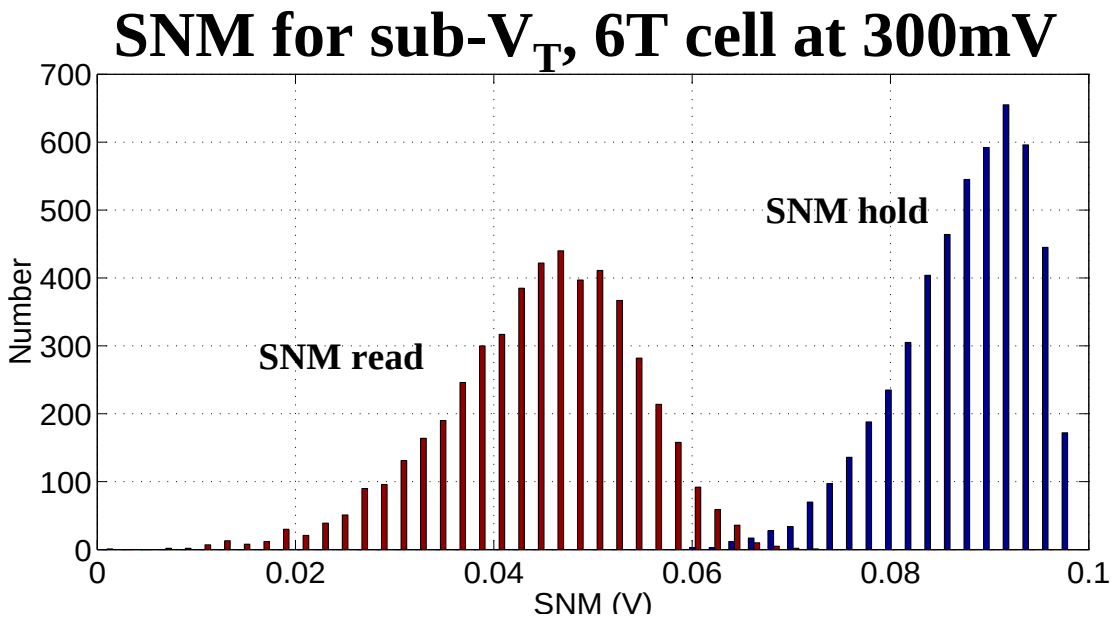


Read SNM is worst-case

6T Read – Static Noise Margin

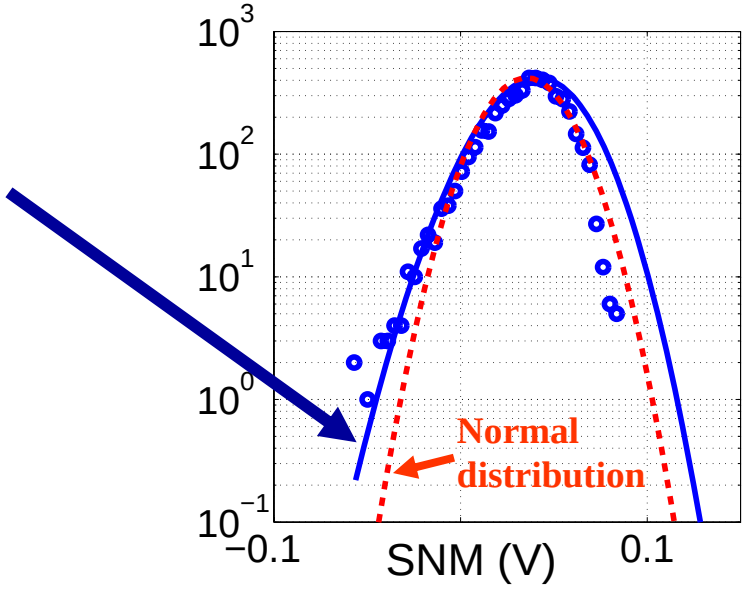
- Variation reduces yield because of SNM



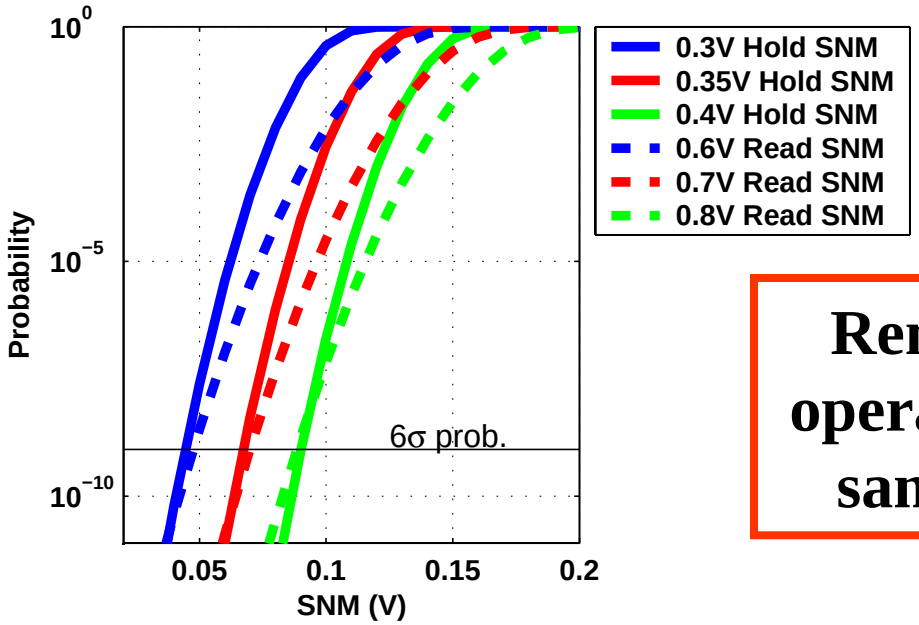


Simulations Compared to Model

Model* gives good estimate for the distribution of SNM at the worst-case tail



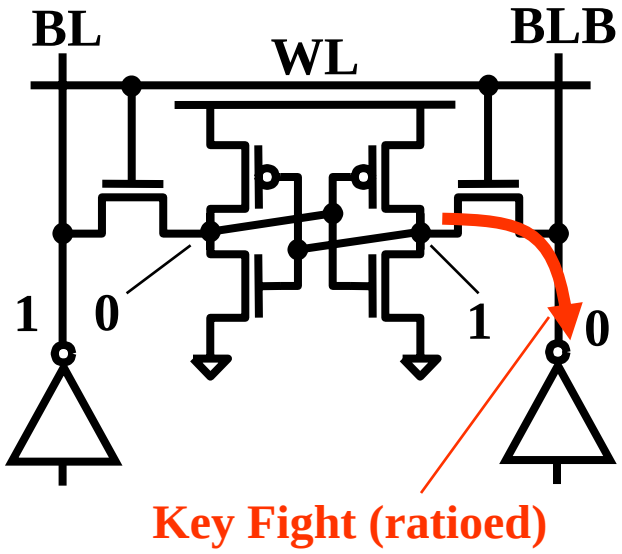
log plot of CDFs

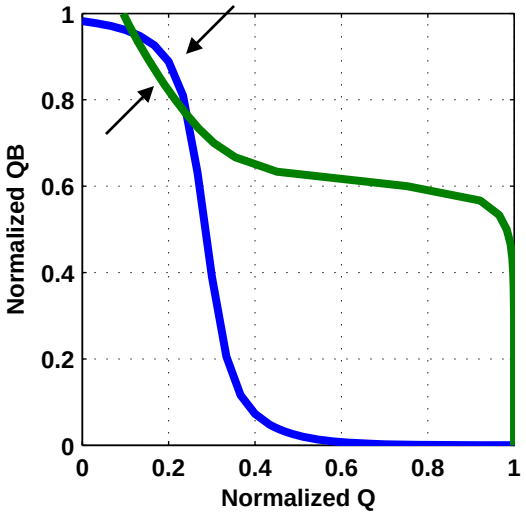


Removing Read SNM allows operation at lower V_{DD} with the same stability at the corners

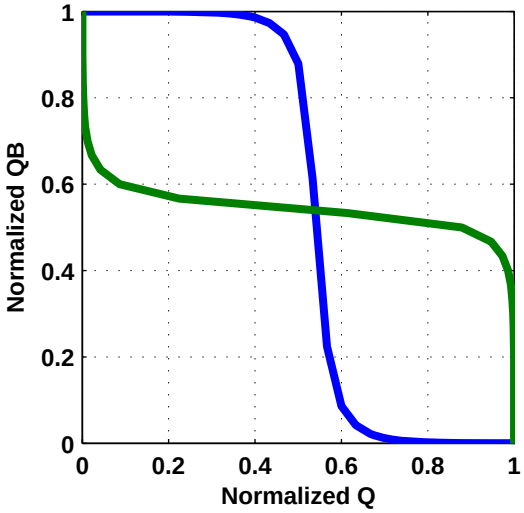
*Calhoun and Chandrakasan, ESSCIRC 2005.

Write Failures

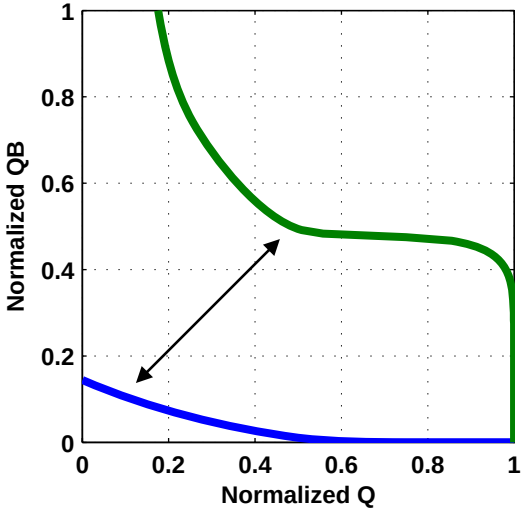




Write failure: Positive SNM

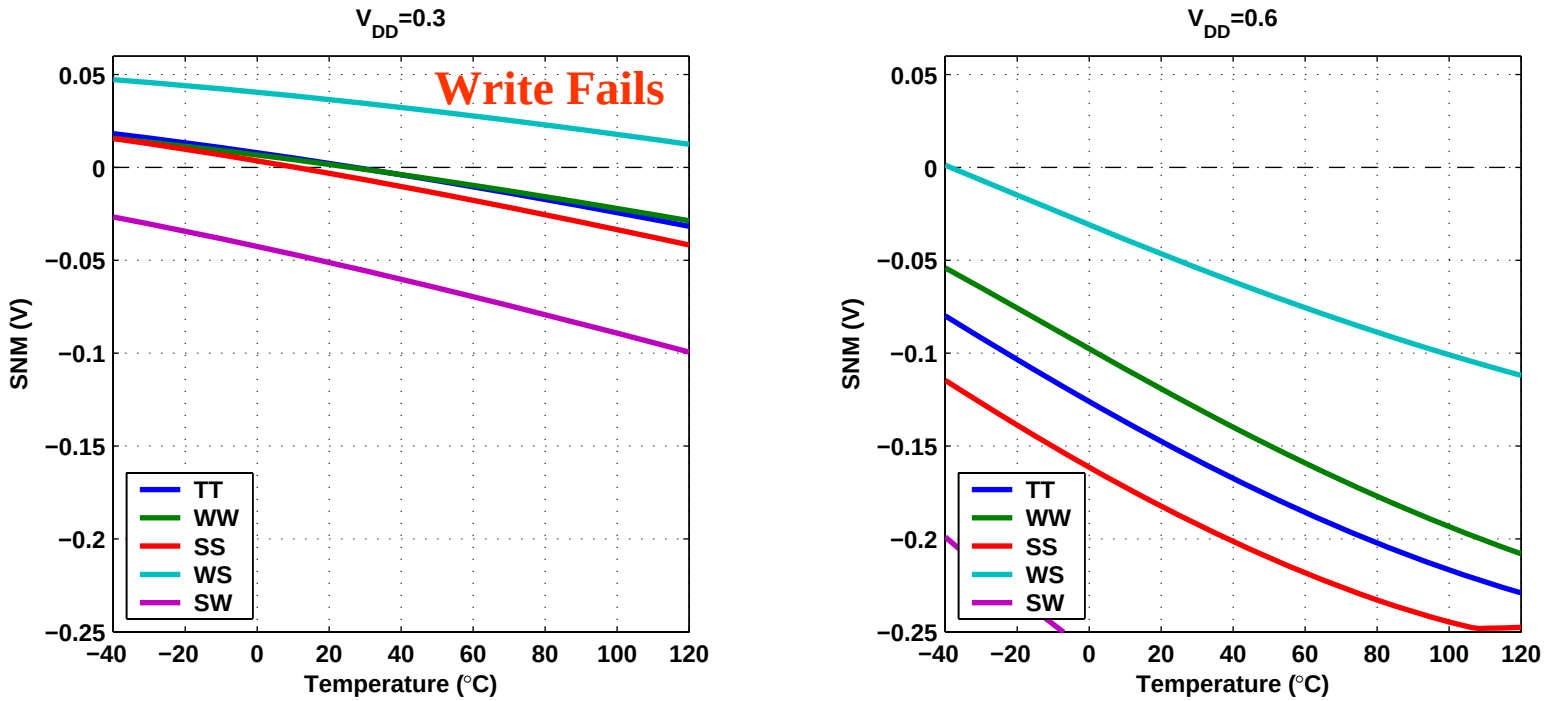


Prior to write



Successful write: Negative "SNM"

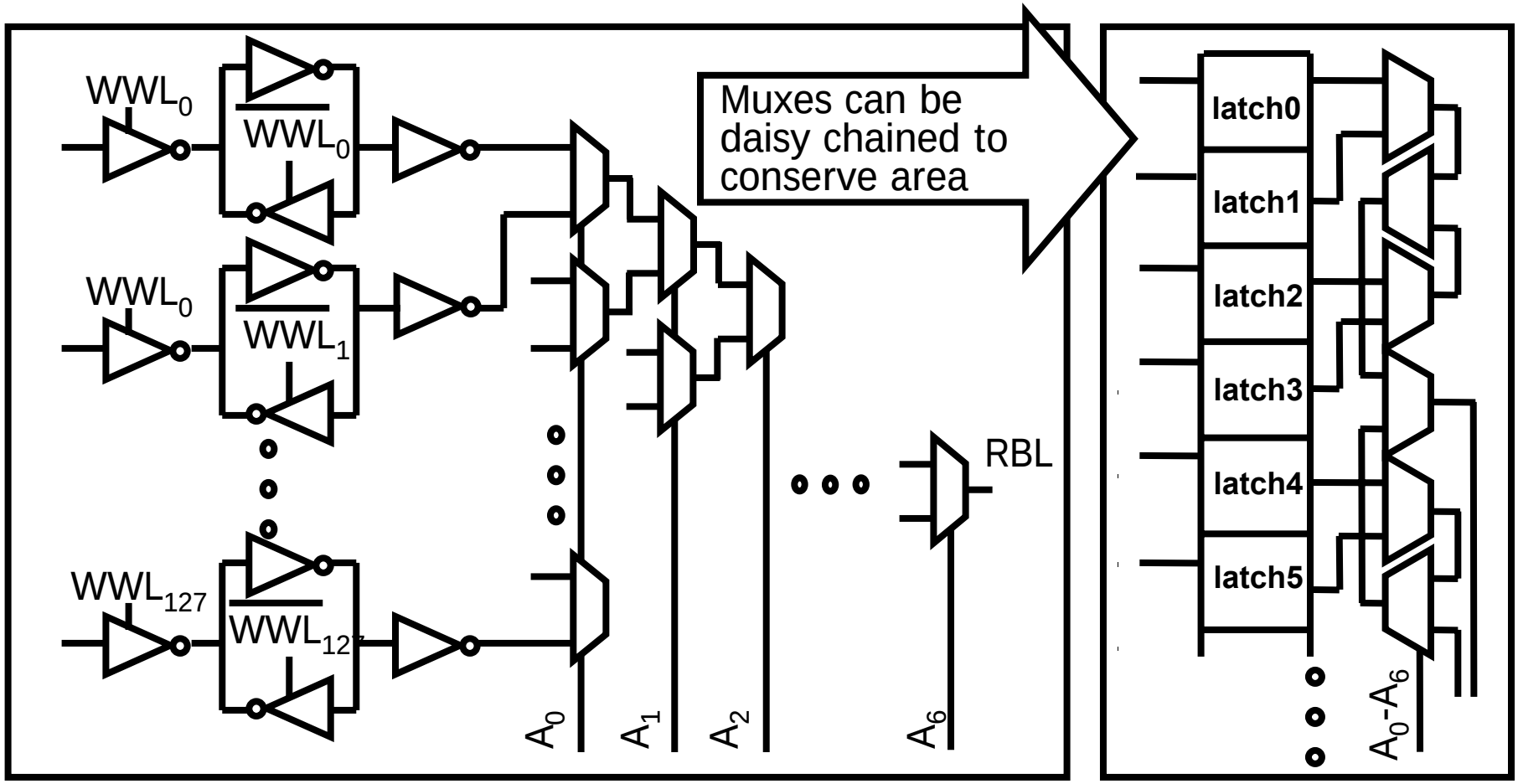
Cannot Write 6T Bitcell



Conventional Write: 0.6V is about the best we can hope for

Mismatch will make this even worse

Previous Work

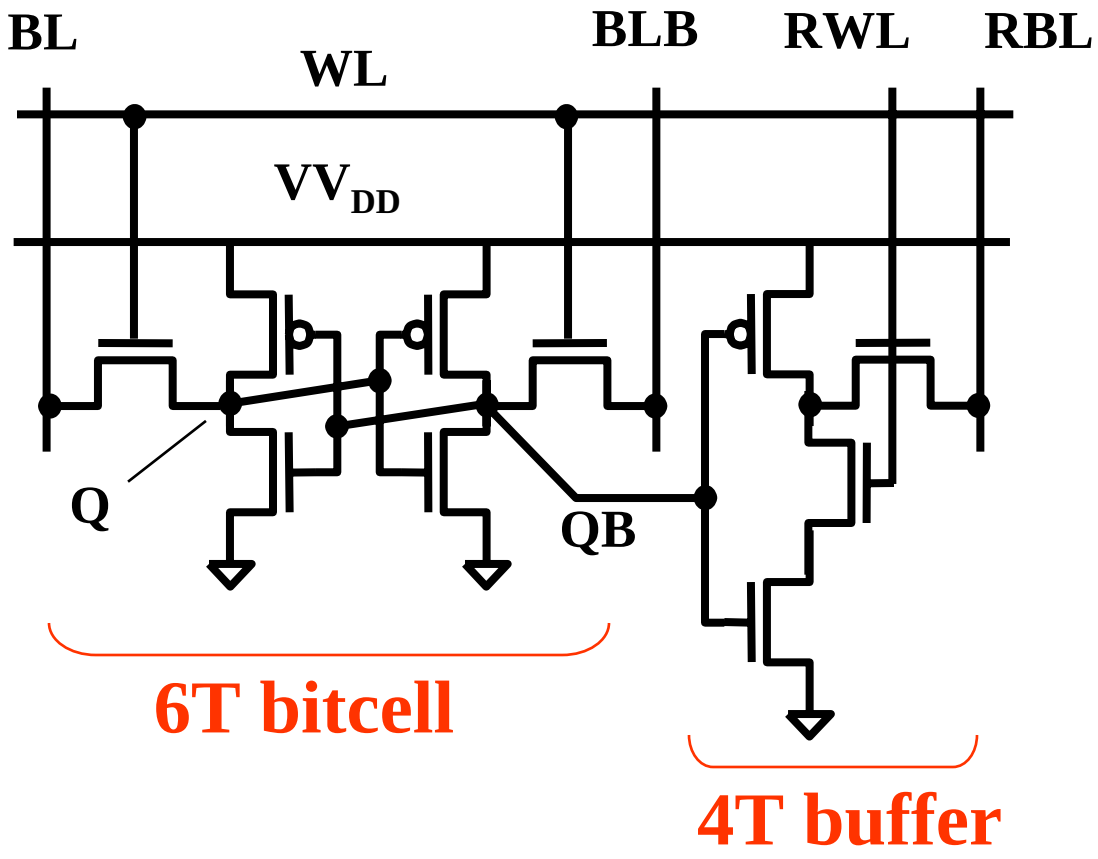


courtesy of A. Wang

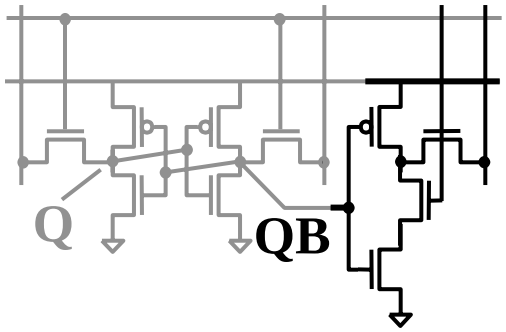
- **18T cell equivalent (when you include the mux)**
- **20-50X slower than 6T at 1.2V**

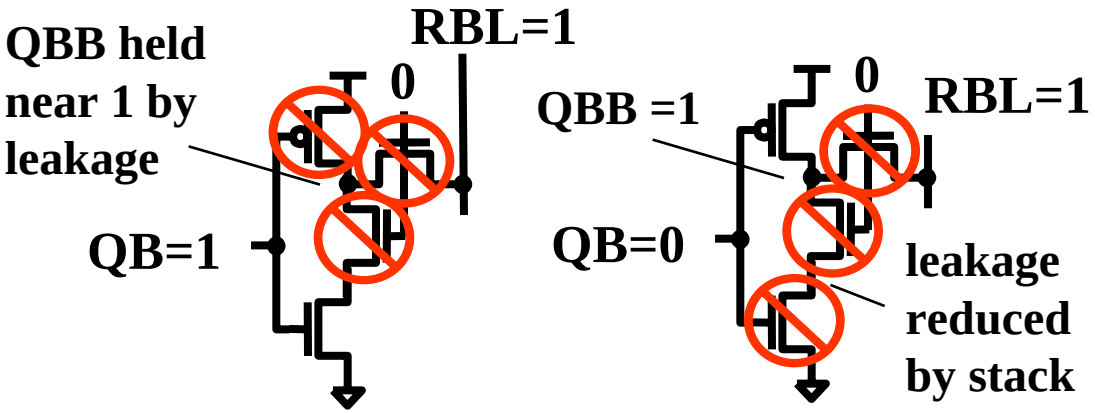
Wang and Chandrakasan *ISSCC* 2004

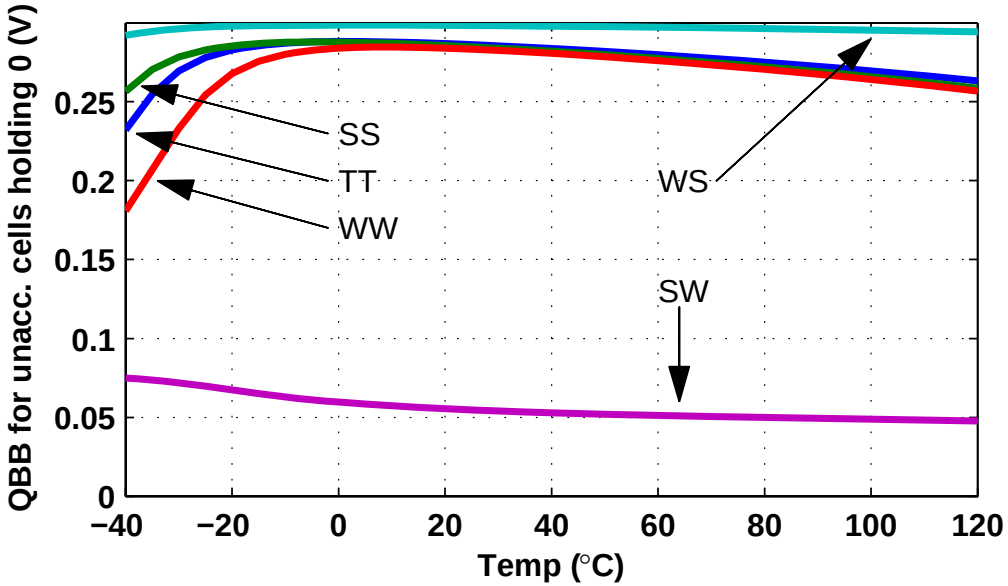
Proposed 10-T bitcell for Sub-V_T



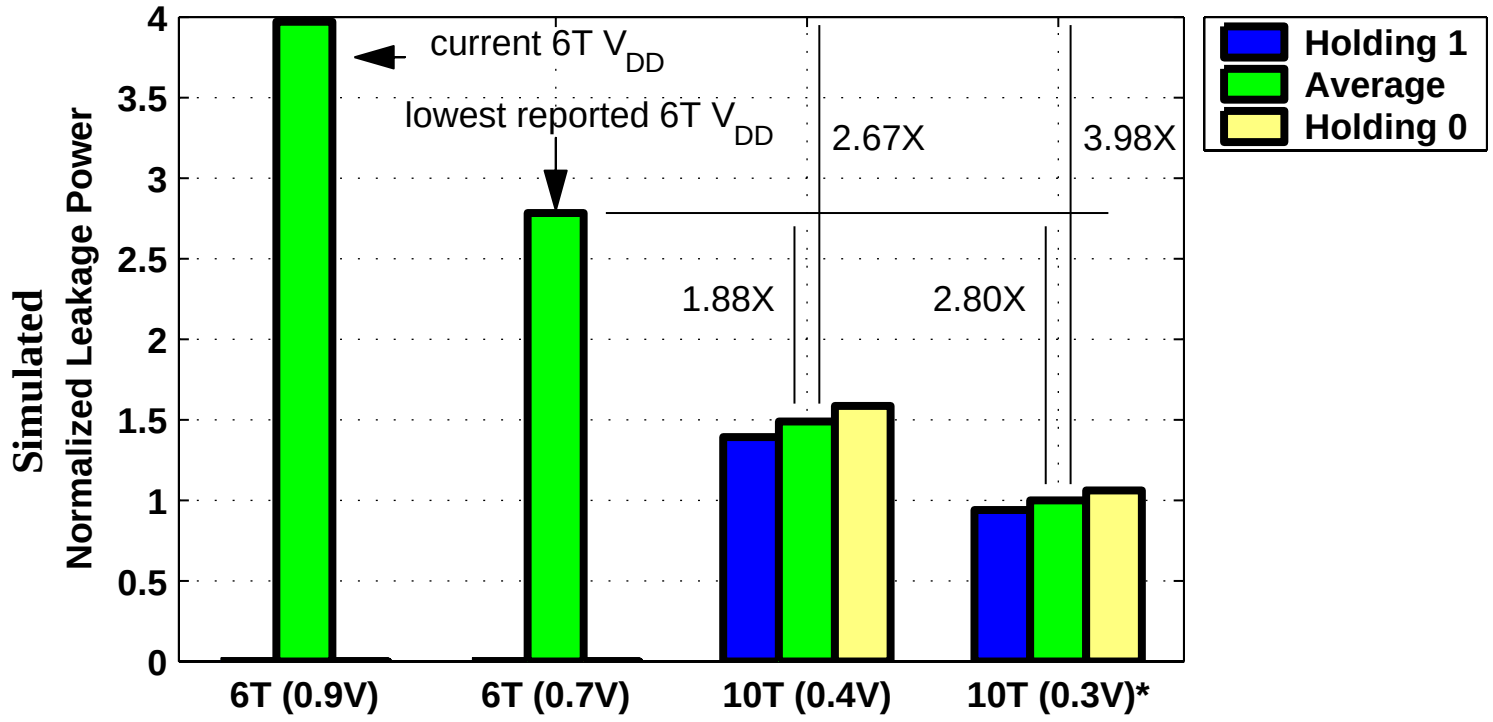
10T Bitcell Reduces Bitline Leakage







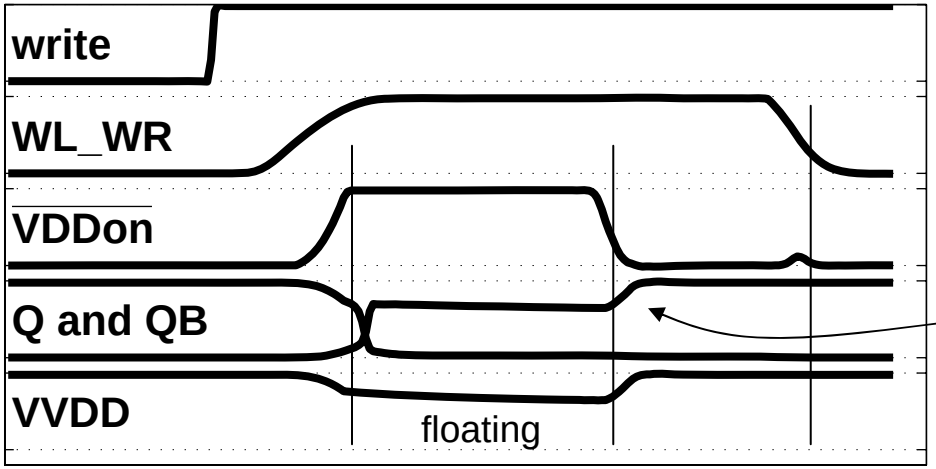
Leakage Power Savings with 10T Bitcell



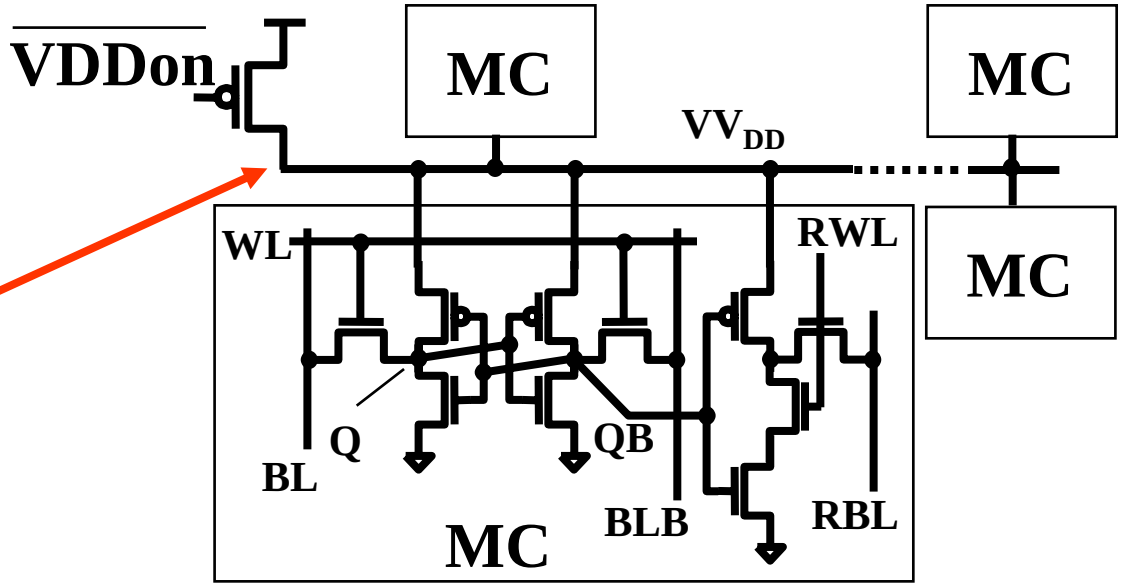
- 6T memories in 65nm usually at 0.9V or greater (lowest reported is 0.7V)
- 10T bitcell allows scaling to lower voltages
- Lower voltage operation reduces leakage power dramatically for unaccessed cells

10T Bitcell Allows Sub-V_T Write

Floating V_{DD} weakens feedback and allows write

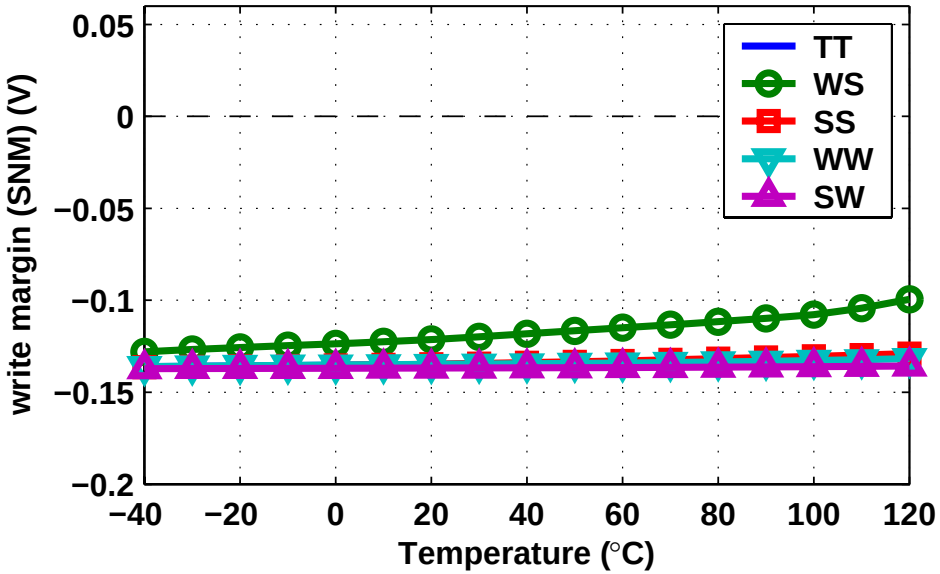


feedback restores '1' to V_{DD}

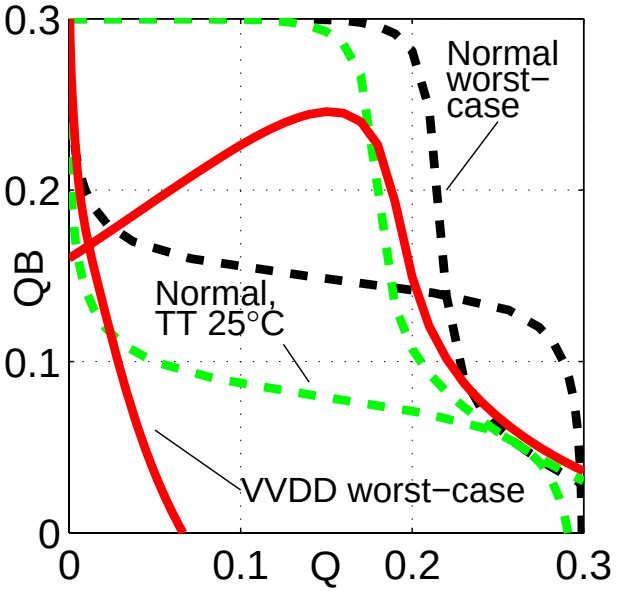


Folded WL shares VV_{DD}

10T Bitcell Allows Sub-V_T Write

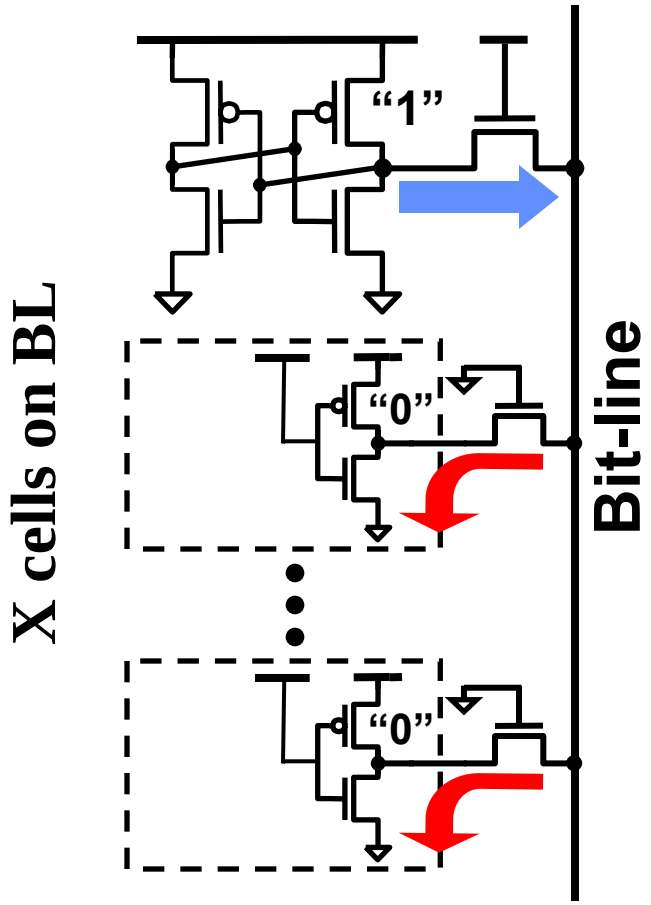


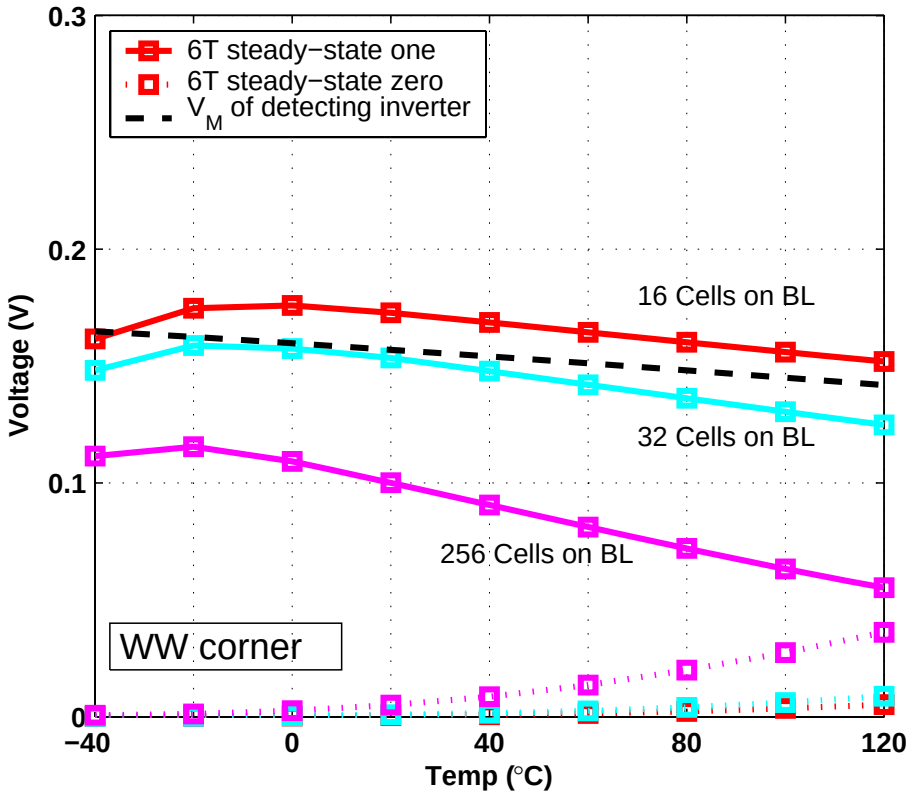
Write successful across process corner and temperature



Write margin correctly negative at worst-case corner

Bitline Leakage Limits Integration Level

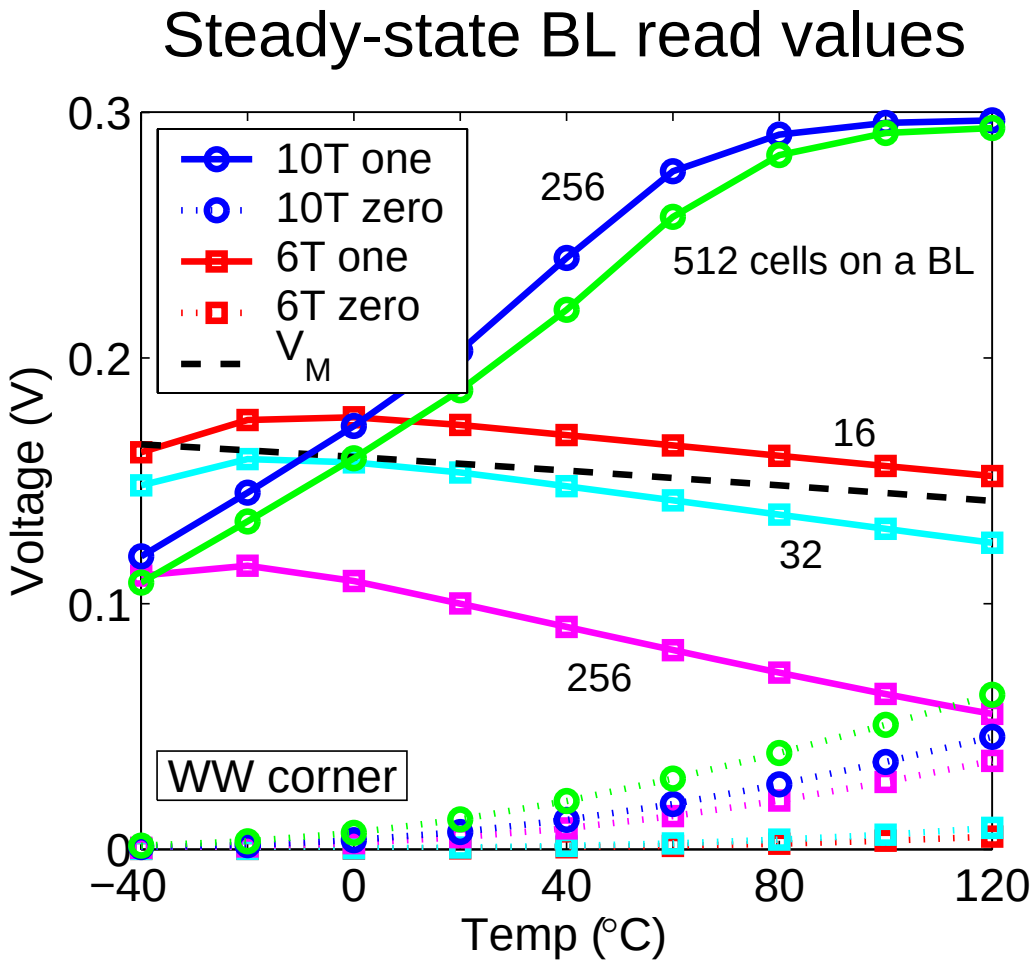




- BL leakage degrades read values

16 bitcells on bitline is best can hope for standard 6T

10T Bitcell Lowers Bitline Leakage

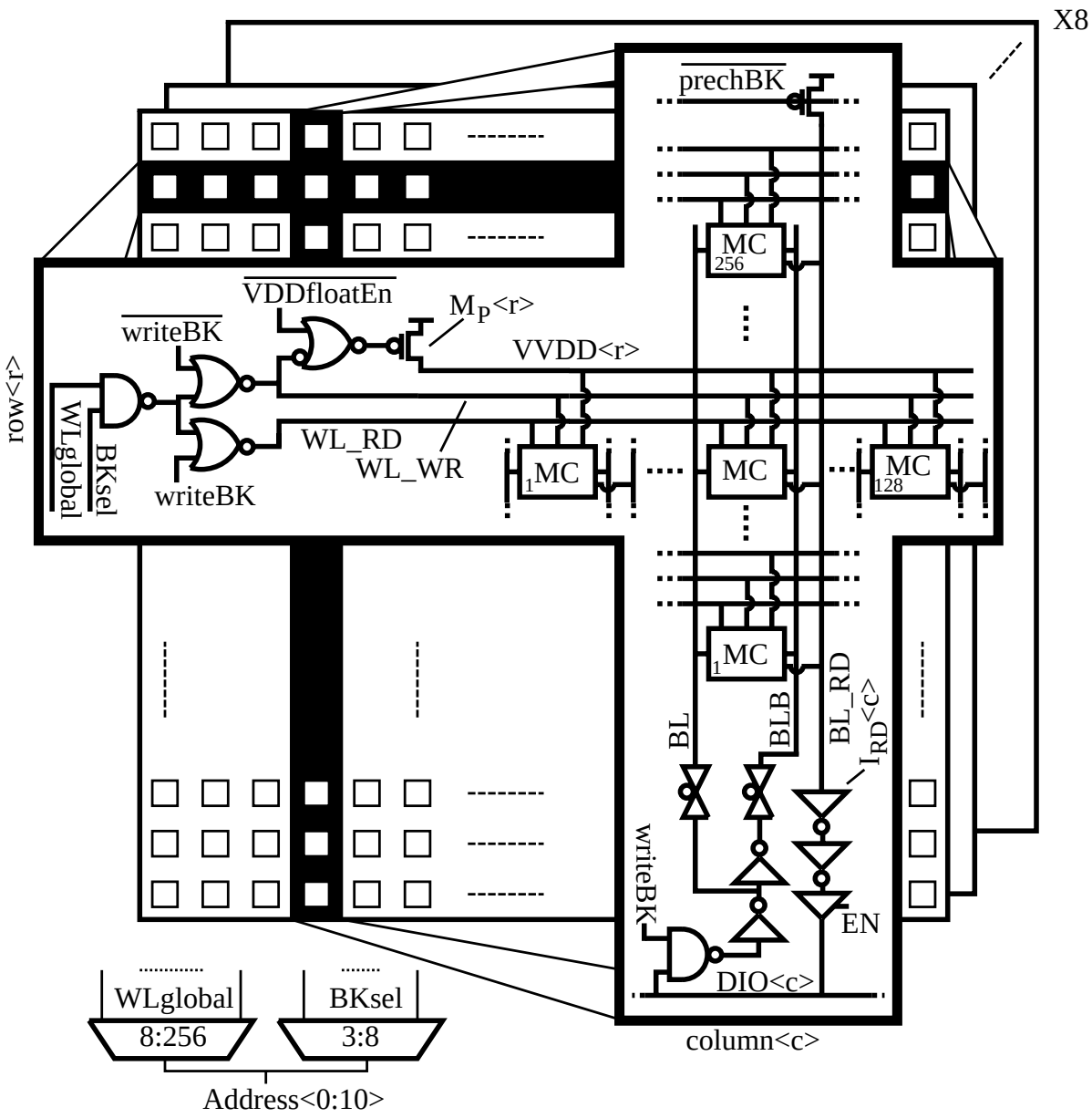


10T bitcell enables higher level of integration on BL

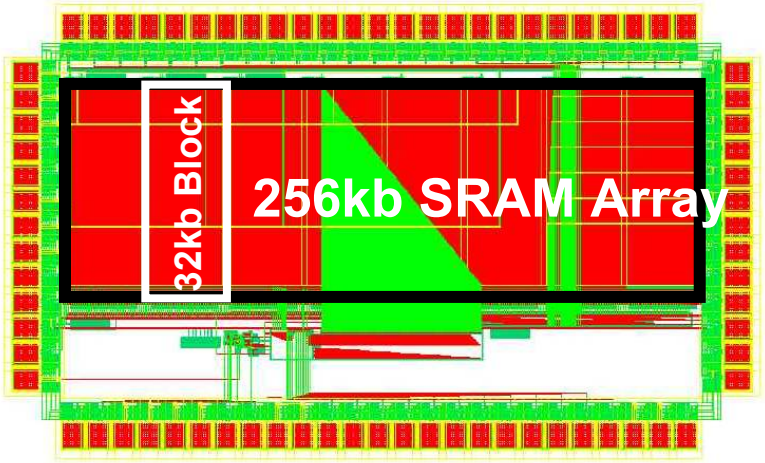
Test Chip Architecture

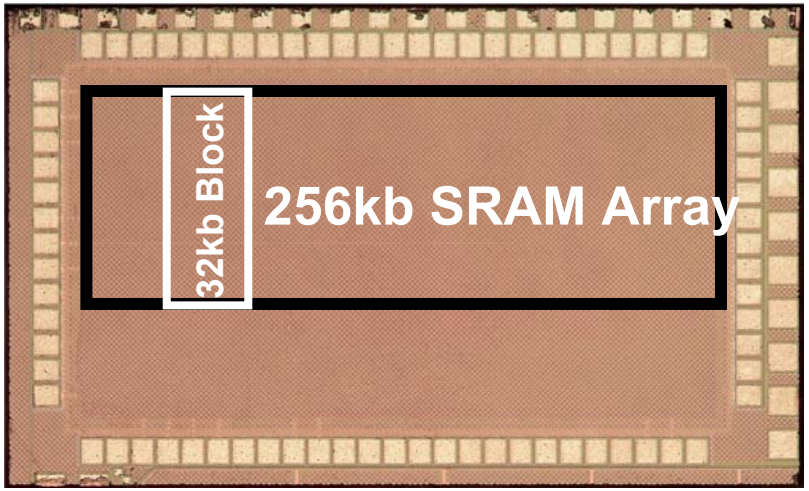
- 256 rows and 128 columns per block
- Static CMOS peripherals
- Separate WL V_{DD} for boosting
- Assumed 1x1 redundancy
- Simulation:

Operates at 300mV across all process corners from 0 to 100°C



256Kb 65nm Sub-V_T memory



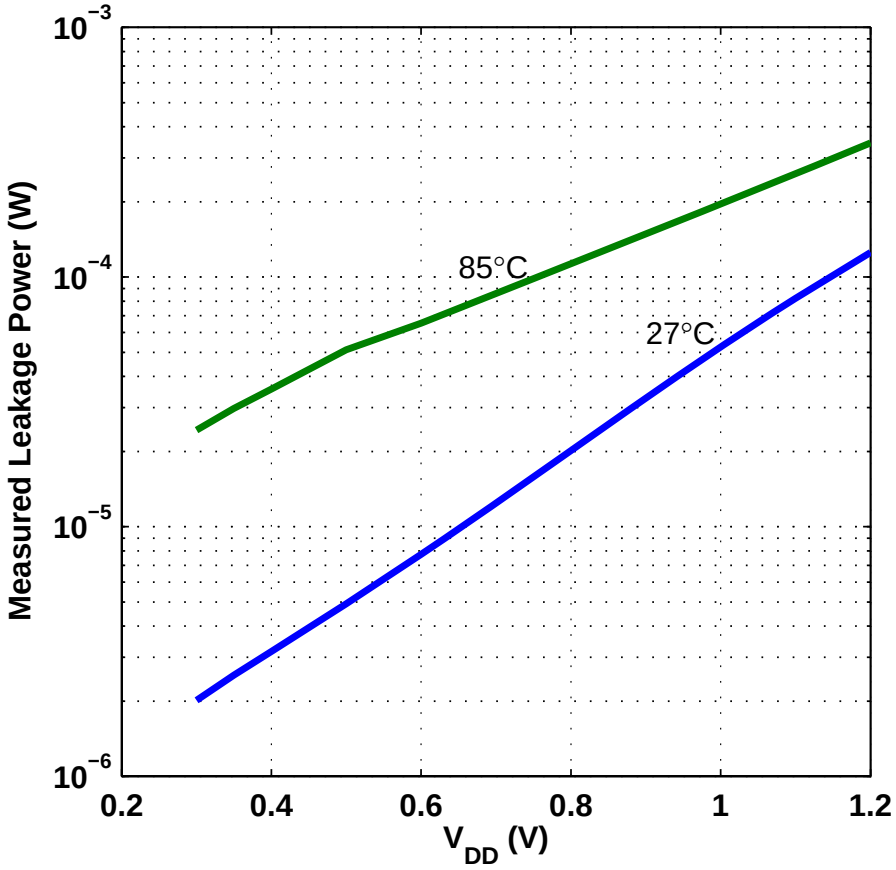


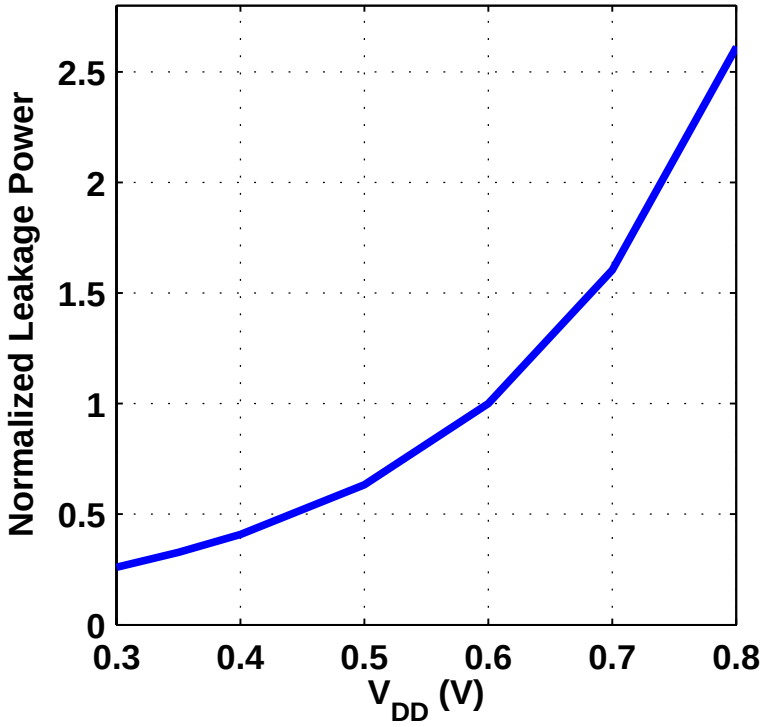
Test chip addressing the sub-V_T problems using 10T bitcell: 1.89mm by 1.12mm

Chip functions to below 400mV, holds without error to <250mV:
At 400mV, 3.28μW and 475kHz at 27°C

Reads without error to 320mV (27°C) and 360mV (85°C)
Write without error to 380mV (27°C) and 350mV (85°C)

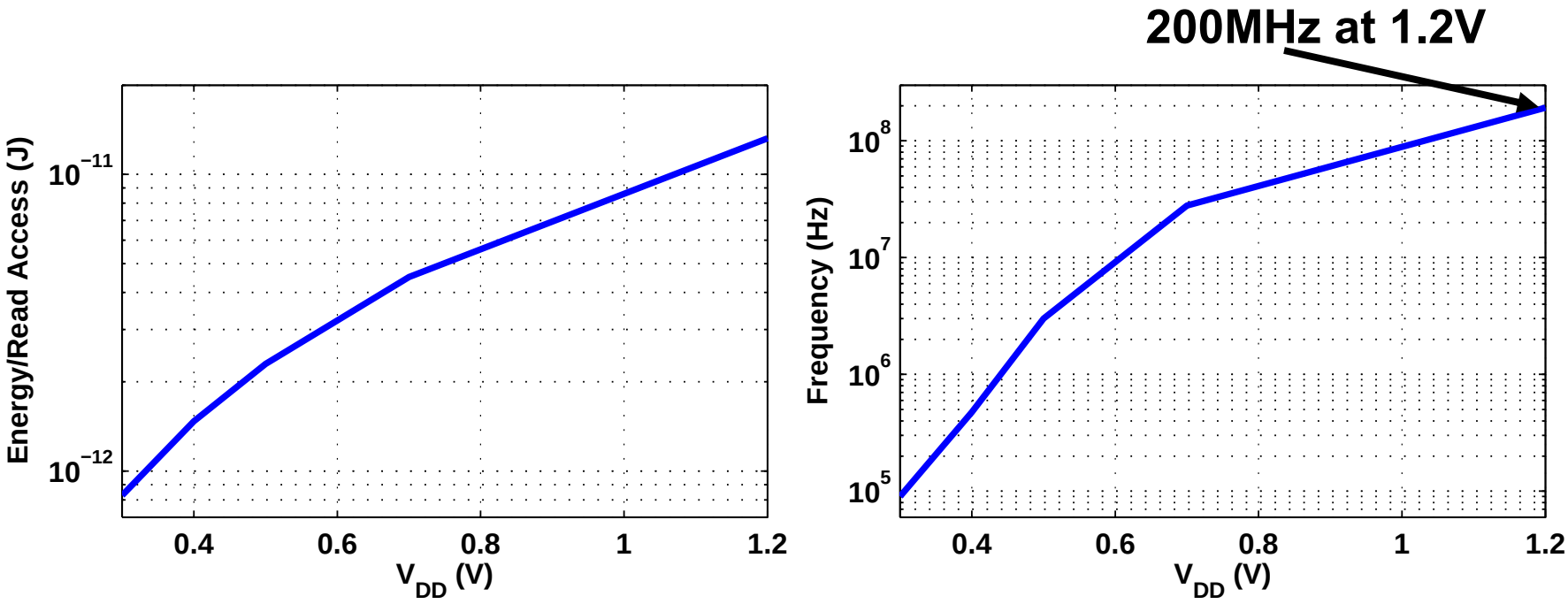
Power Measurements





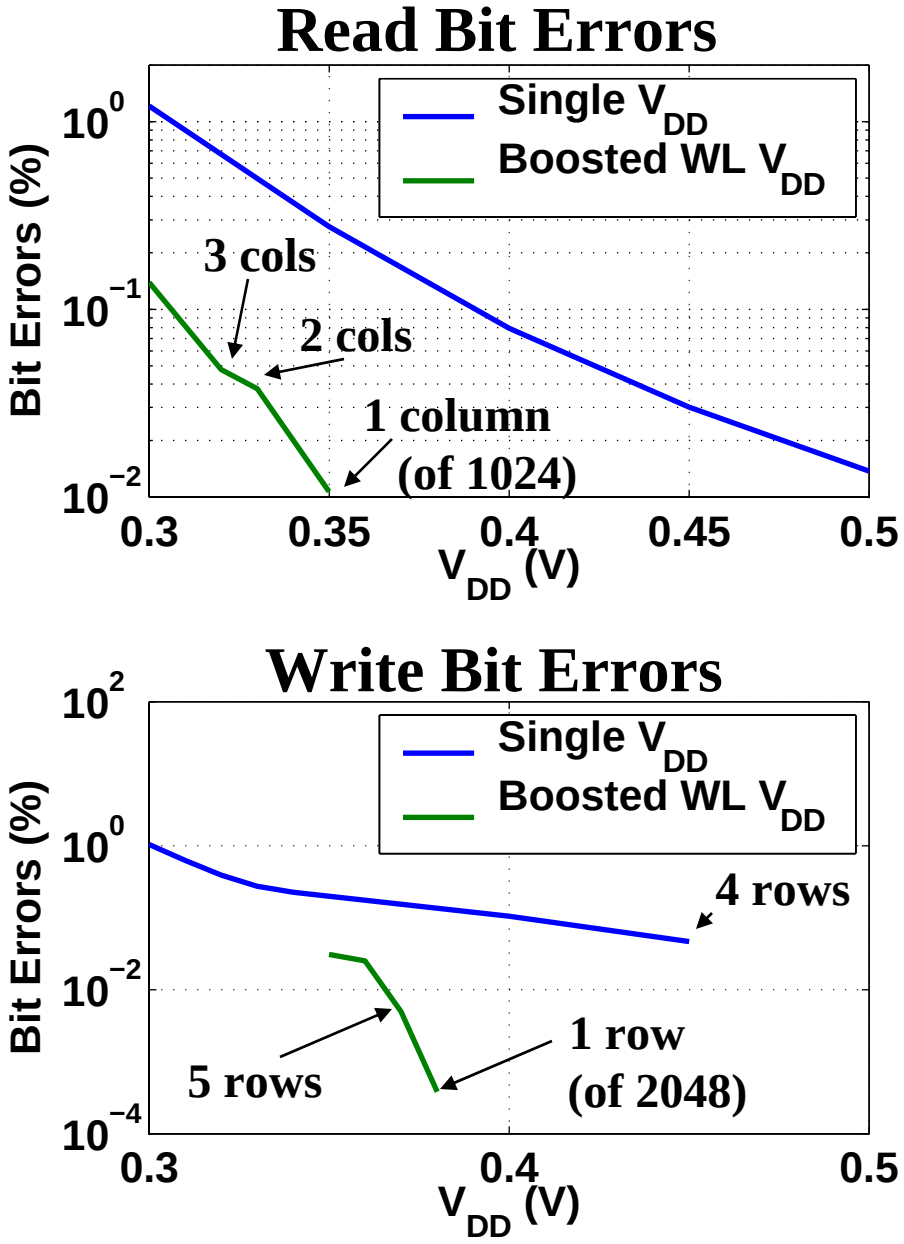
Relative to 0.6V 6T SRAM, 2.2X less leakage power at 0.4V and
3.3X less leakage power at 0.3V
>60X less leakage power than 1.2V

Active Energy Savings with 10T Bitcell



- 6T memories in 65nm usually at 0.9V or greater (lowest reported is 0.7V)
- Operating 10T bitcell at lower voltages saves energy
- 10T memory can provide high frequency operation at higher voltages when necessary

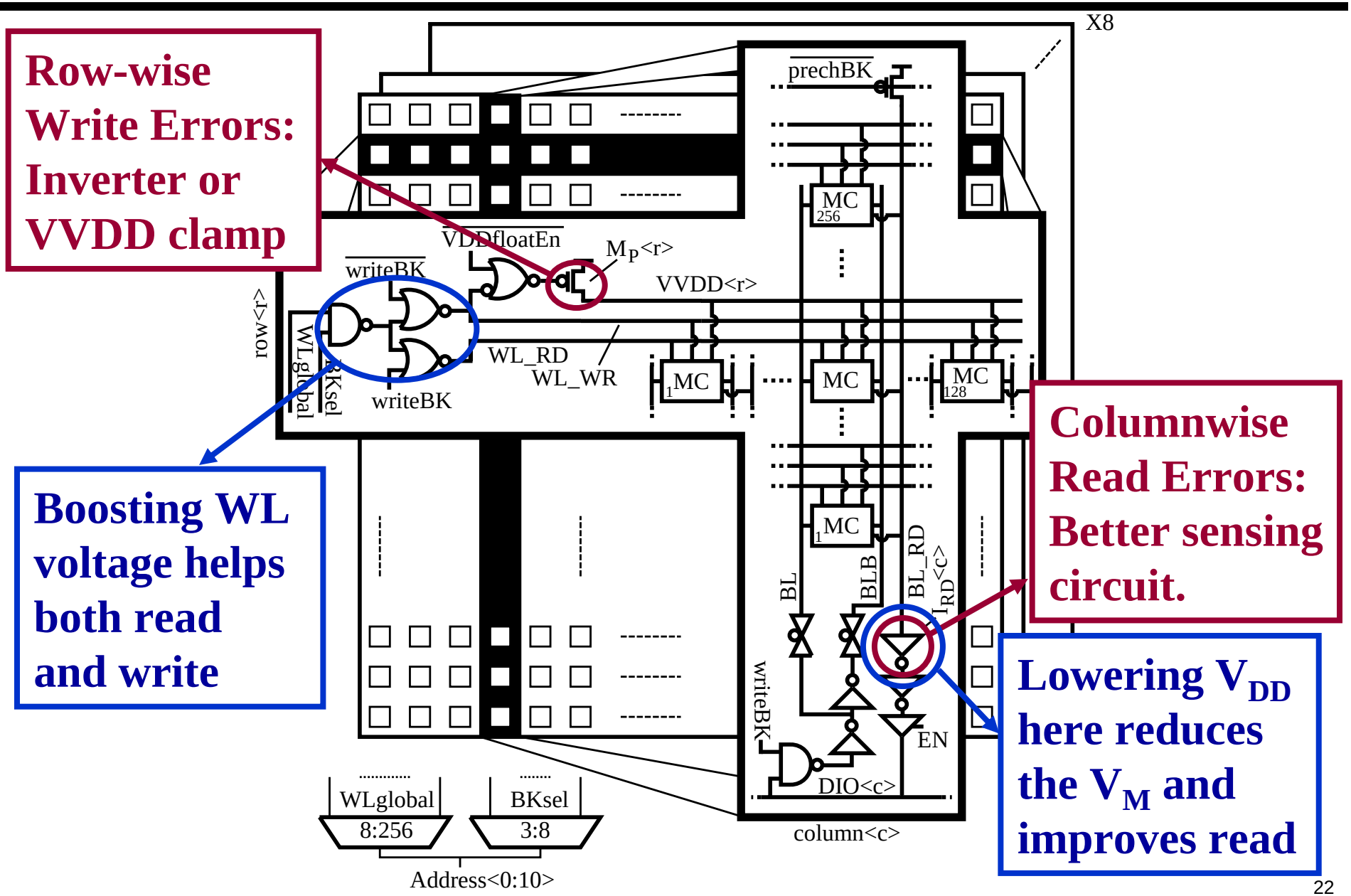
V_{DD} Scaling Limits



Redundancy and/or boosted WL account for mismatch

1x1 redundancy and WL boosting:
Read works to <u>320mV</u>
Write works to <u>380mV</u>

Voltage Limits and Proposed Improvements



Conclusions

- Standard 6T approach limited to ~0.6-0.7V and 16 cells per bitline
- Proposed 10T bitcell shows sub-threshold operation with overall power and energy savings
- Sub-V_T memory requires circuits and architectures to manage variability and low I_{on}/I_{off}

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