Highly Interleaved 5b 250MS/s ADC with Redundant Channels in 65nm CMOS

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Outline

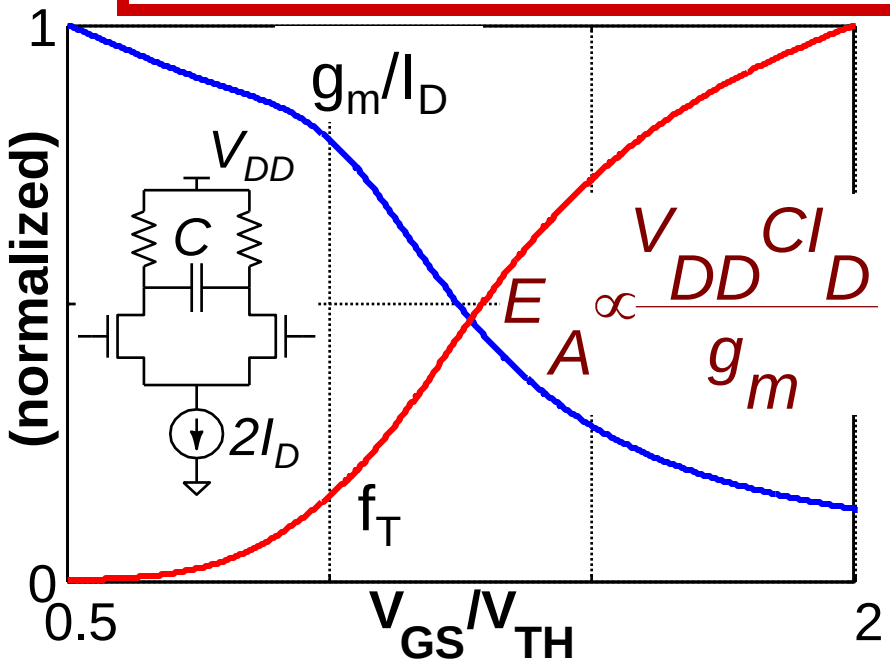
- Parallelism in ADCs
- Local Variation and Redundancy
- Chip Implementation
- Measured Results
- Variation and Yield Data
- Conclusions

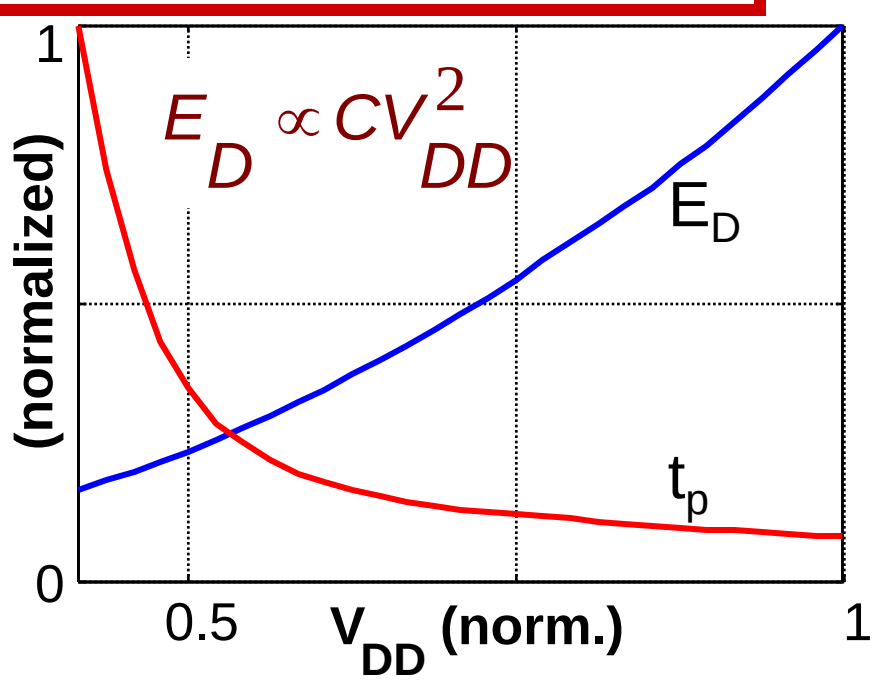
Why Time-Interleave?

- Push resolution/speed boundary of an architecture [Poulton, ISSCC 2003], [Draxelmayr, ISSCC 2004]

Slower ADCs are more energy efficient

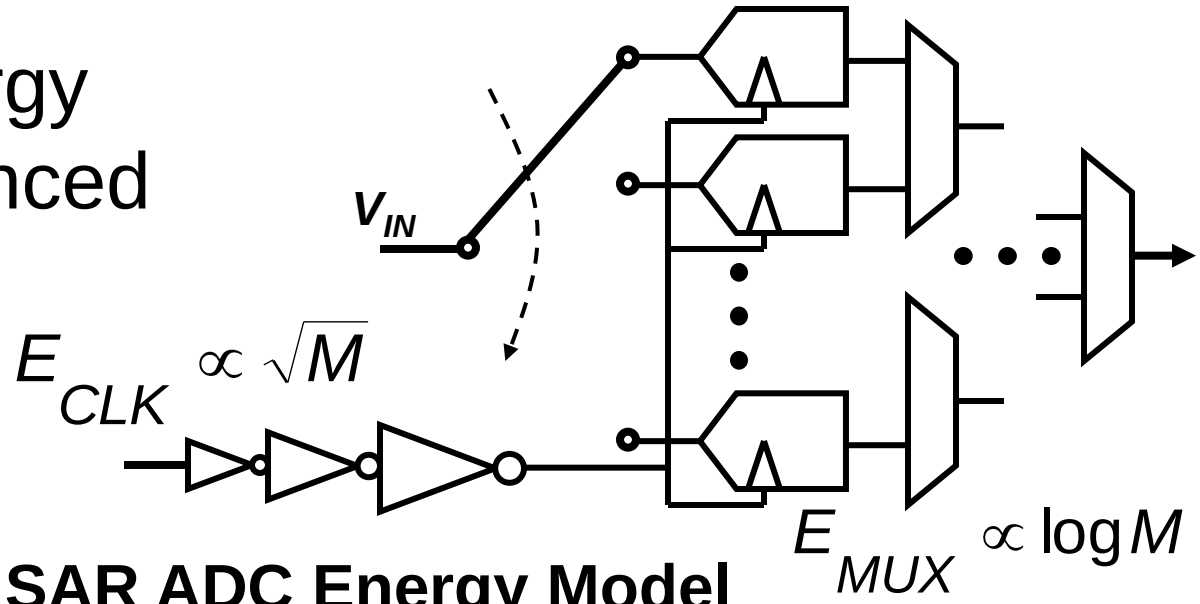
- Analog circuits biased in sub-threshold
- Reduced digital supply voltages

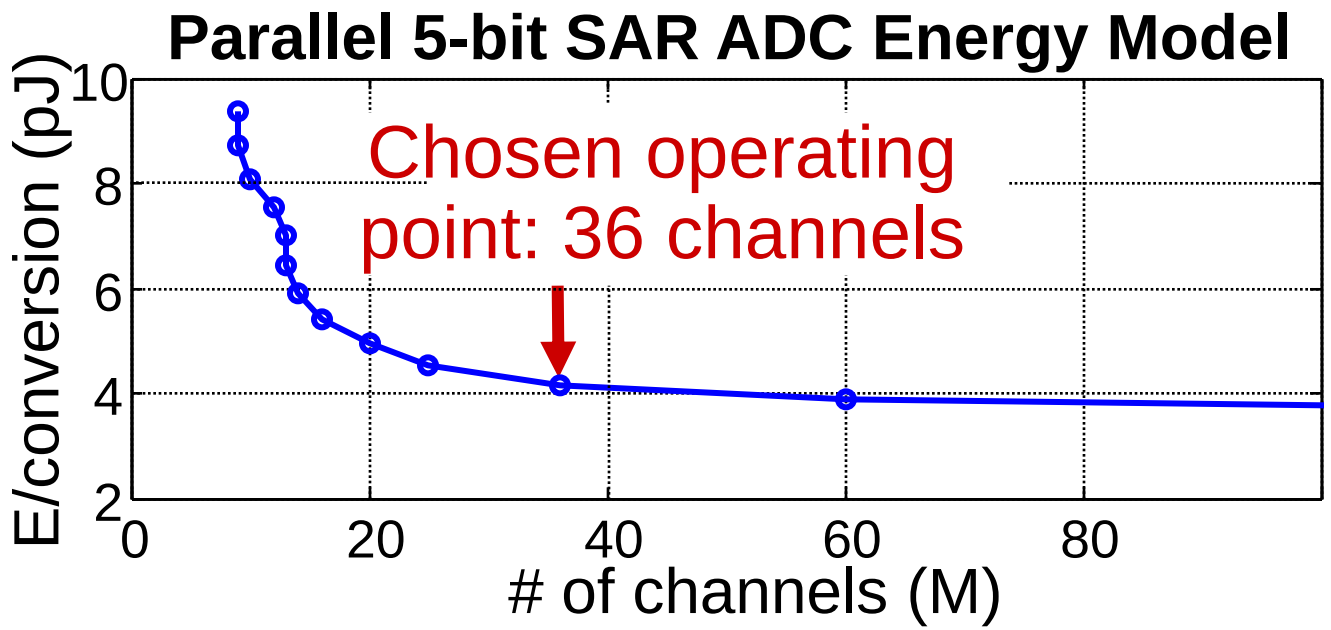




Parallelism and Energy

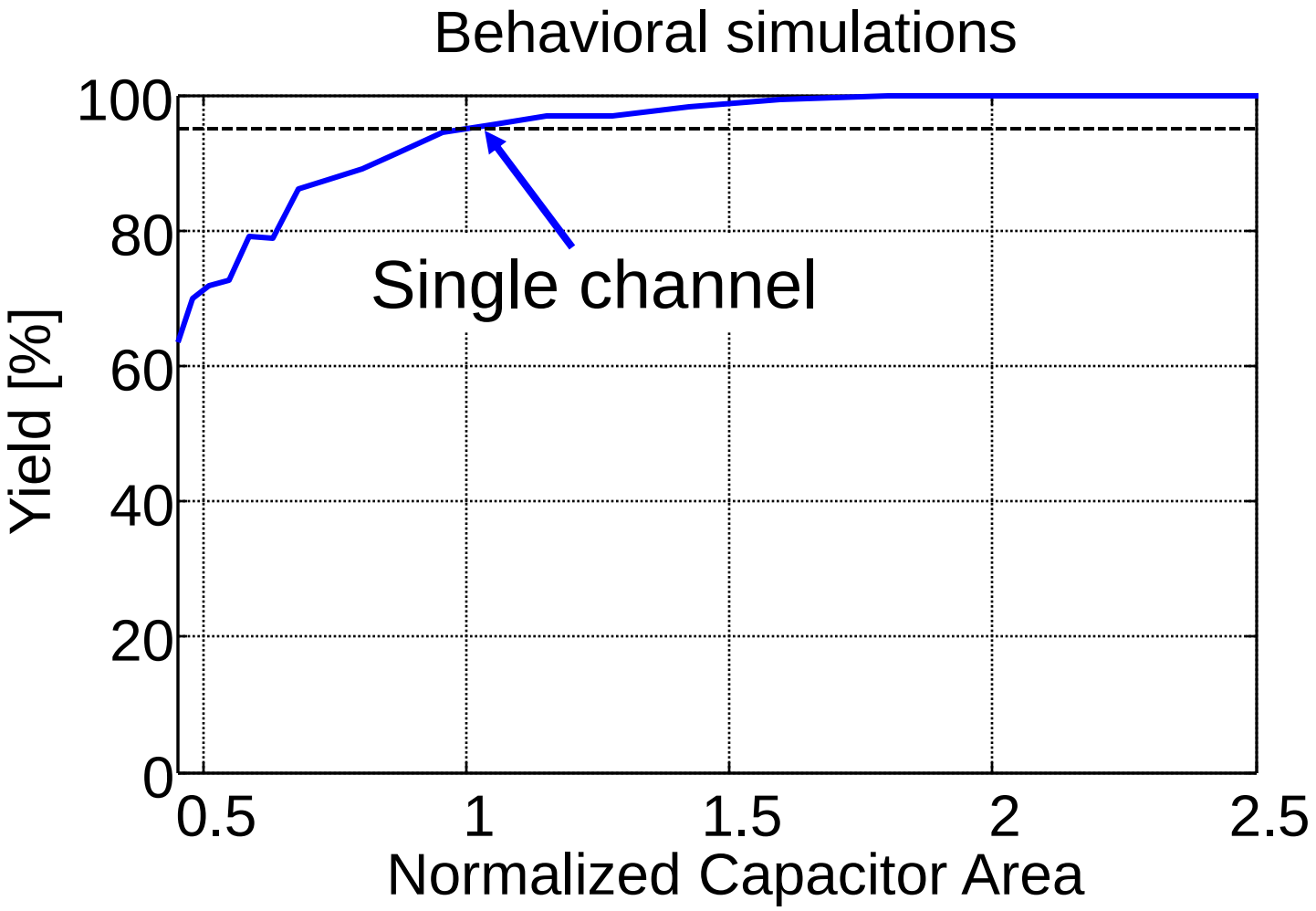
Per-channel energy advantages balanced by overheads of parallelism



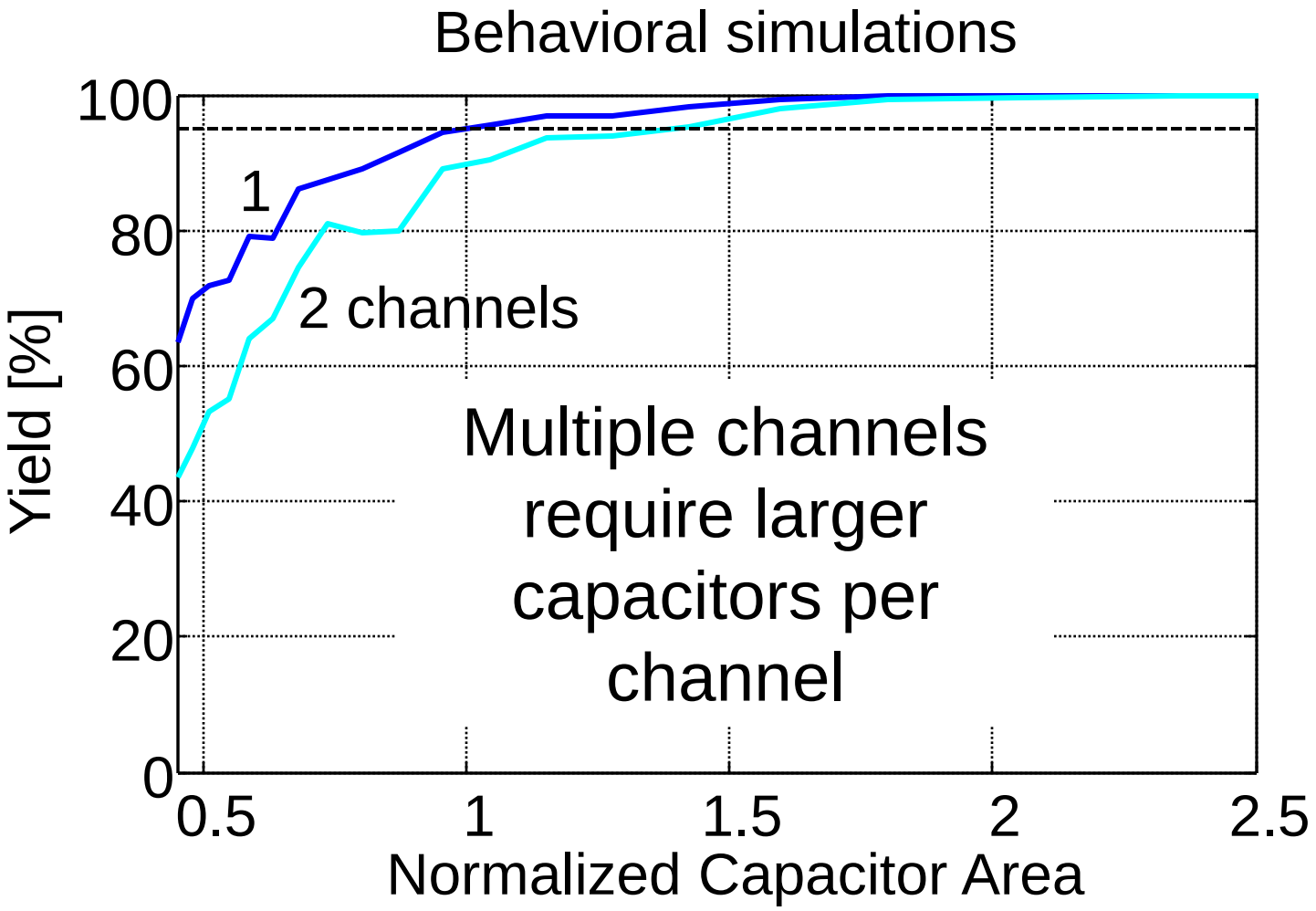


M = # of channels

Capacitor Sizing and Yield



Capacitor Sizing and Yield



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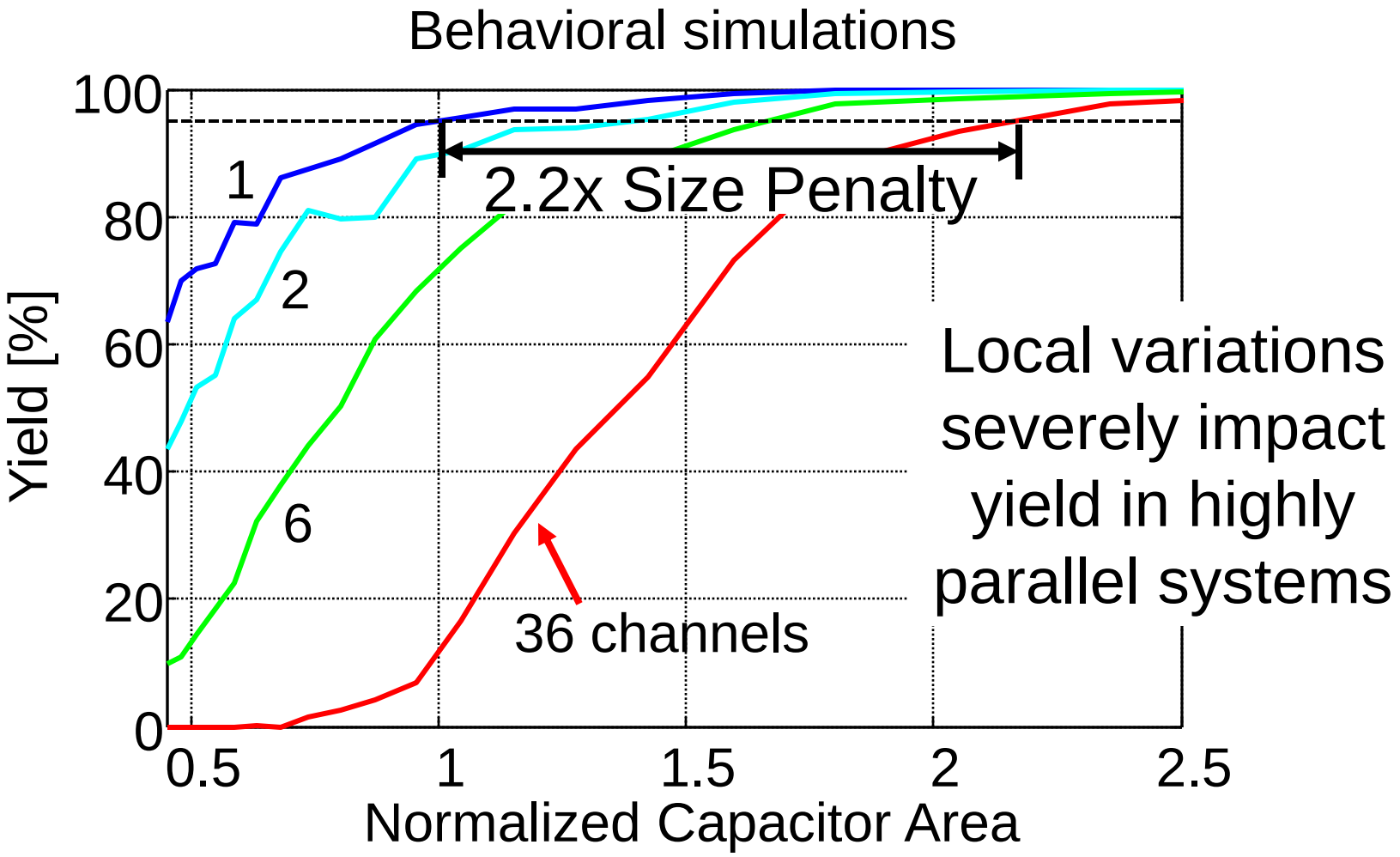
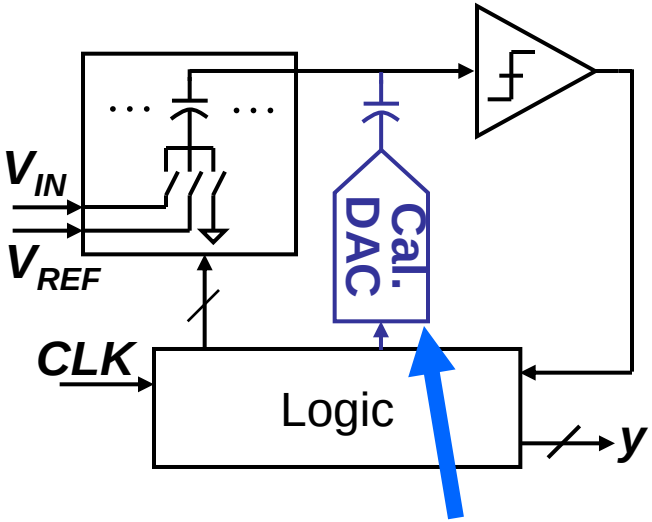
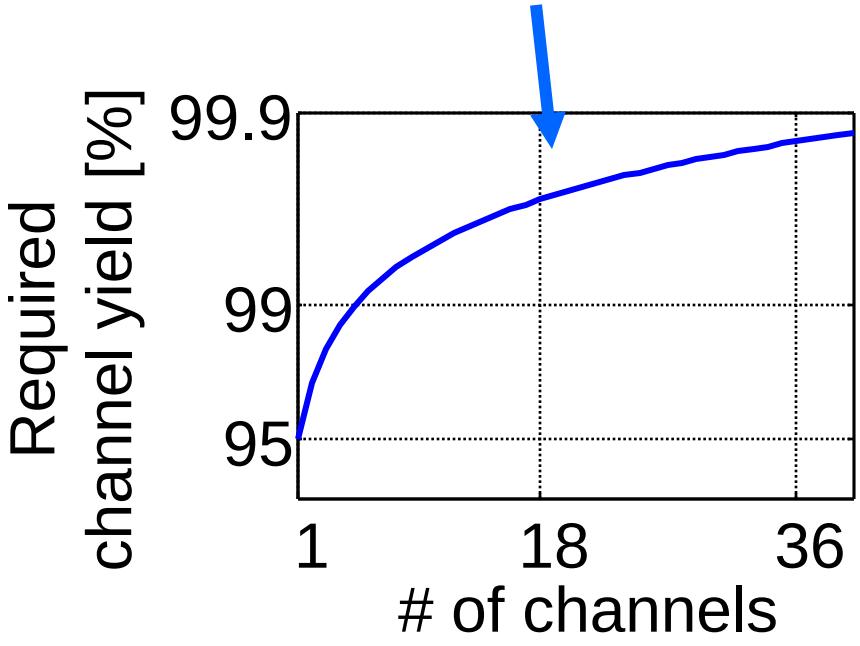


Mitigating Local Variation

- Calibration is the standard solution to improve yield [Poulton, ISSCC 2003]
- Final required channel yield is unchanged by calibration



Corrects for INL, DNL, & OS

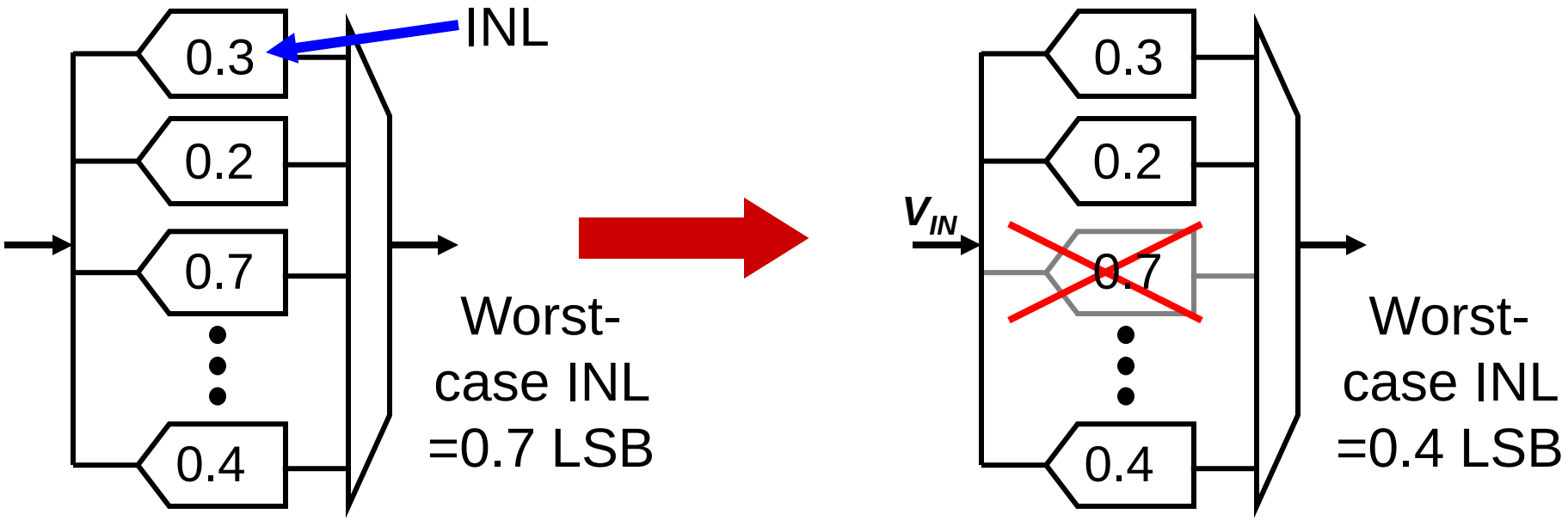


Fault coverage is limited by particular calibration choice

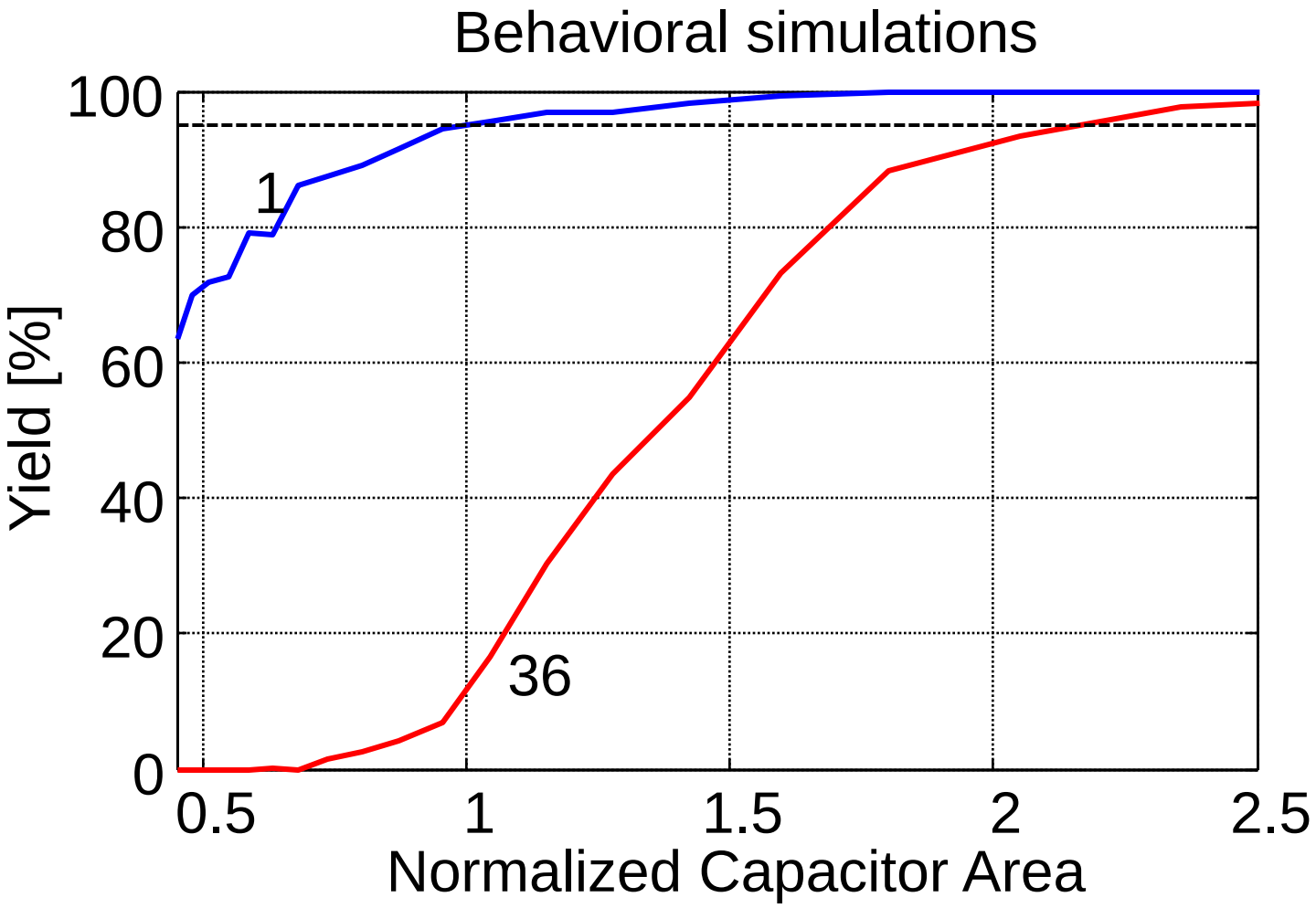
Redundancy

Adding extra (redundant) channels addresses the underlying statistics

- Apply redundancy at maximum level of parallelism
- Eliminate the “worst” channels that otherwise limit yield



Capacitor Sizing + Redundancy



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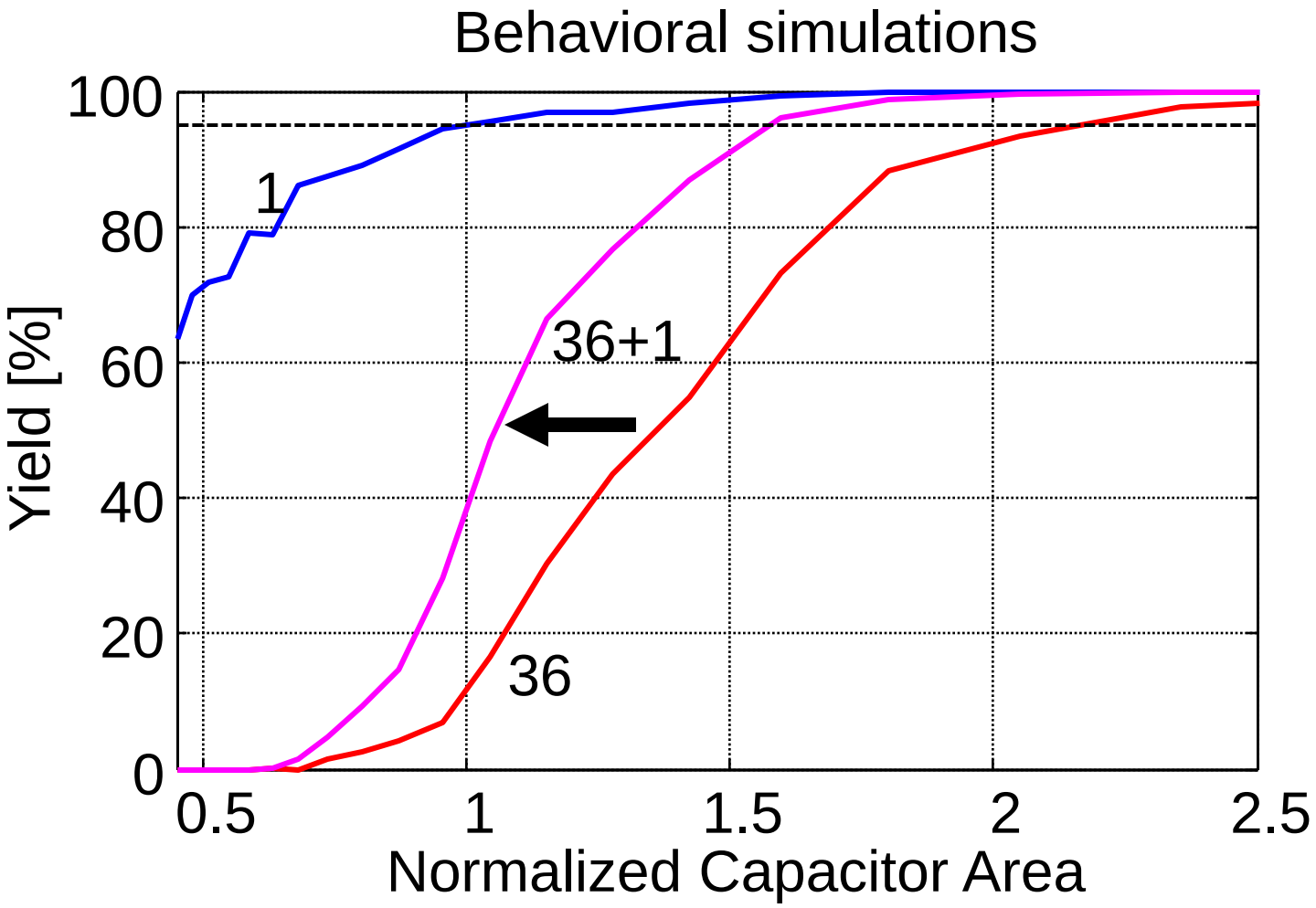

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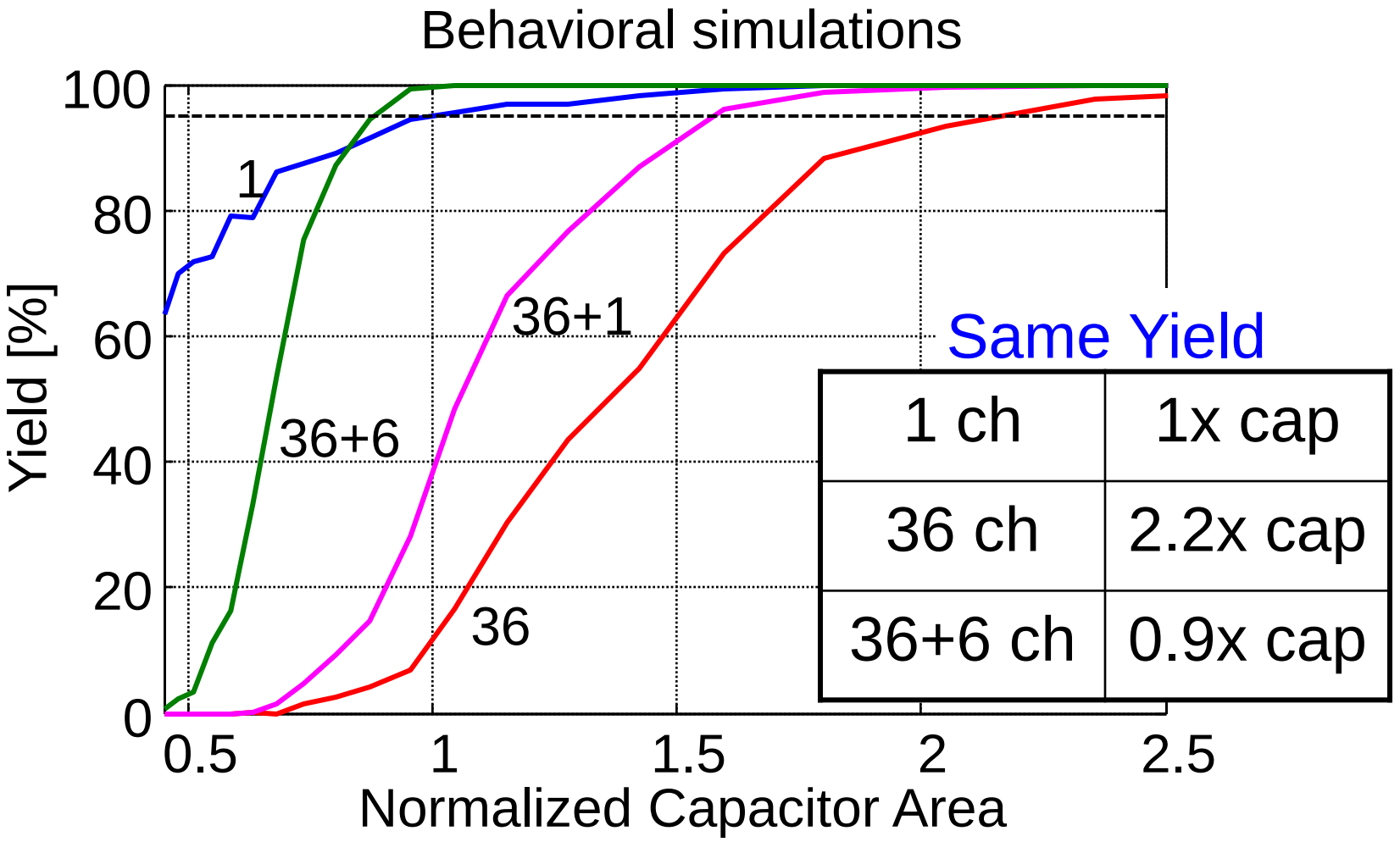
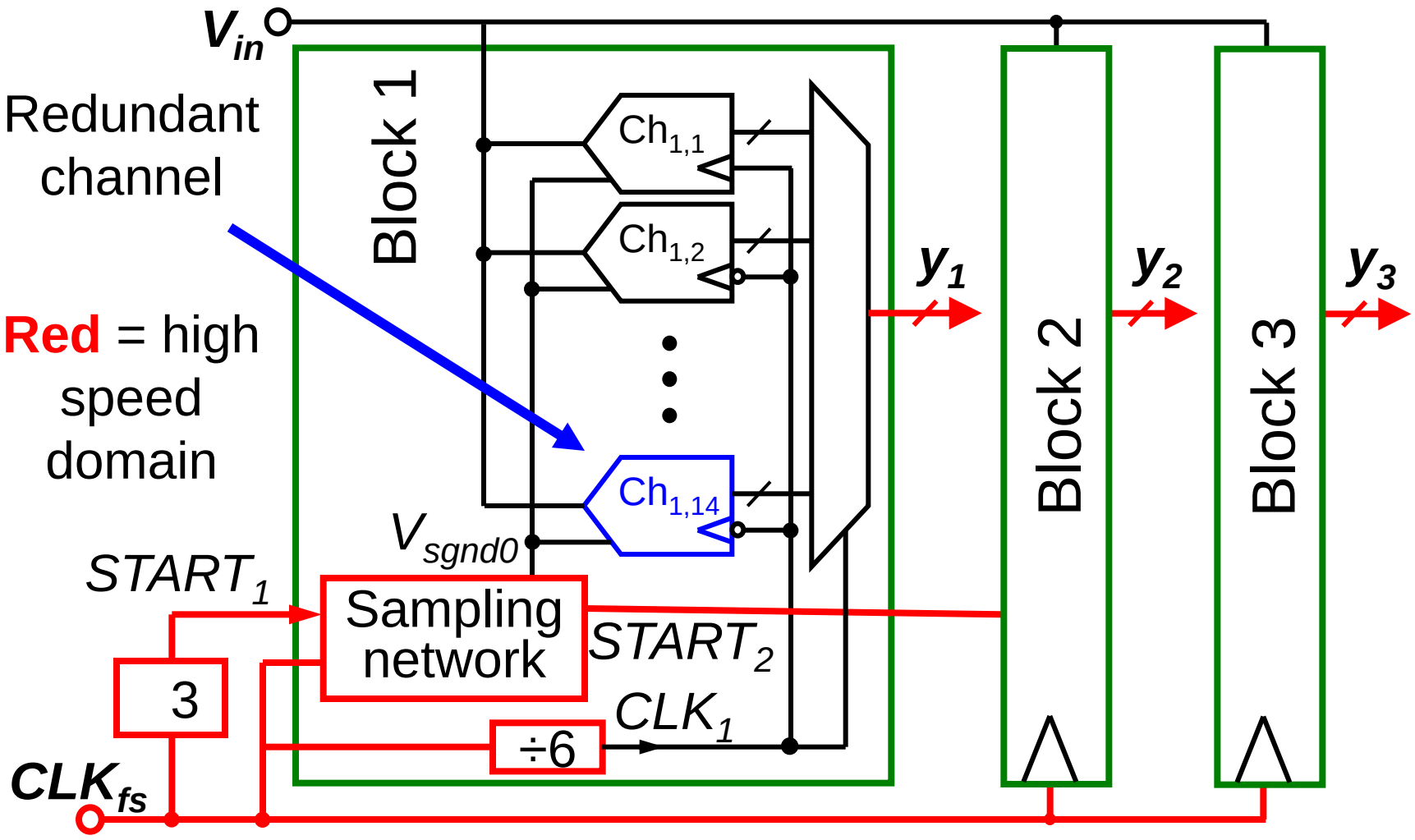
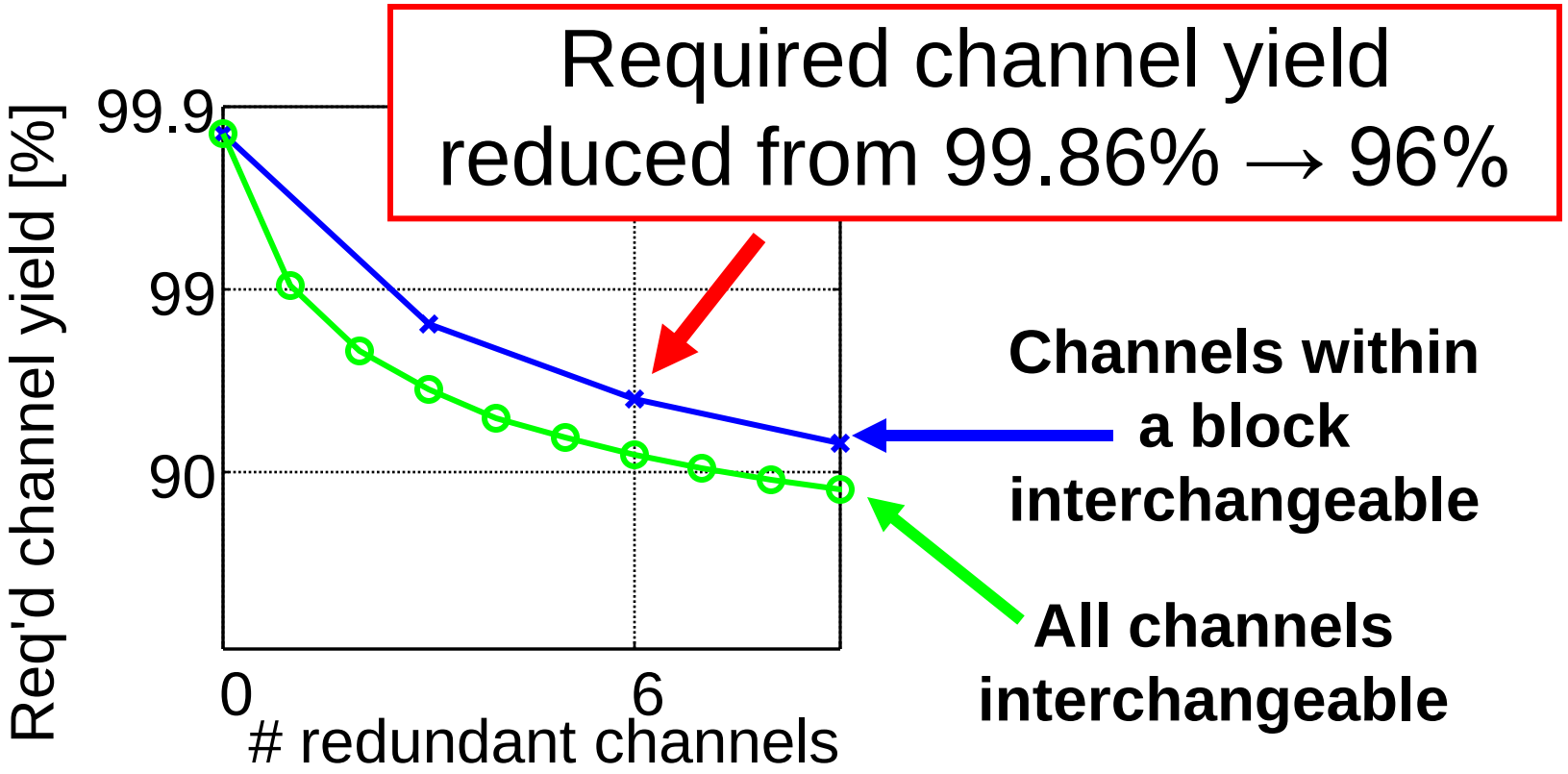


ADC Block Diagram



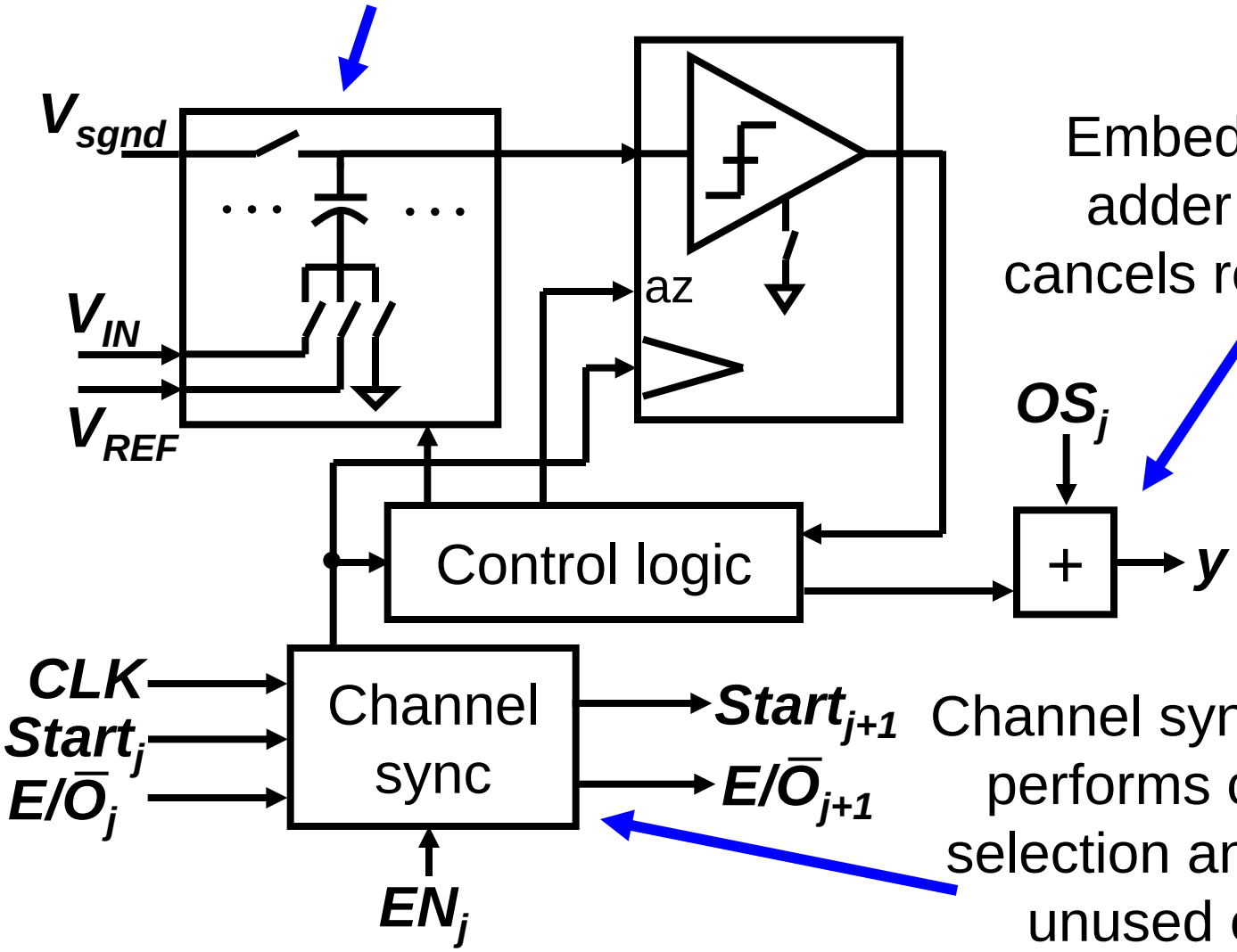
Redundancy and Yield

- Generalization: redundant channels reduce required channel yield for a given overall yield (95%)



SAR Channel Implementation

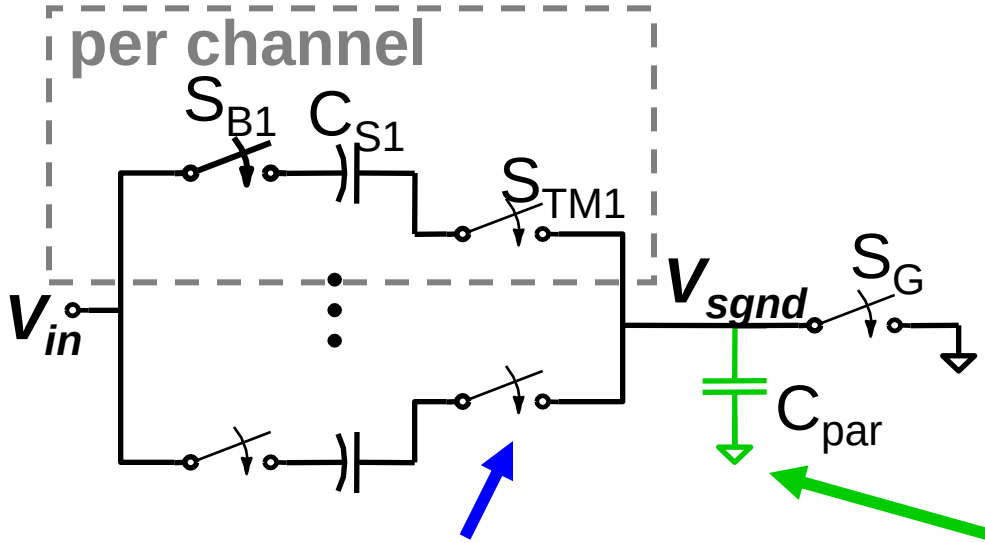
Split capacitor array [Ginsburg, JSSC 4/07]



Embedded digital adder efficiently cancels residual offset

Channel synchronization performs clock edge selection and bypasses unused channels

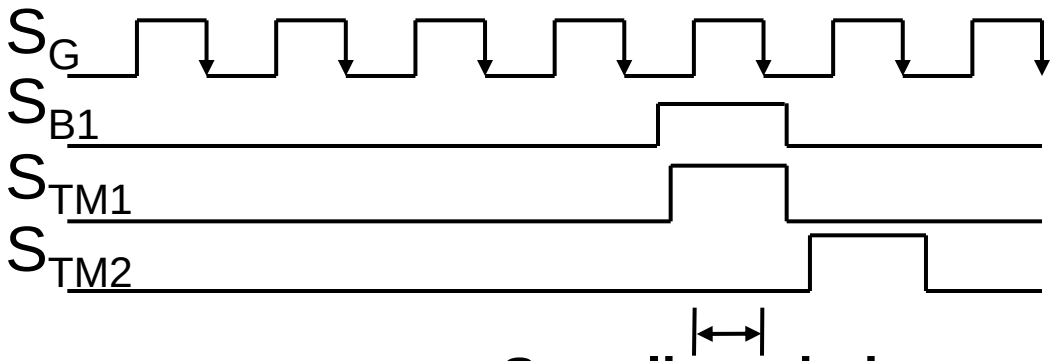
Global Sampling Network



Top-plate switches smaller than bottom-plate

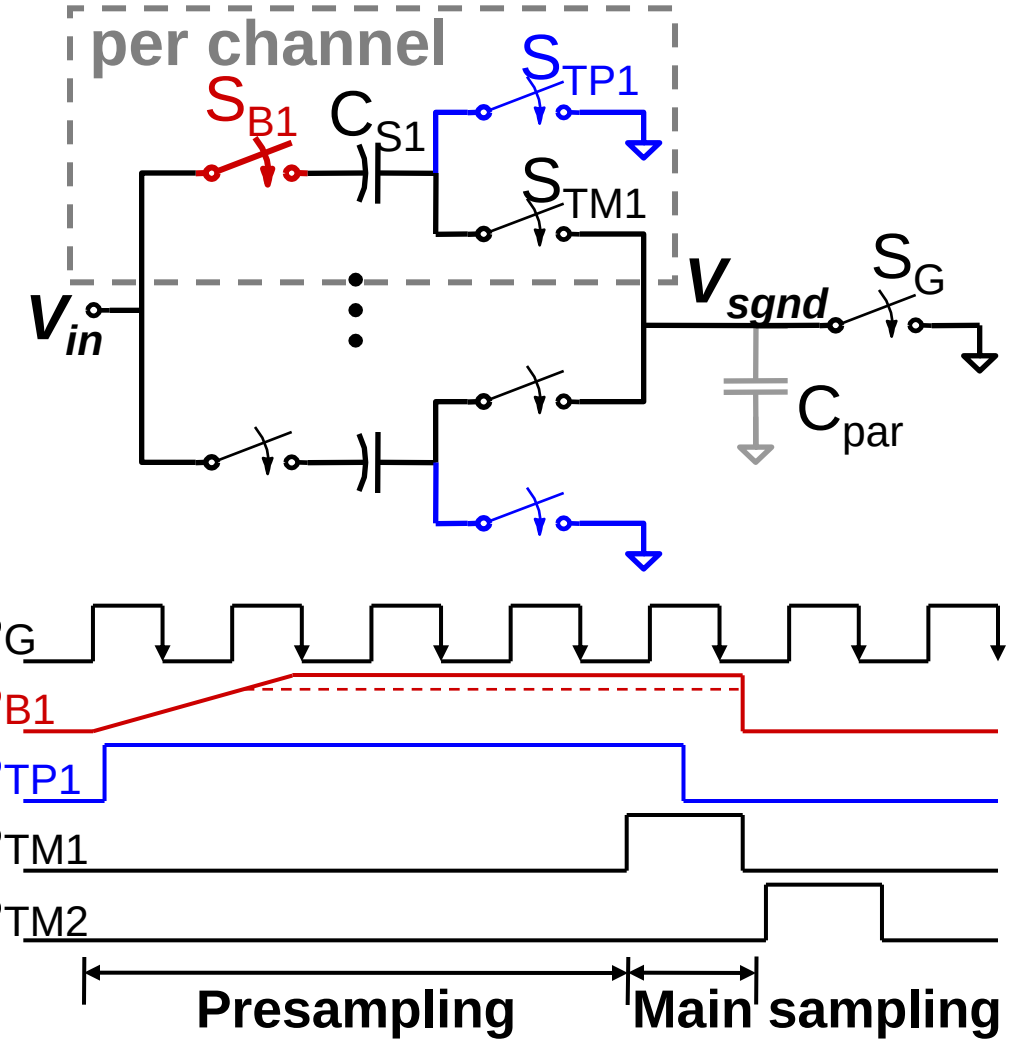
Timing skew minimized by a global switch [Gustavsson, TCAS-II, 9/00] that defines all sampling instants.

Block structure reduces parasitic capacitance that causes residual skew

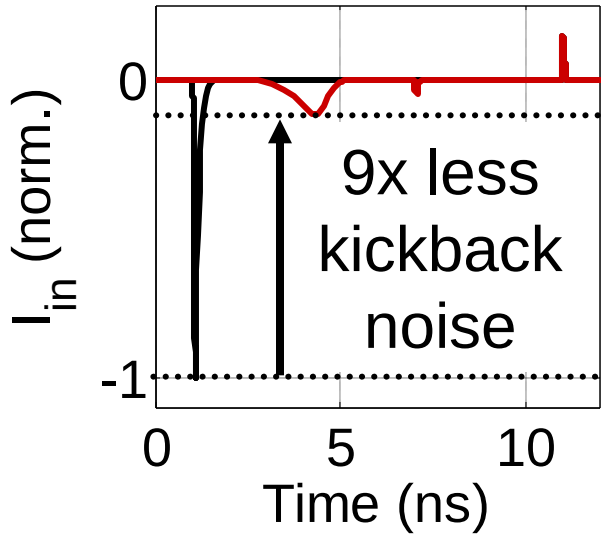


Sampling window

Extended Sampling Network

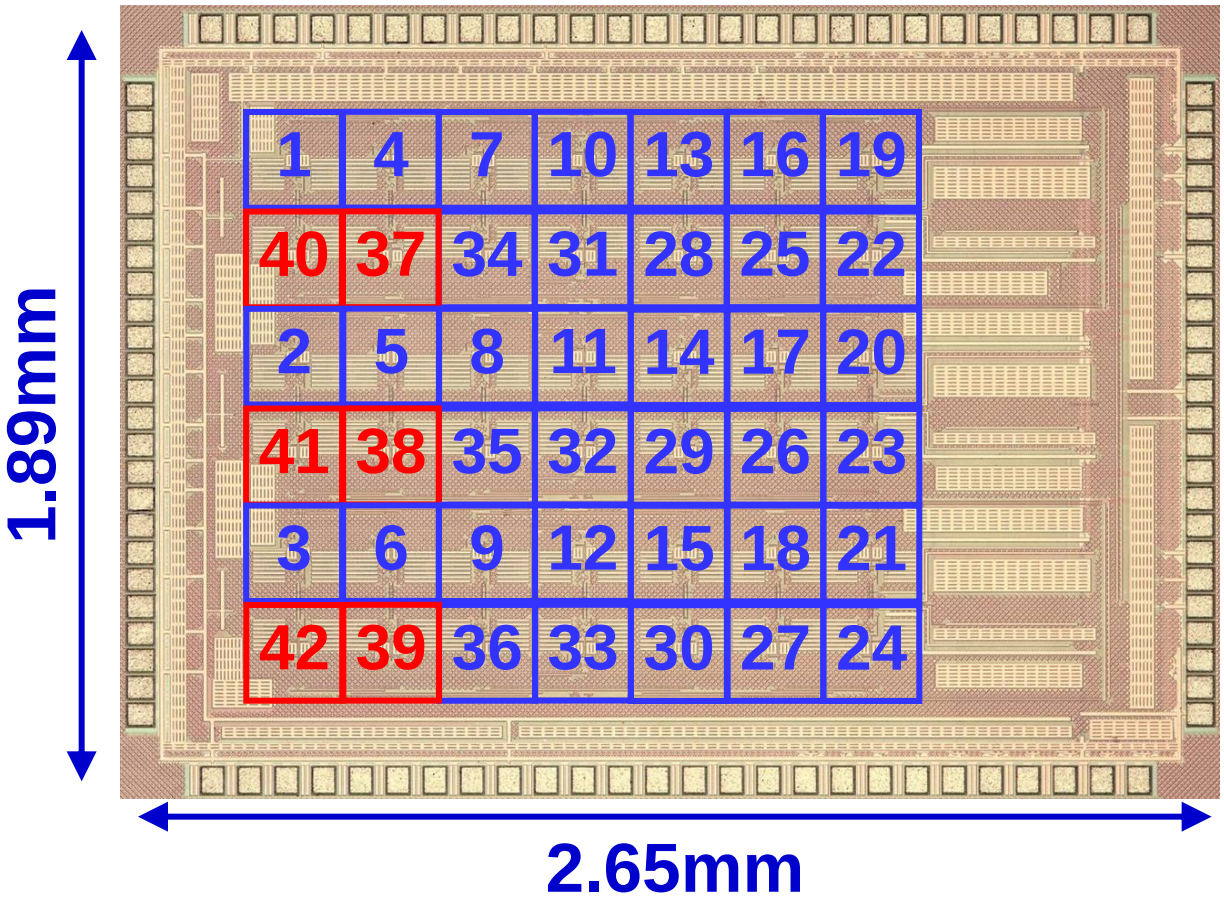


Longer settling time with minimal crosstalk on input and V_{sgnd}



Chip Implementation

65nm CMOS



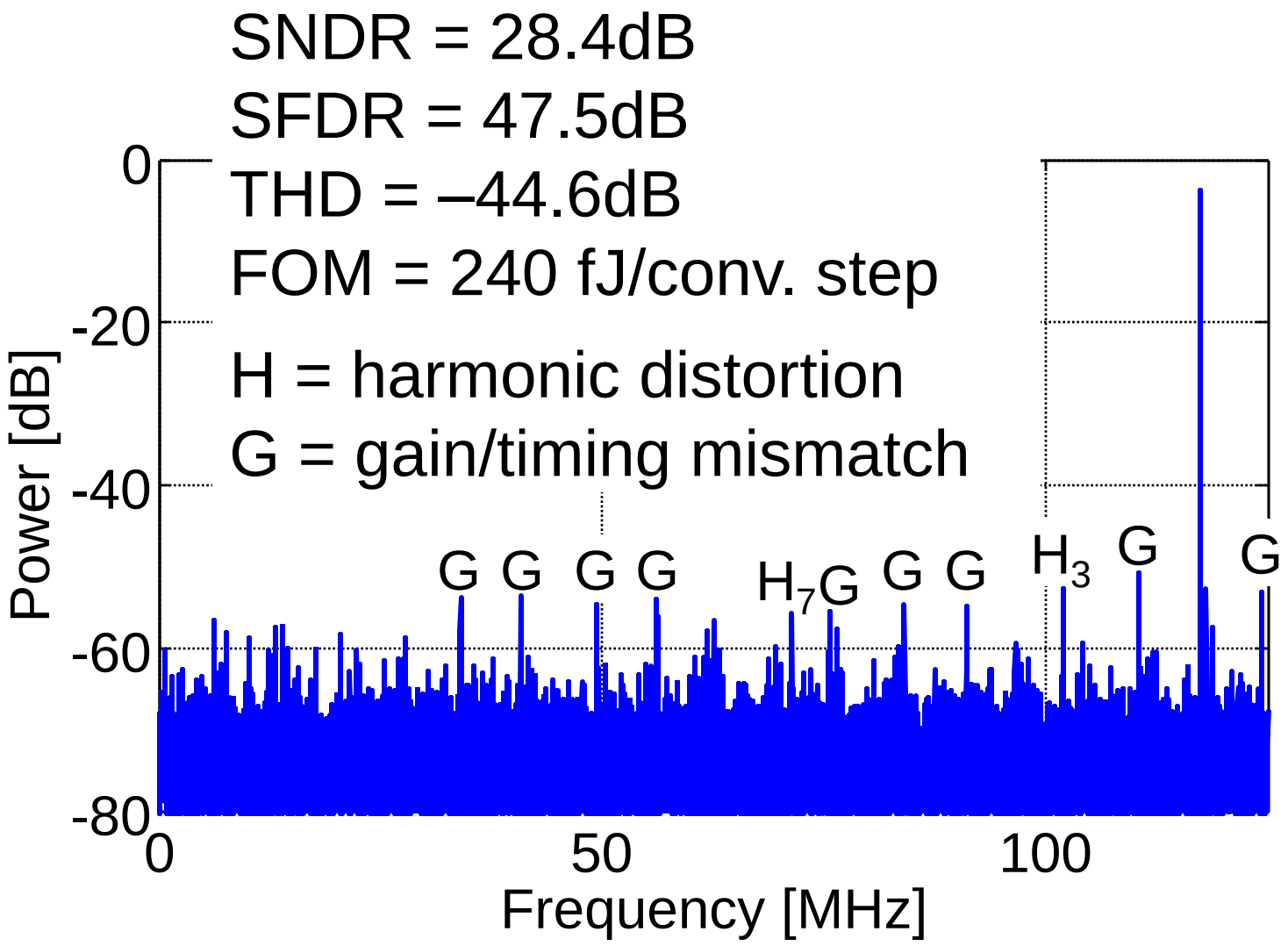
Power at 250MS/s

1.17mA at 0.8V

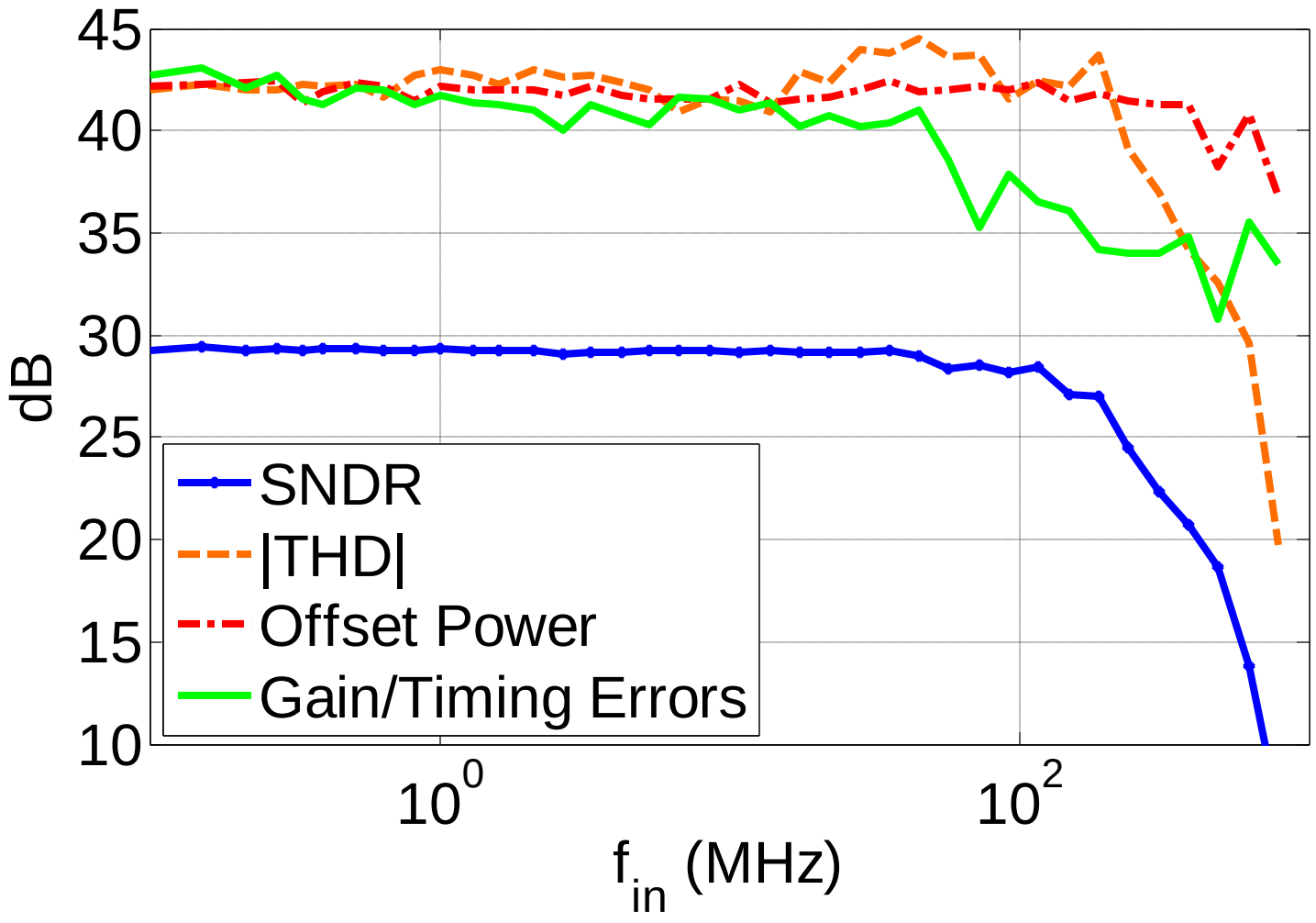
+ 0.2mA at 1.2V (sampling)

1.20mW total

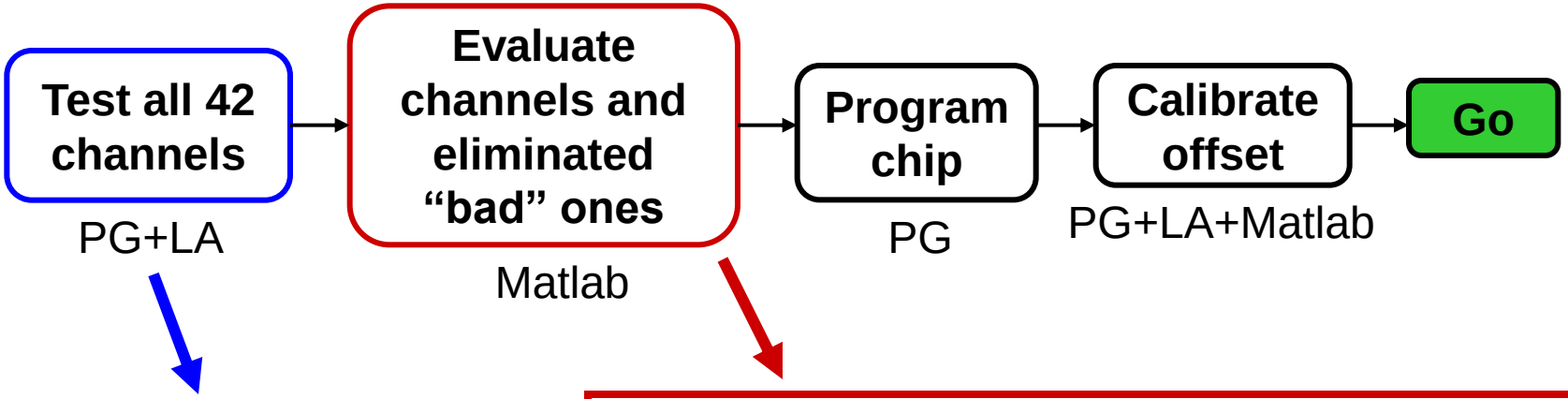
Measured FFT (f_{in} = 117MHz)



Measured Dynamic Performance



Channel Selection Overview

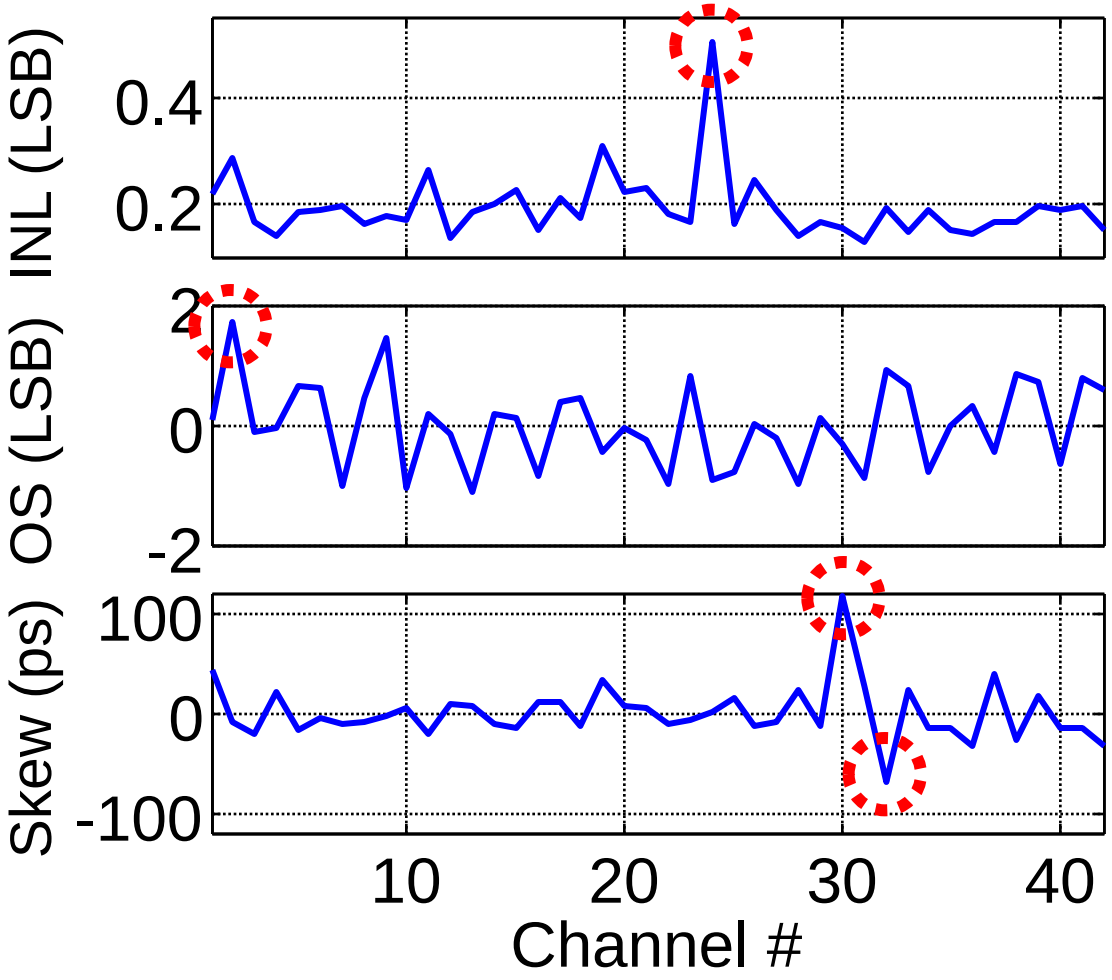


4 tests

- Chs. 1-36 (low-F)
- Chs. 1-36 (high-F)
- Chs. 7-42 (low-F)
- Chs. 7-42 (high-F)

1. Calculate per-channel INL, DNL, SNDR, THD, gain, OS, skew.
2. Assess penalties for marginal/out-of-spec channels.
3. Iteratively eliminate channels with highest penalties.

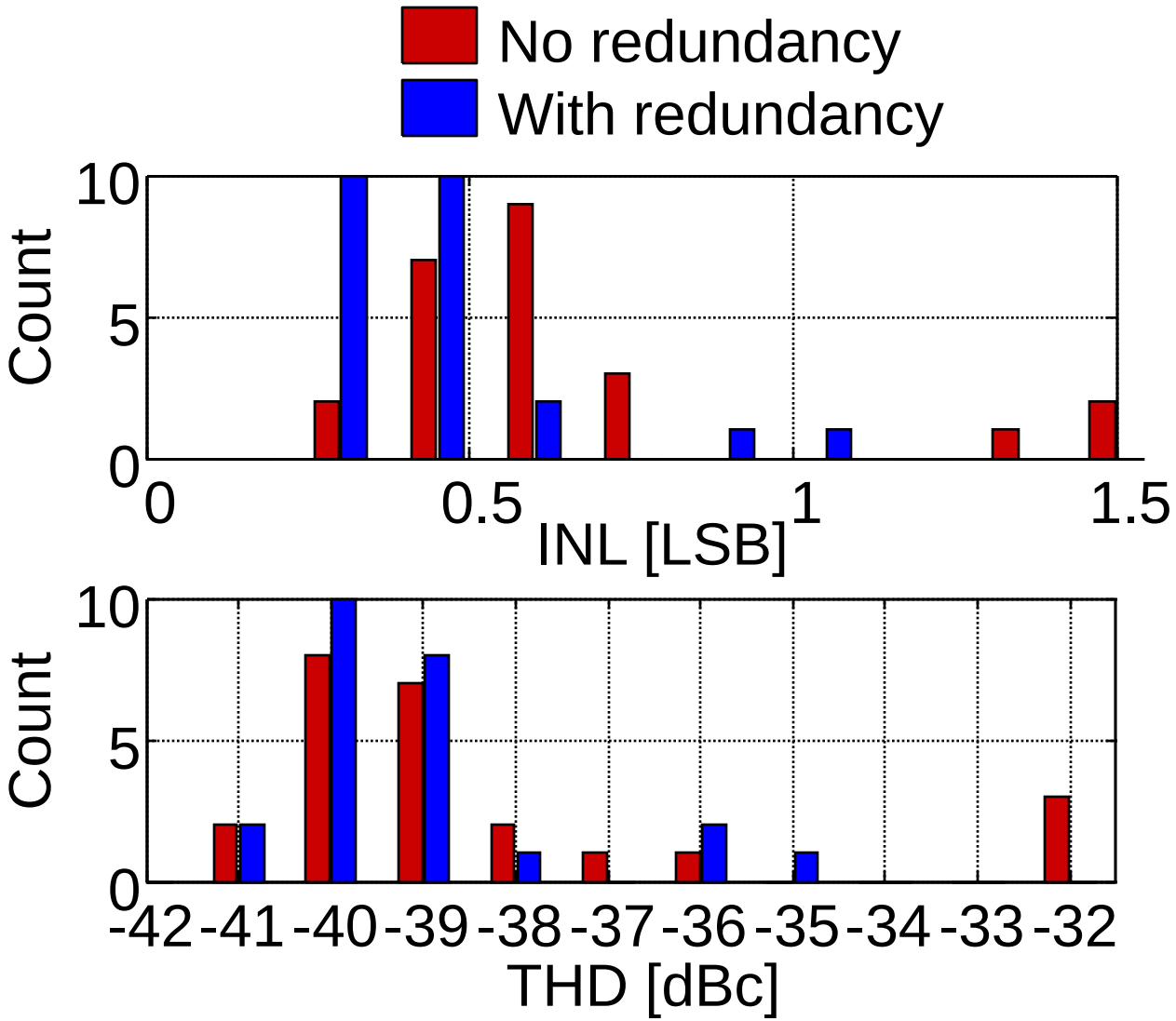
Channel Selection Example



INL	0.50 LSB ↓ 0.31 LSB
$OS_{p\text{-}p}$	2.8 LSB ↓ 2.0 LSB
δt_{rms}	28.5 ps ↓ 18.8 ps

before/after channel selection

Histograms Across Chips



Histograms show the worst active channel on the chip

Total Yield

Metric	Specification (every channel)	Yielding Chips out of 24	
		No redundancy	With redundancy
INL	≤ 0.6 LSB	14	21
Offset	≤ 2 LSB	19	24
SNDR	≥ 27 dB	19	22
THD	≤ –33 dBc	21	24
All Specifications		10	**21**

Redundancy improves yield from 42% → 88%

Conclusions

- Slower ADCs are more energy efficient due to sub-threshold operation and voltage scaling
- Redundancy is an extremely powerful tool to counteract yield loss from local variation
  - Apply redundancy at the maximum level of parallelism
- Demonstrated a global sampling network with long sampling windows and small crosstalk

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