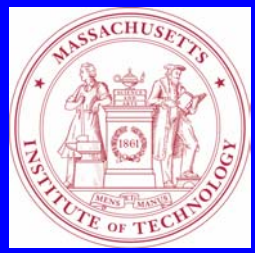
A 500MS/s 5b ADC in 65nm CMOS



Brian P. Ginsburg and Anantha P. Chandrakasan

Massachusetts Institute of Technology Microsystems Technology Laboratory

Symposium on VLSI Circuits

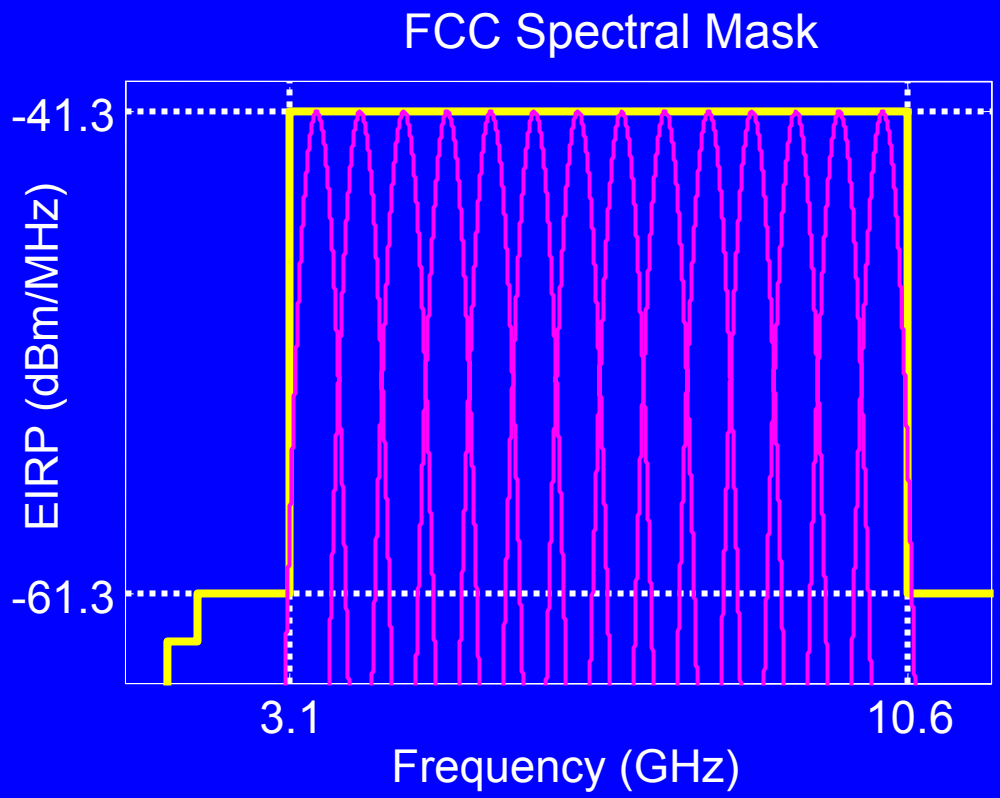
Honolulu, HI

June 16, 2006

Table of Contents

Ultra-Wideband Radio

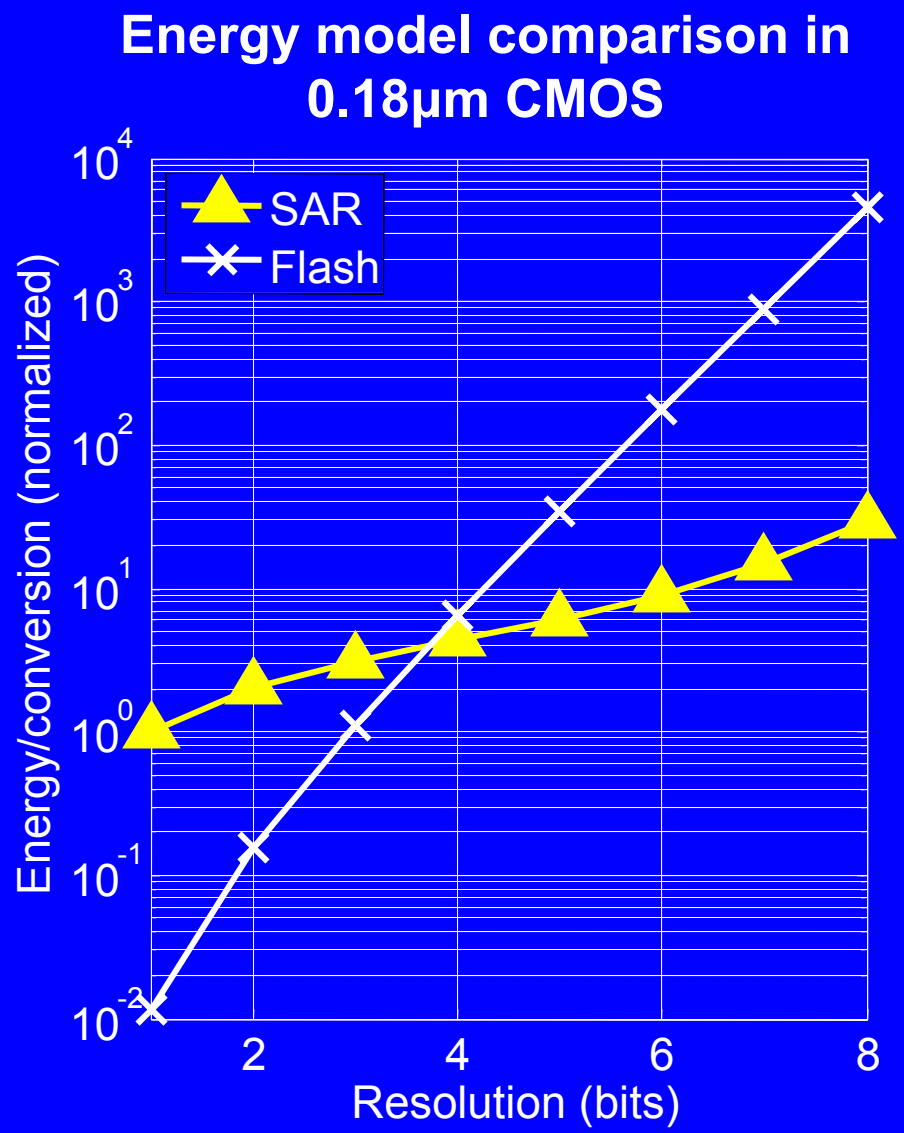
- **FCC specifications**
  - **– >500MHz 10dB bandwidth**
  - **– Very low average power density**
- **Research targets a system that transmits pulses in 500MHz channels.**



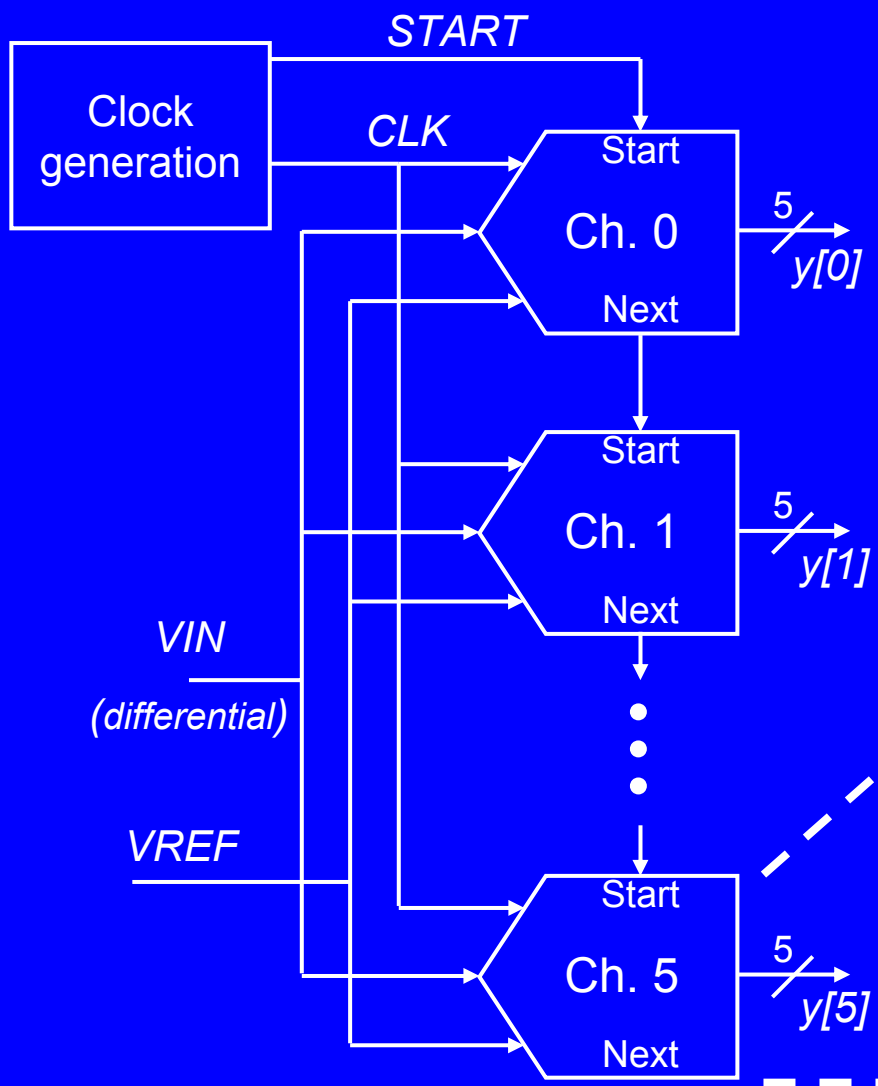
Specifications: 5b, 500MS/s

Architecture Selection

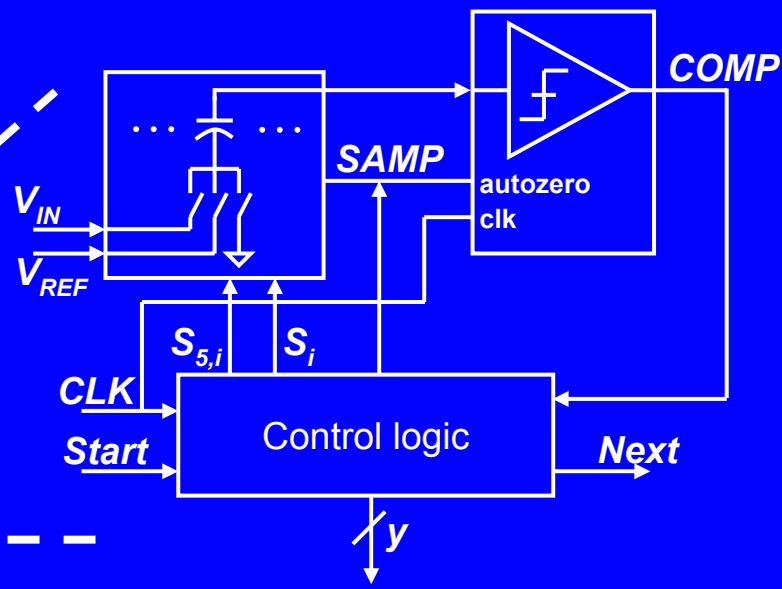
- Flash is traditional architecture for 500MS/s, 5b operation
  - Exponential # of comparators
- Successive approximation register (SAR) architecture
  - Linear # of comparisons
  - Feedforward comparator
  - Time-interleaving required for throughput



Architecture: Parallel SAR



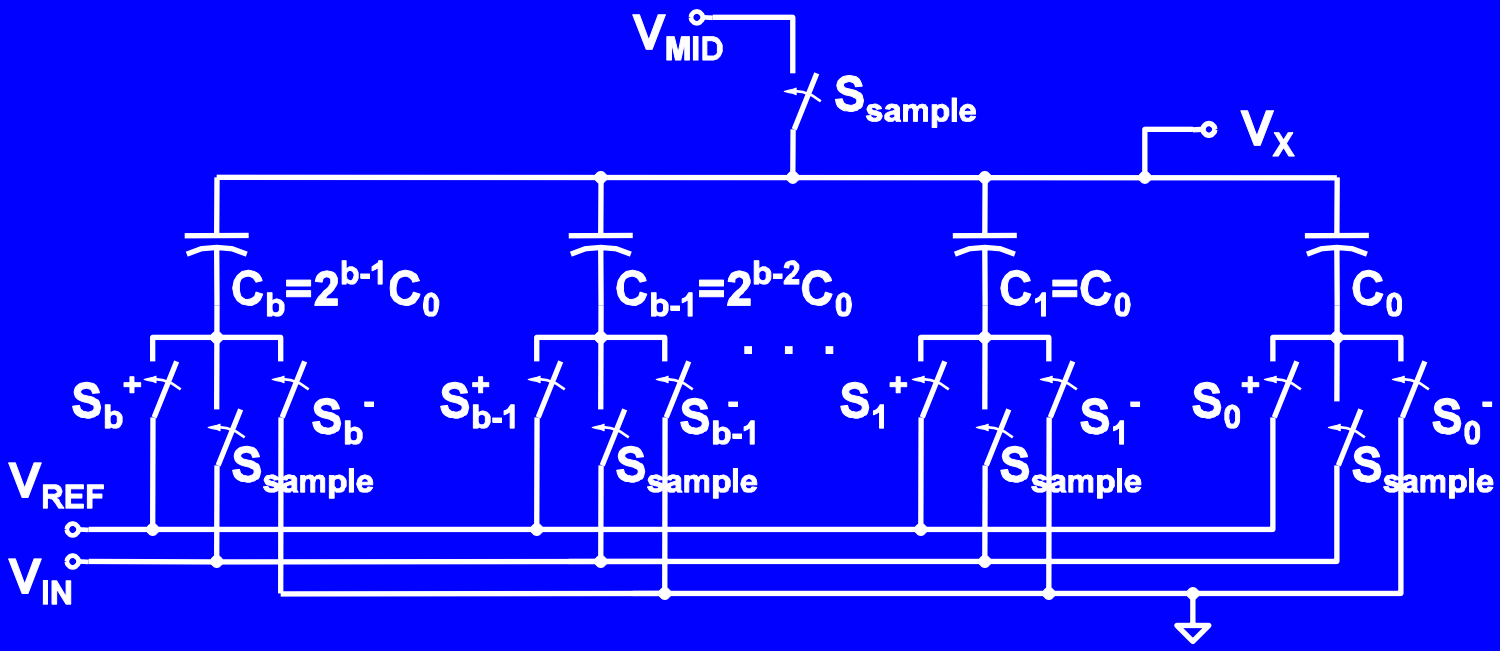
- **All critical sampling edges aligned to common 500MHz clock.**
- **Start token and clock are the only synchronization between channels.**



Technology Considerations

- Challenges
  - Reduced power supplies (1.2V maximum)
  - Increased device variation/mismatch
  - Lower output impedance
- SAR architecture well suited to advanced processes
  - Use non-minimum length transistors throughout comparator to improve matching and $g_m r_o$.
  - NMOS only sampling with low reference voltage of 0.4V.
  - Fully static CMOS digital implementation for SAR controller

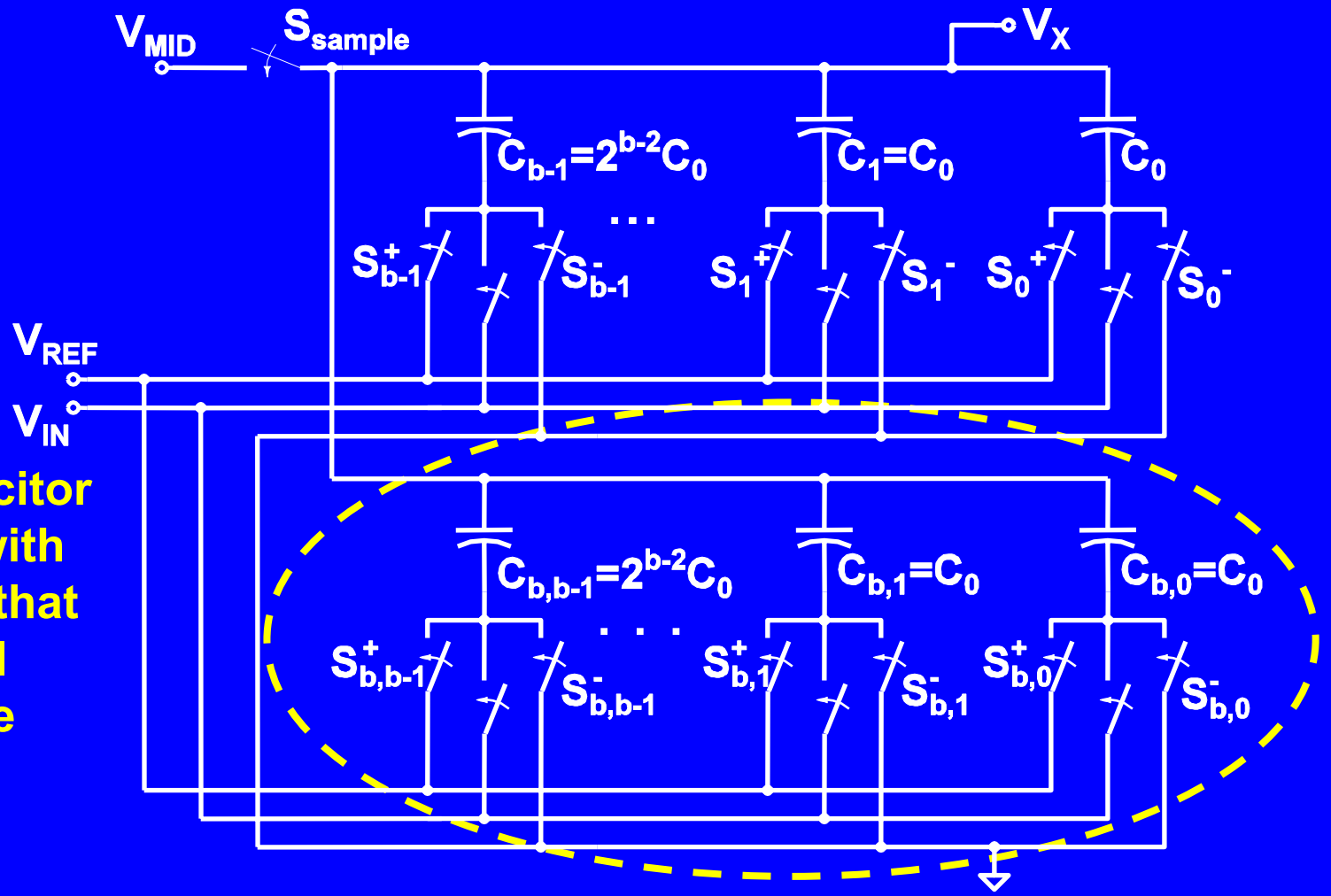
Conventional Capacitor Array



- b-binary weighted capacitors with an extra unit capacitor.
- Samples the input and used as the feedback DAC during bit decisions:

$$V_X = V_{MID} - V_{IN} + \frac{\sum_{i=0}^{b-1} 2^i d_i C_0}{2^b C_0} V_{REF}$$

Split Capacitor Array



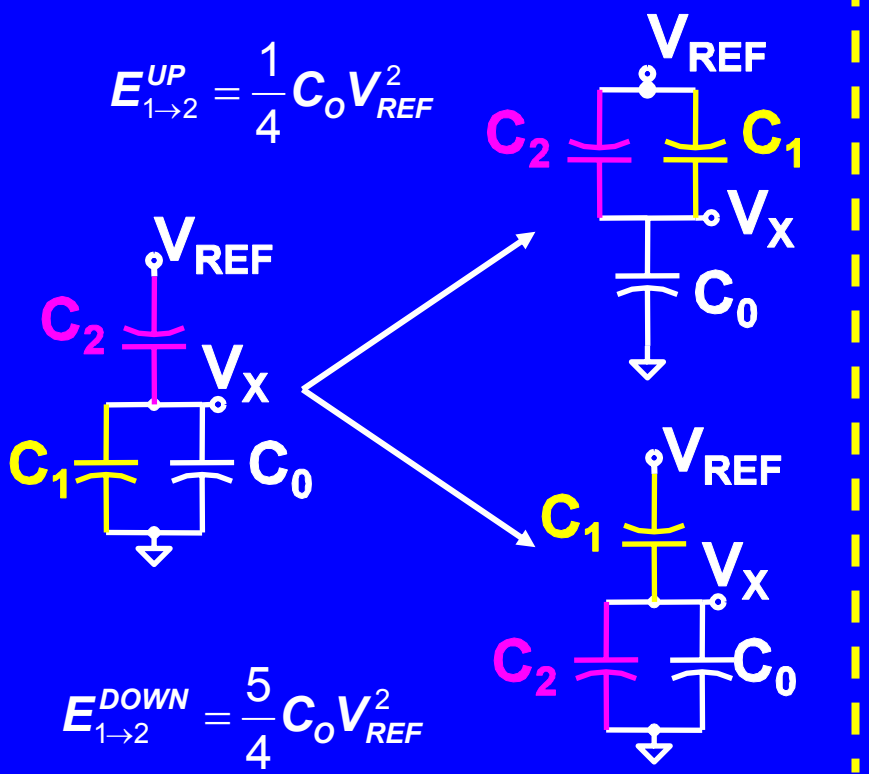
MSB capacitor replaced with sub-array that is identical copy to the rest of the array.

- Total array capacitance and area requirements unchanged.
- Theoretical analysis in [Ginsburg, ISCAS 2005]

Split Capacitor Switching Technique

Conventional Array

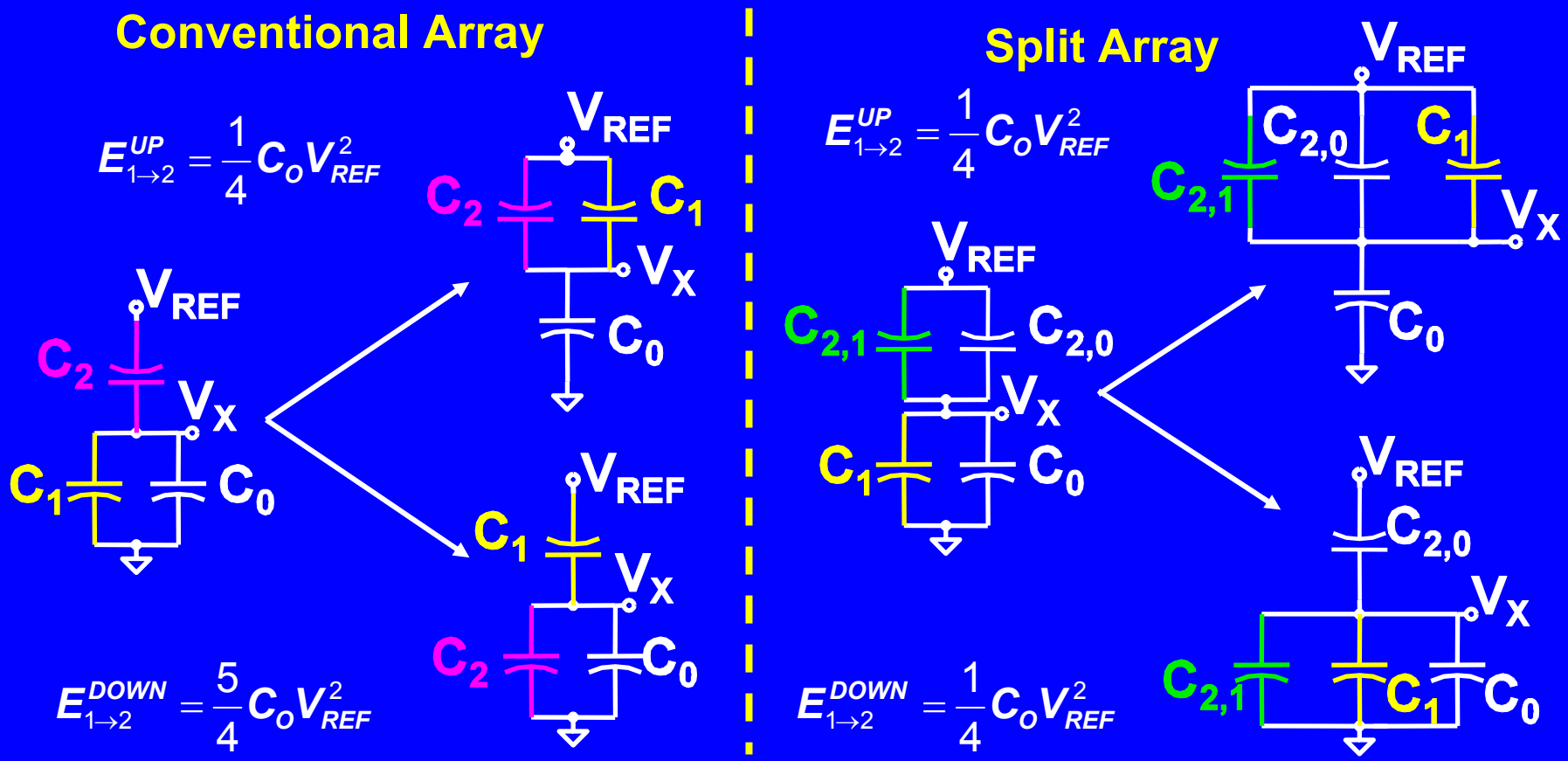
$$E_{1\rightarrow 2}^{UP} = \frac{1}{4} C_O V_{REF}^2$$



$$E_{1\rightarrow 2}^{DOWN} = \frac{5}{4} C_O V_{REF}^2$$

Split Array

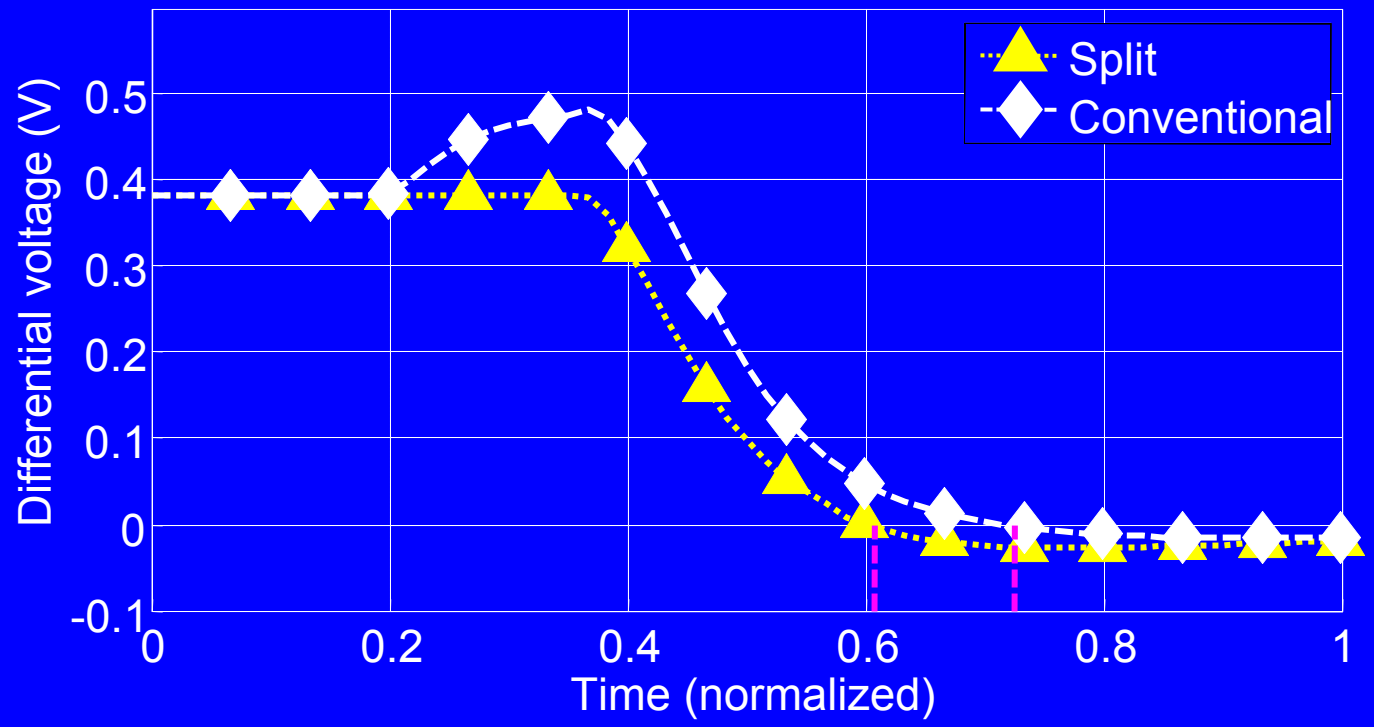
Split Capacitor Switching Technique



Reduces switching energy drawn from V_{REF} by 37%.

Capacitor Array Settling Time

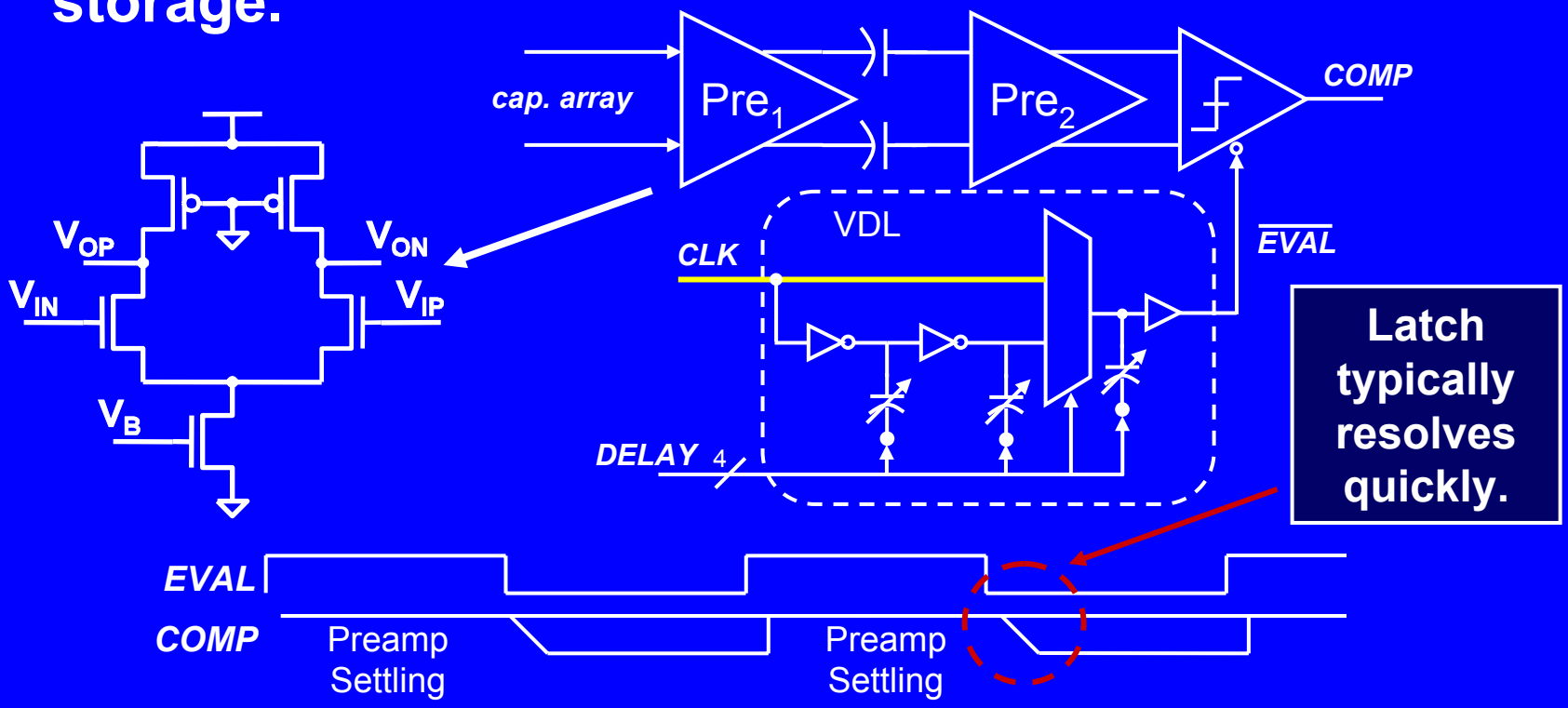
- **A “down” transition requires two switching events, which, for the conventional capacitor array, can be mismatched in time.**



Up to 10% speed improvement

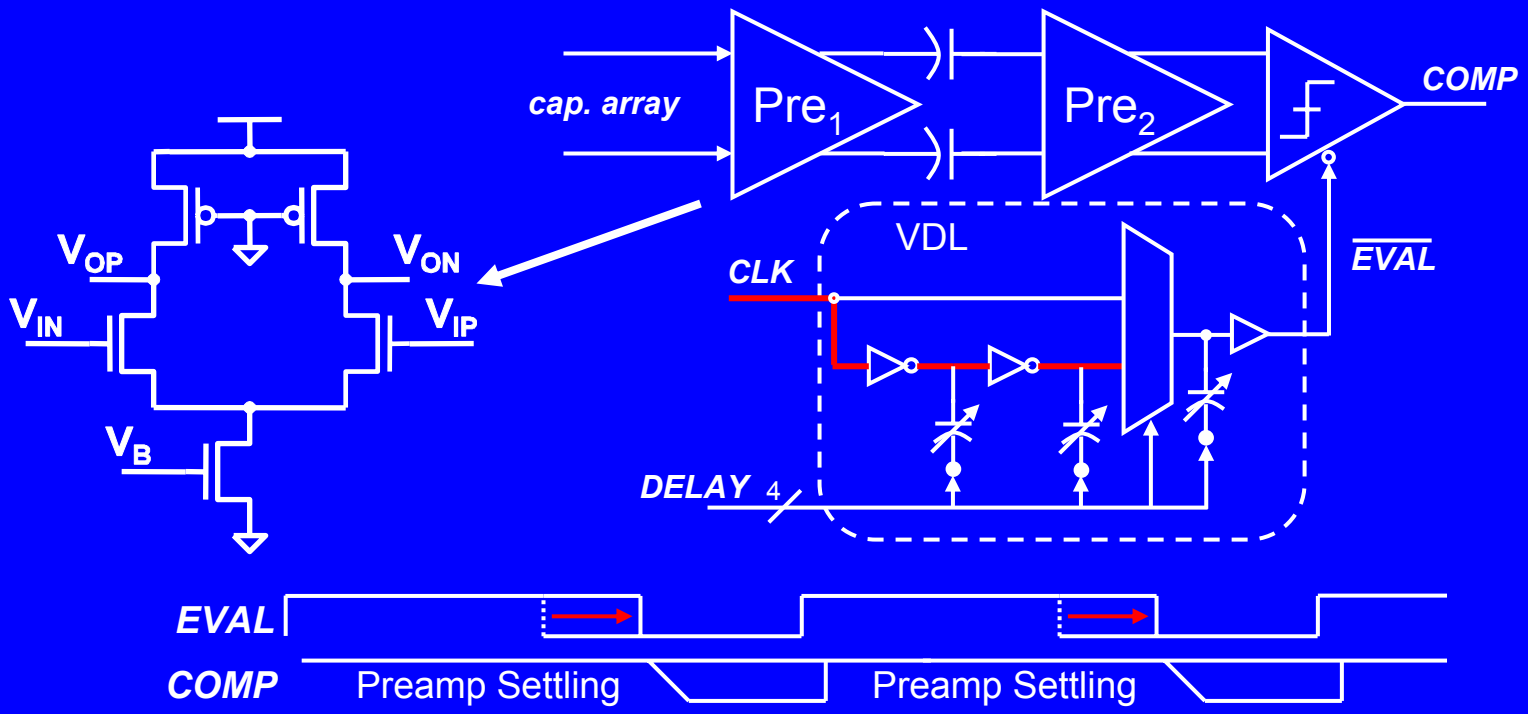
Comparator

- Preamplifiers' gain and speed requirement set to amplify input beyond offset of the regenerative latch within the settling period.
- Preamplifier offset reduced through output offset storage.



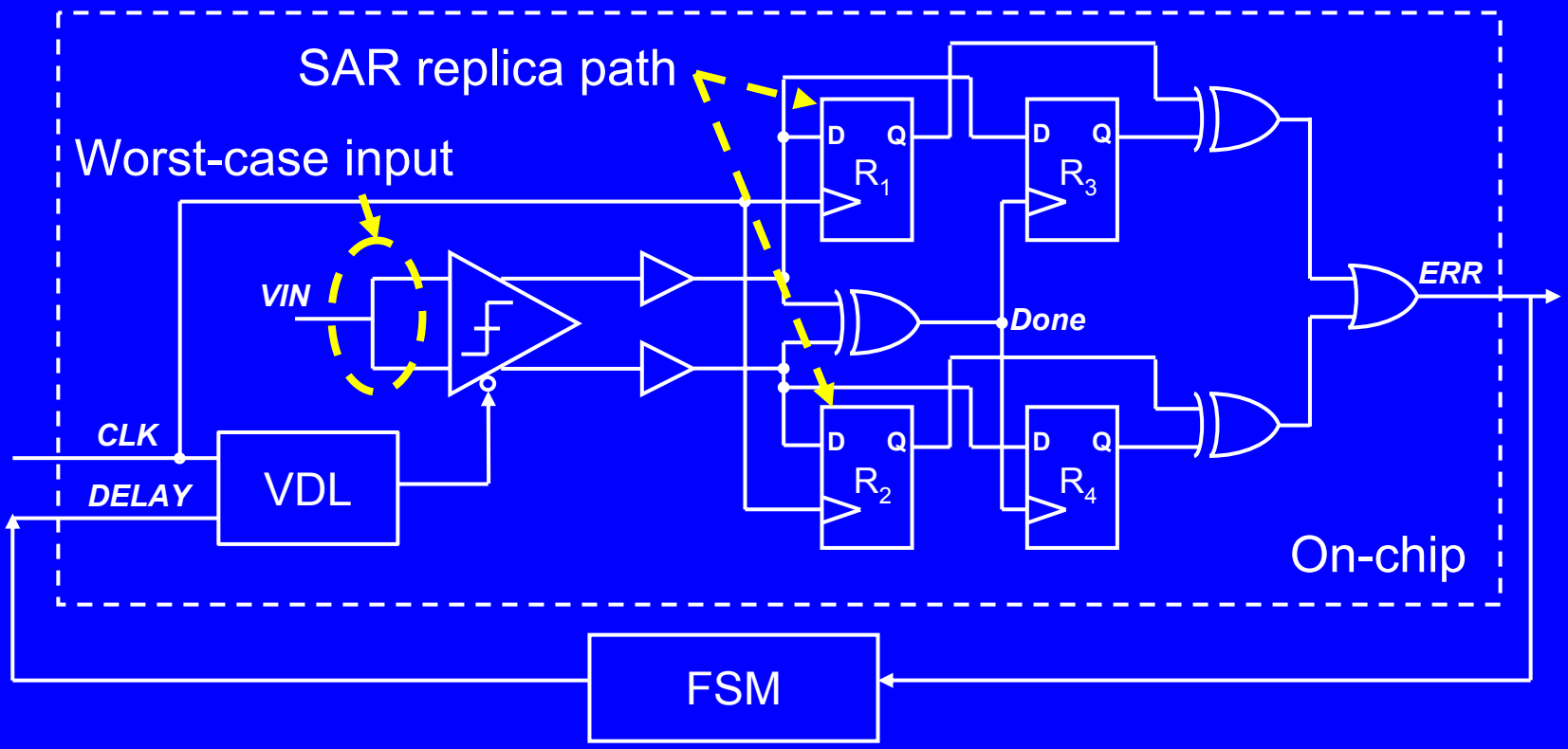
Optimized Latch Strobing

- Delay the onset of latch regeneration, shifting time from the end of the period to the beginning.
- Preamplifier currents can be reduced without sacrificing linearity.



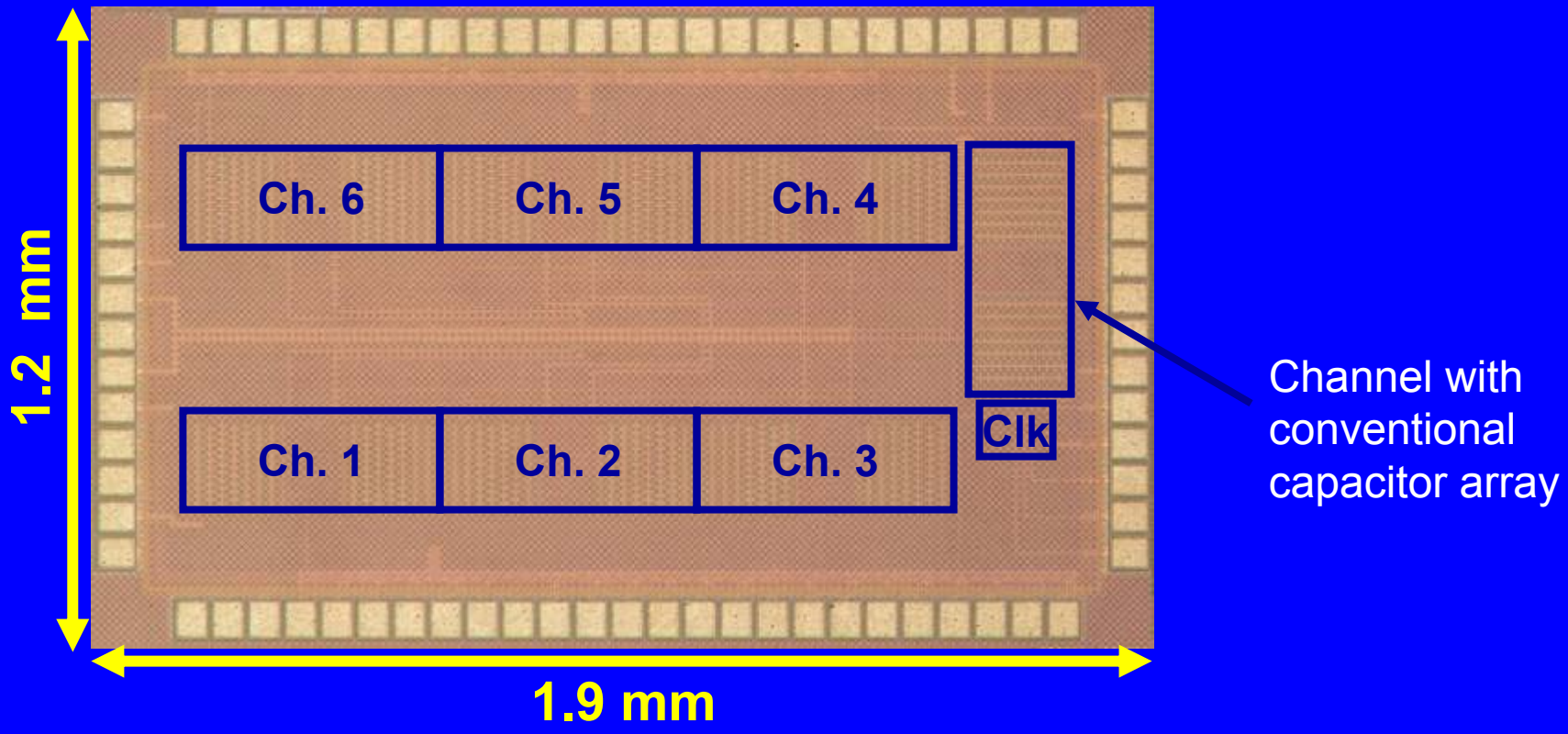
Delay Detection

- The delay can be fine tuned using an on-chip circuit combined with an off-chip FSM.
- On-chip, an FSM would require a counter and simple logic to adjust the delay for a desirable bit error rate.

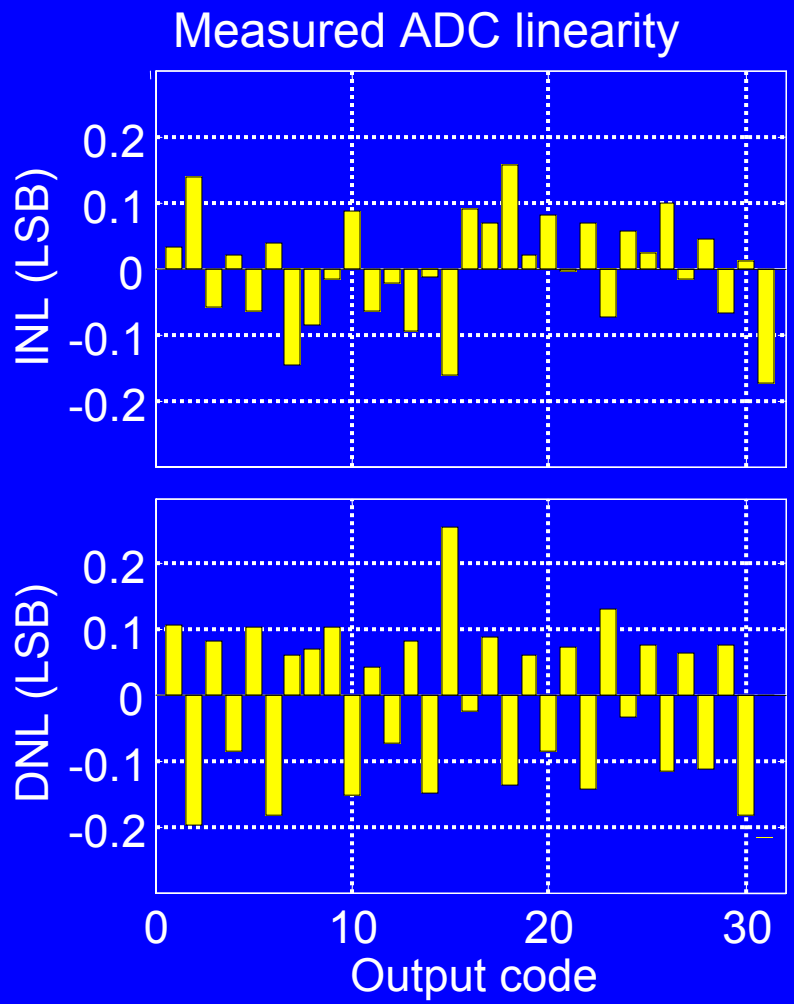


Prototype

- **Prototype fabricated in digital 65nm CMOS.**
  - **Interdigitated metal comb capacitors**



Static Results

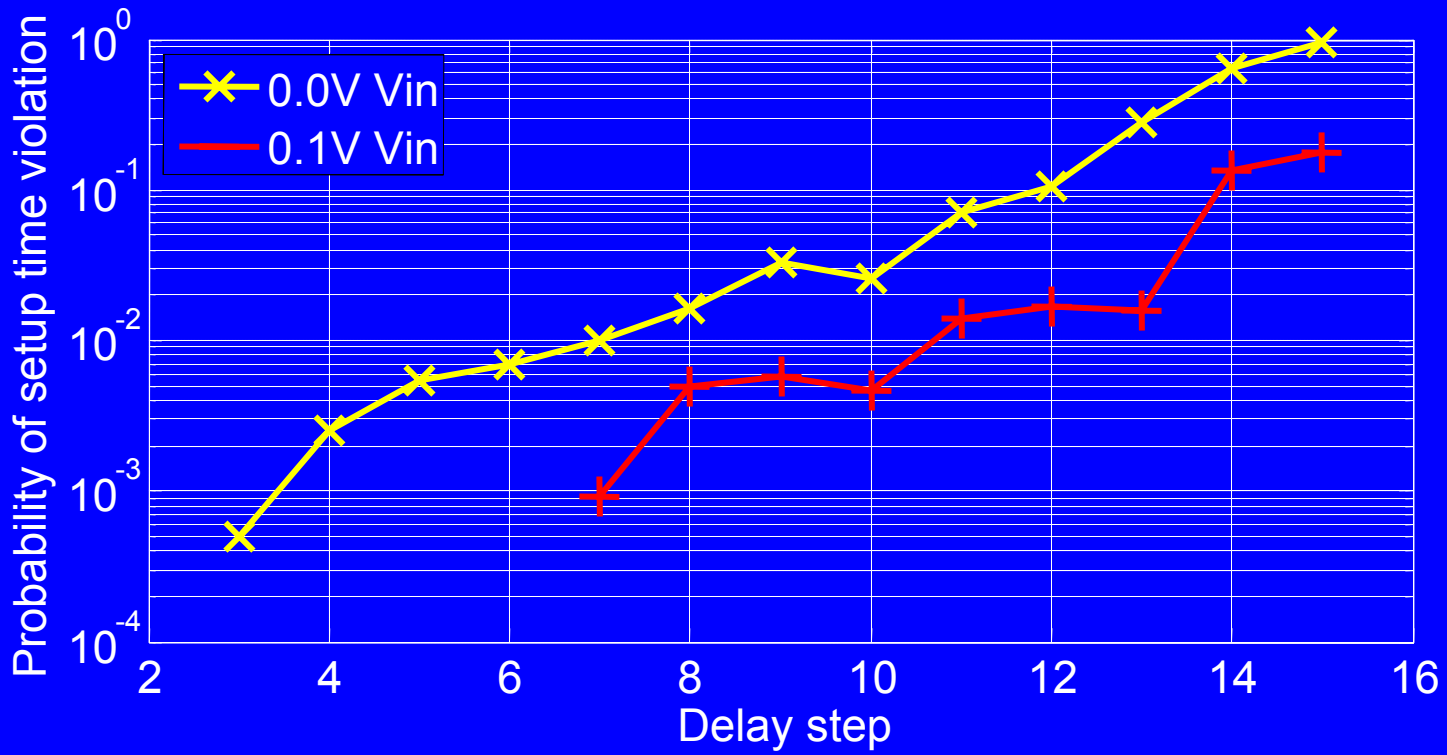


- **Code density test at 500MS/s**
  - **Split capacitor array shows no linearity degradation versus conventional array.**

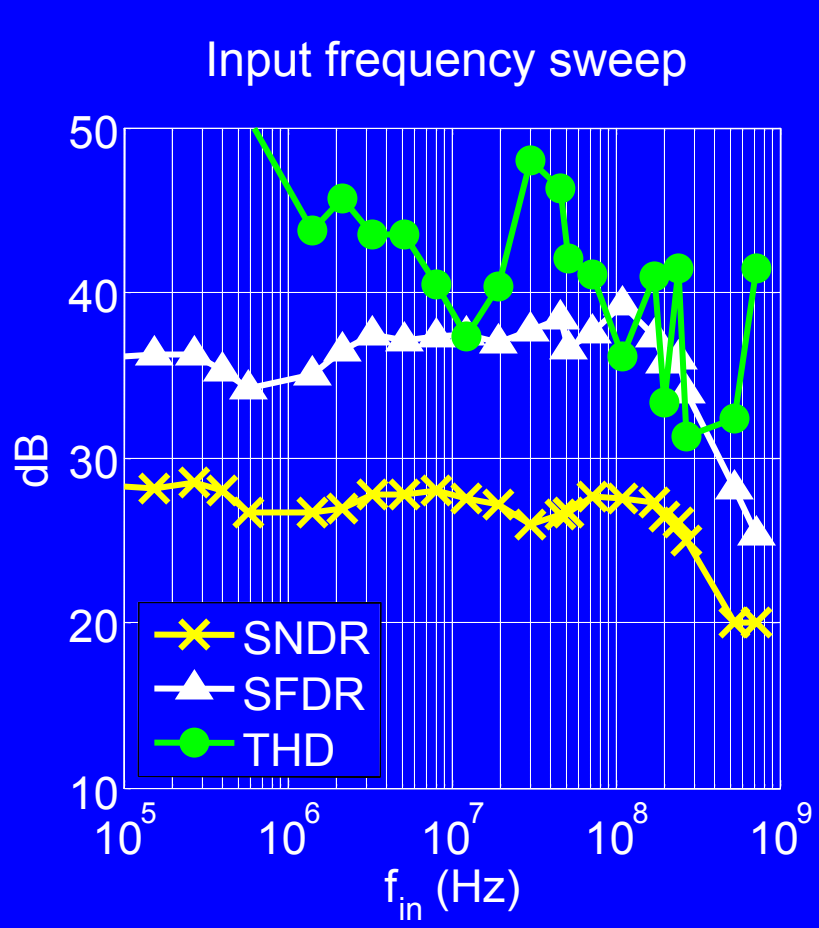
31% savings in switching energy from V_{REF} supply

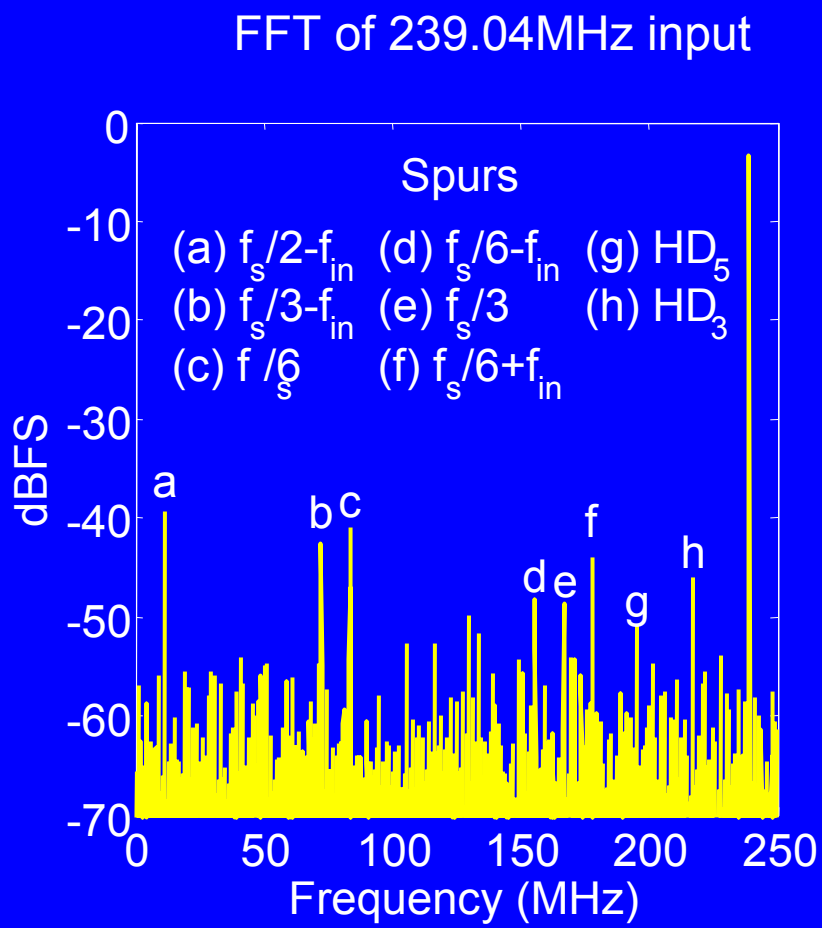
Latch Delay Detection

- For 500MS/s operation, optimal delay step is 0 or 1 (P_e<<10^{-6}), which extend analog settling by 10%.
- At 250MS/s clock frequency, setting the delay optimally improves SNDR by 1dB.



Dynamic Performance (500 MS/s)

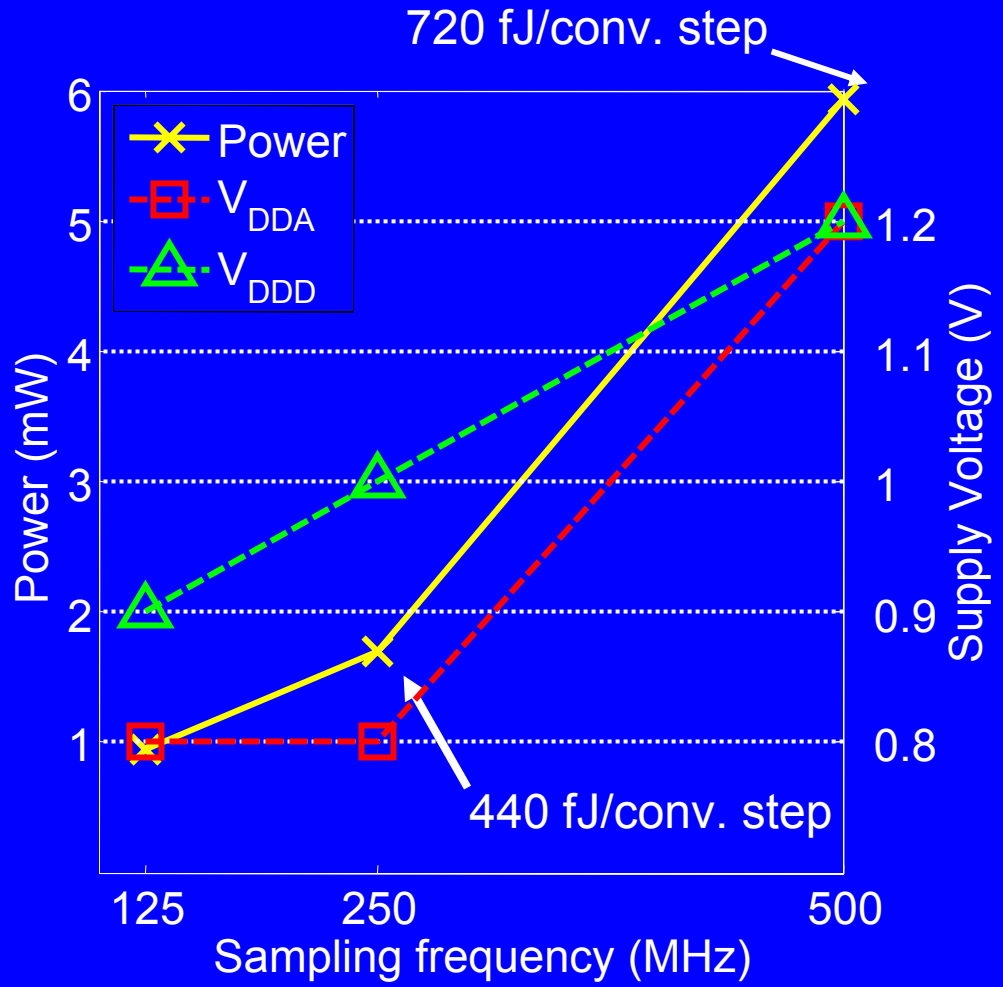




Nyquist performance; time-interleaving spur power still below total noise power at 250MHz input

Power consumption

- **Full Nyquist performance at 4 ENOB**
- **At peak performance, analog and digital power supplies each use 3mW.**
- **Peak energy efficiency at lower voltage/speed**



Conclusions

- Successive approximation register architecture well suited for deep sub-micron CMOS.
- Charge conservation techniques can reduce power and improve speed in mixed signal circuits.
- Joint timing optimization of analog and digital improves performance.

Acknowledgments

- Texas Instruments for chip fabrication
- NDSEG Fellowship
- DARPA