A Baseband Processor For Pulsed Ultra-Wideband Signals

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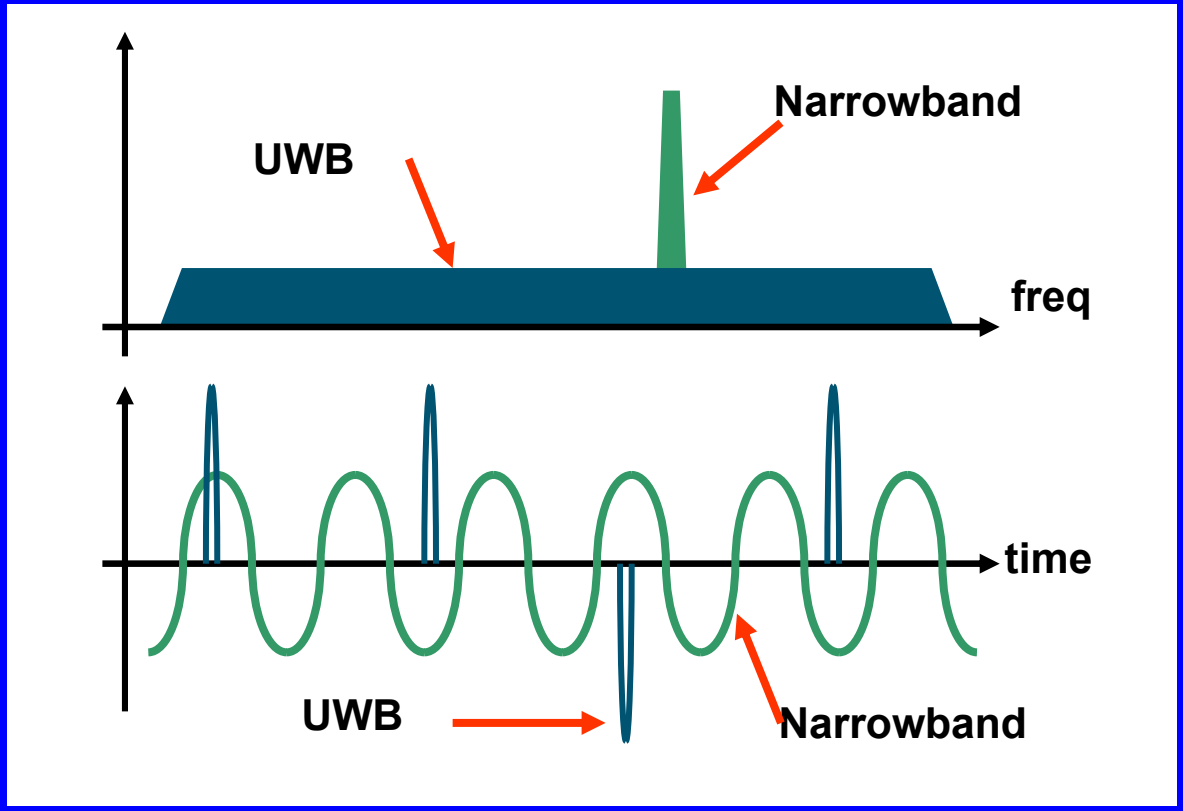
Outline

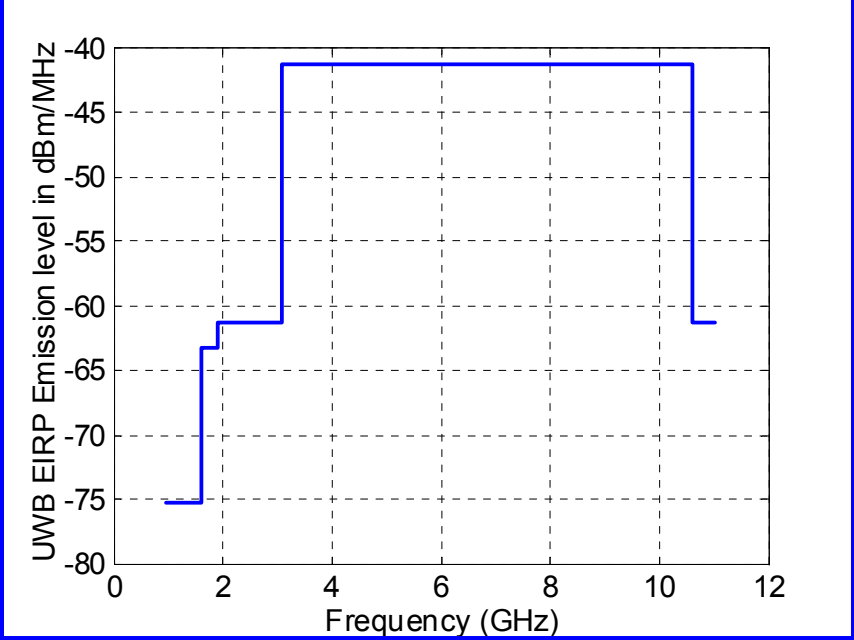
- Introduction to UWB Systems
- Baseband Processor
- Analog to Digital Converter
- Clock Generation System
- Digital Backend
- Results and conclusions

UWB systems

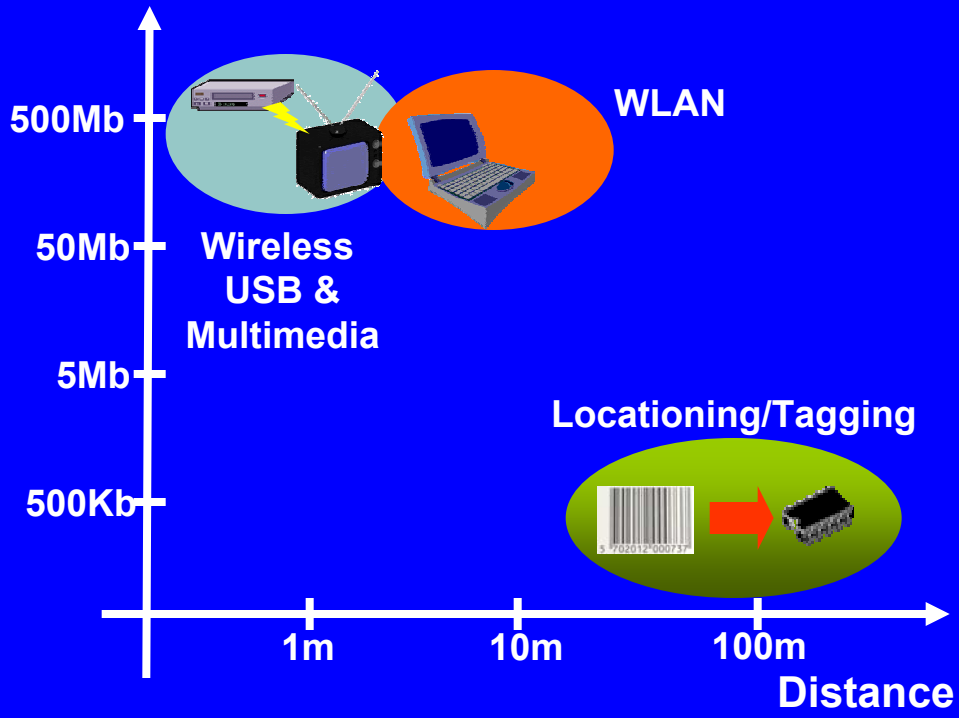


High Data Rate
Excellent Multipath Resolution
Low interference to other systems

Free Unlicensed Spectrum

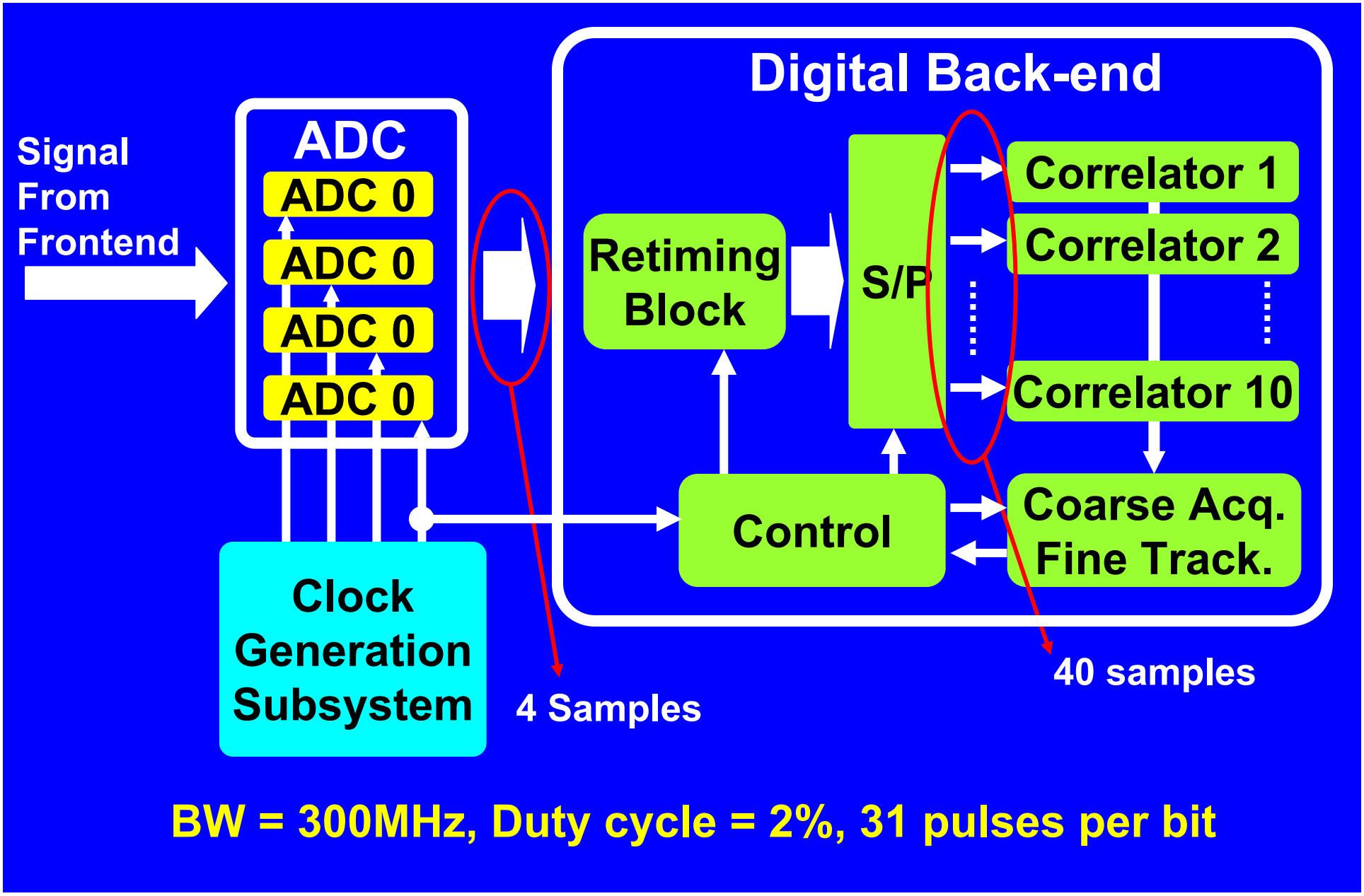


Spectrum allowed for communication



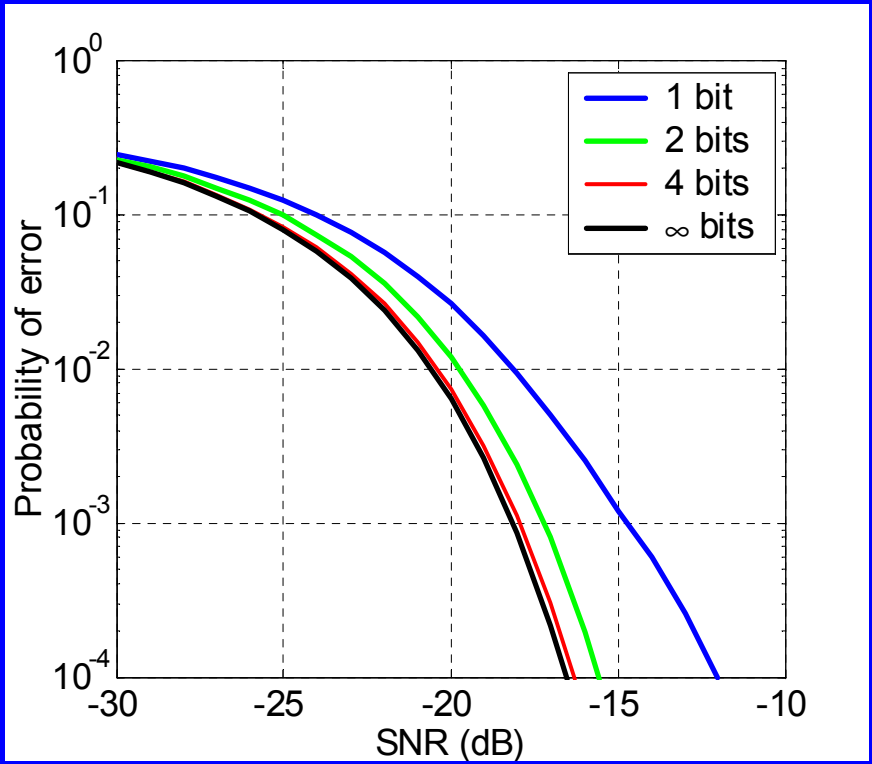
Two IEEE standards in development

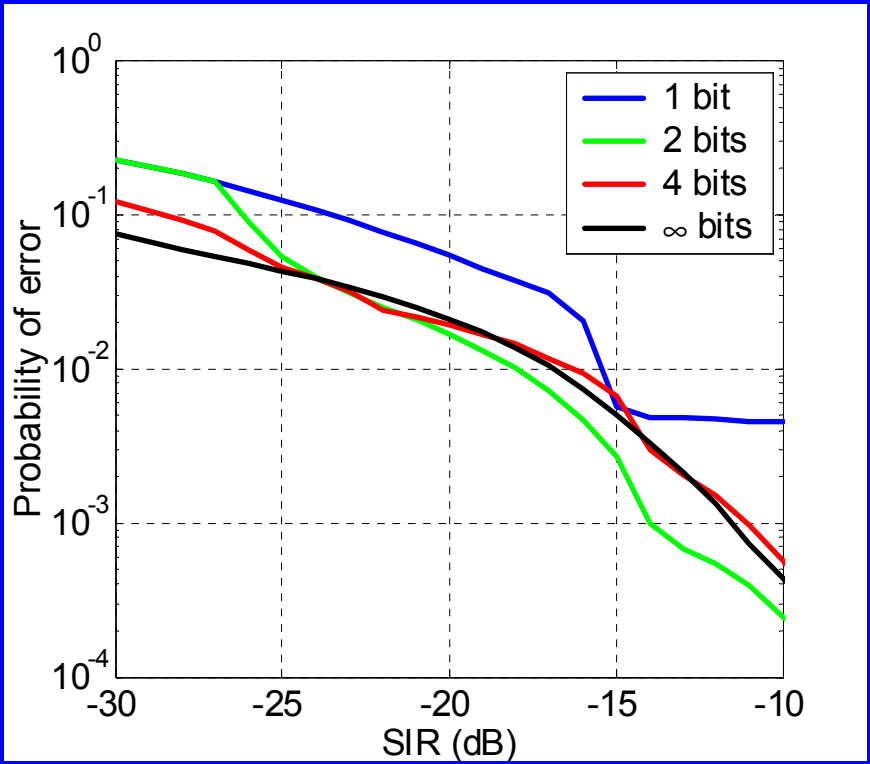
UWB Baseband Processor



BW = 300MHz, Duty cycle = 2%, 31 pulses per bit

Number of bits of the ADC



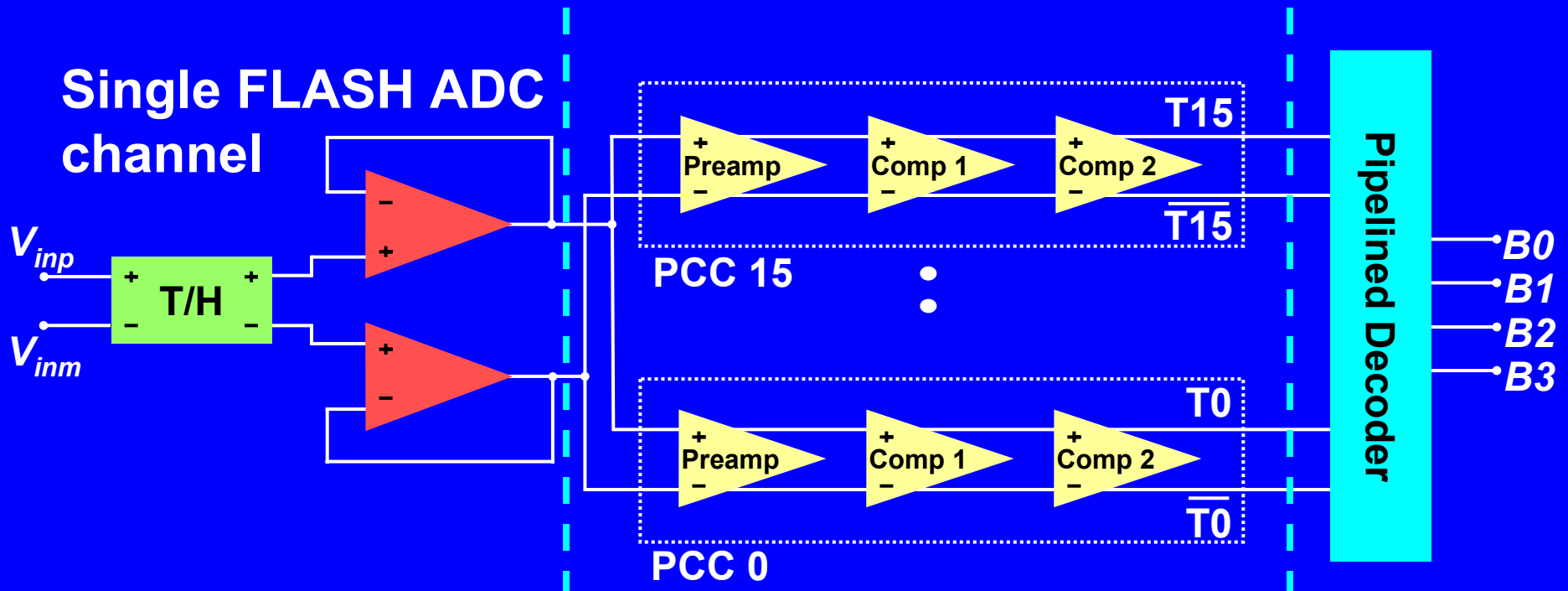


Noise Limited Case

Interference Limited Case

4 bits sufficient for reliable UWB detection

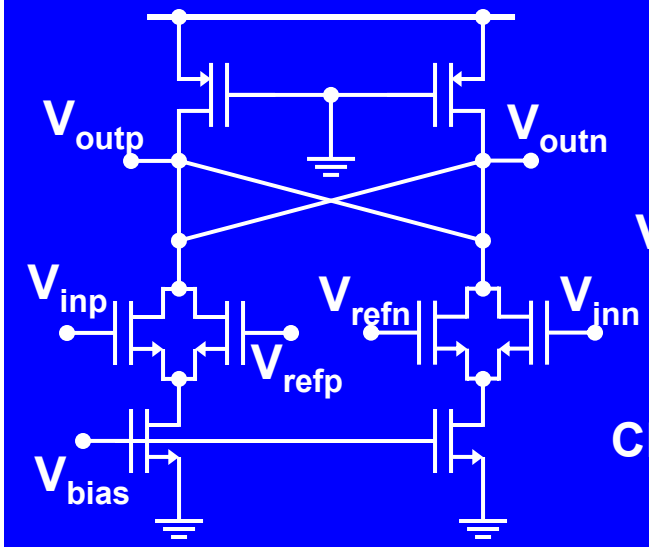
ADC Architecture



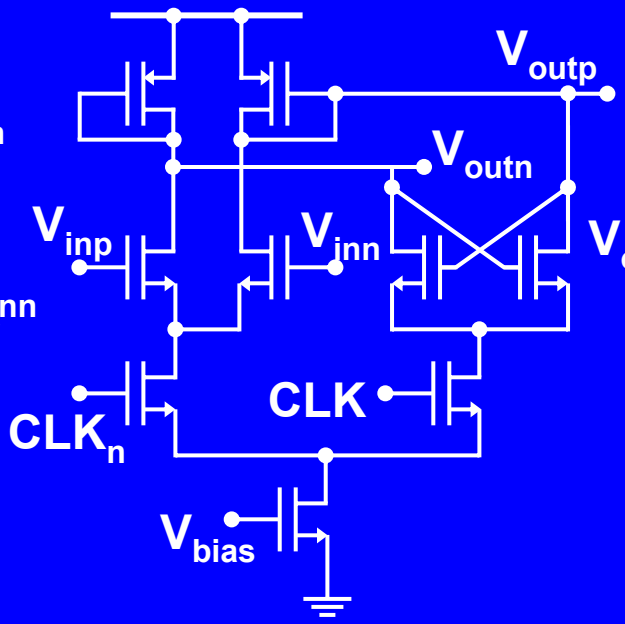
- Switch + Capacitor
- Better dynamic performance
- Low resolution

- Fully Differential Preamplifier and Comparators

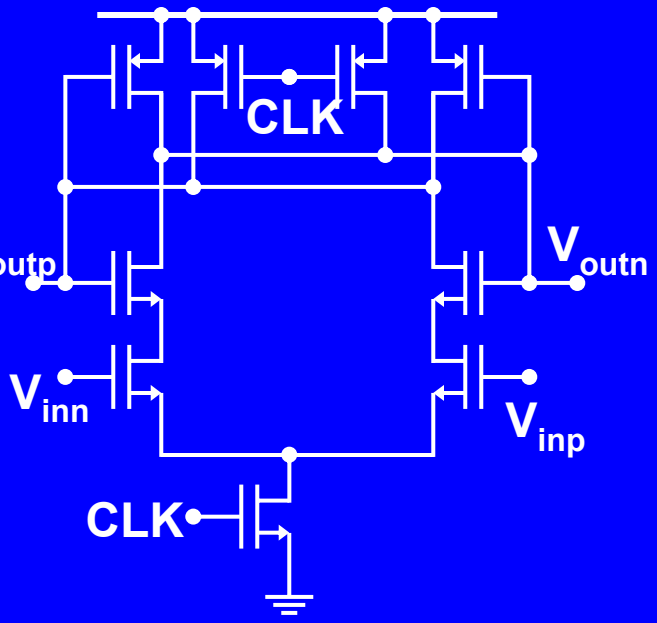
ADC (Circuits)



Preamplifier



Comparator 1

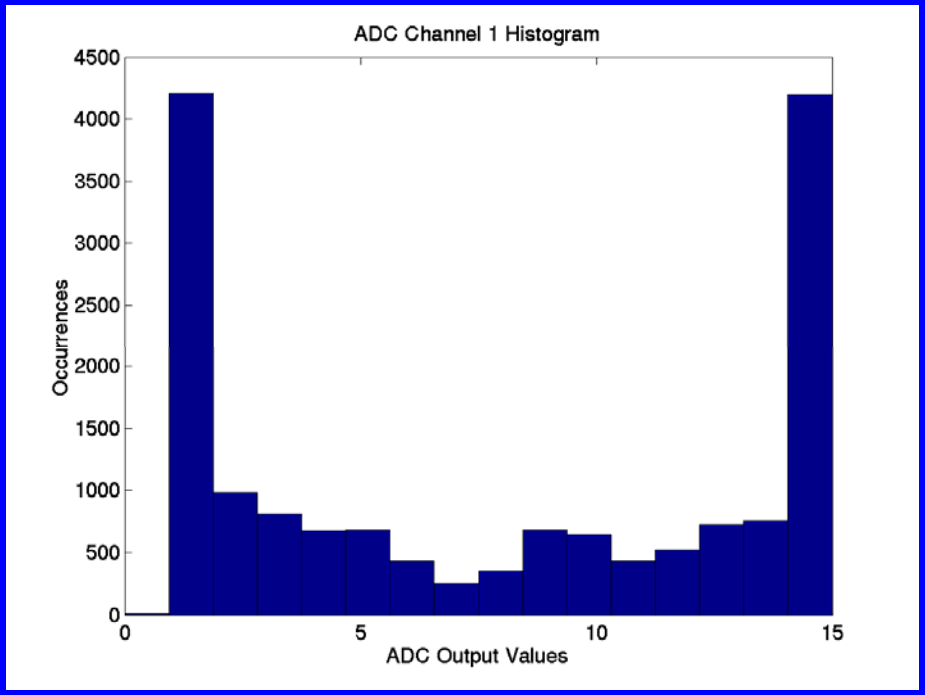


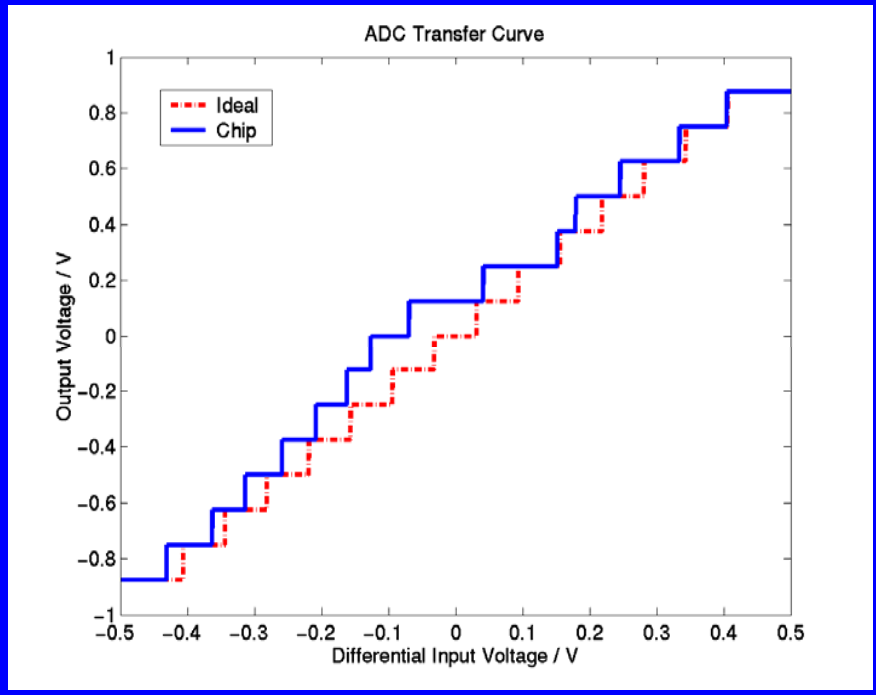
Comparator 2

Gain from positive feedback

2 comparators for metastability resolution

ADC (Measurements)

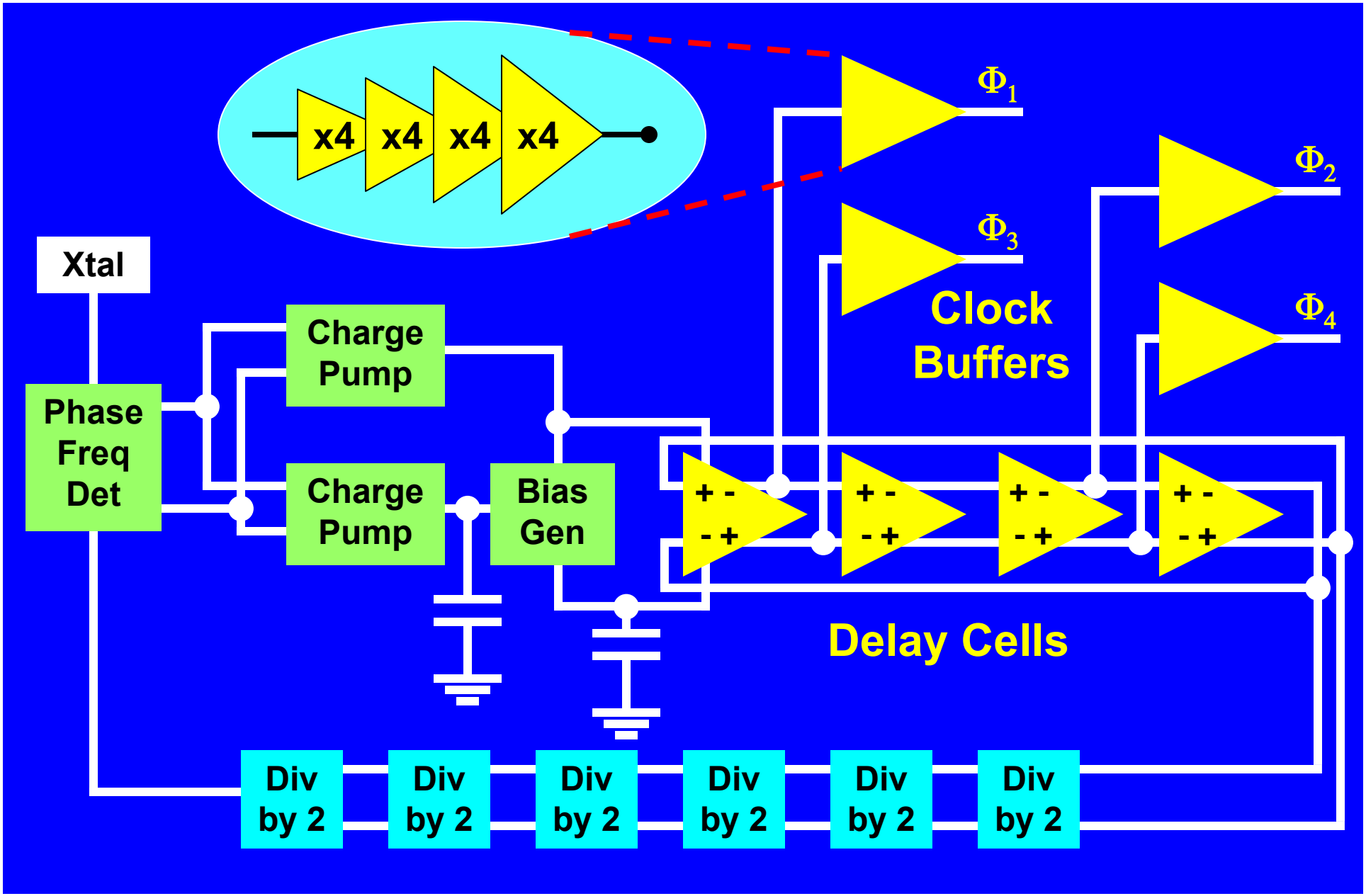




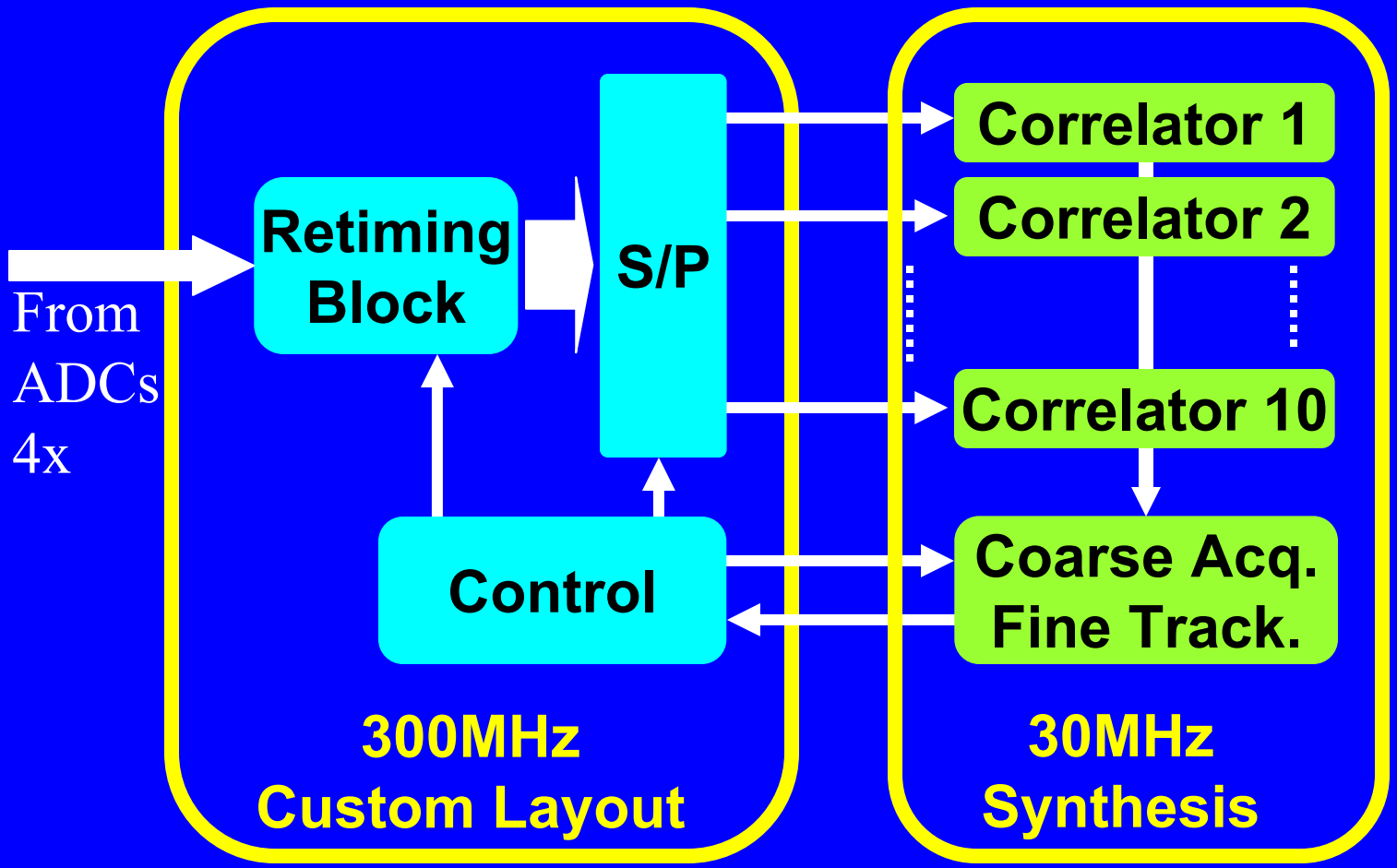
ADC Channel 1		
f_{CLK} / MHz	DNL_{ave} / LSB	INL_{ave} / LSB
250	0.31	0.62
384	0.31	0.62

Dornberg, J., Lee, H.S. and Hodges, D.A., "Full-Speed Testing of A/D Converters", IEEE JSSC, Dec 1984.

Clock Generation Subsystem



Digital Backend Specification



Whole synchronization in digital domain.
Coarse Acquisition < 70μs, Fine Tracking Precision = 1sample

Coarse Acquisition

- **Wider integration window?**

  2 samples per pulse

  N_c pulses per bit

Case 1: 1window ⇒ Width N

$2N_cN$ multiplications

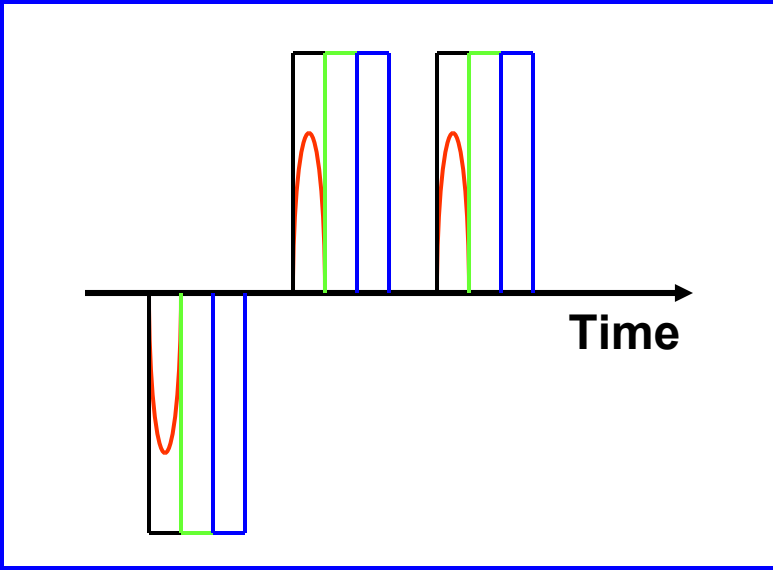
$2N_cN-1$ additions

Case 2: N windows ⇒ Width 1

$2N_cN$ multiplications

$2N_cN-N$ additions

PARALLELIZATION



Loss = 1.7dB

Time to Coarse Acq. 70 μs

50 correlations in parallel

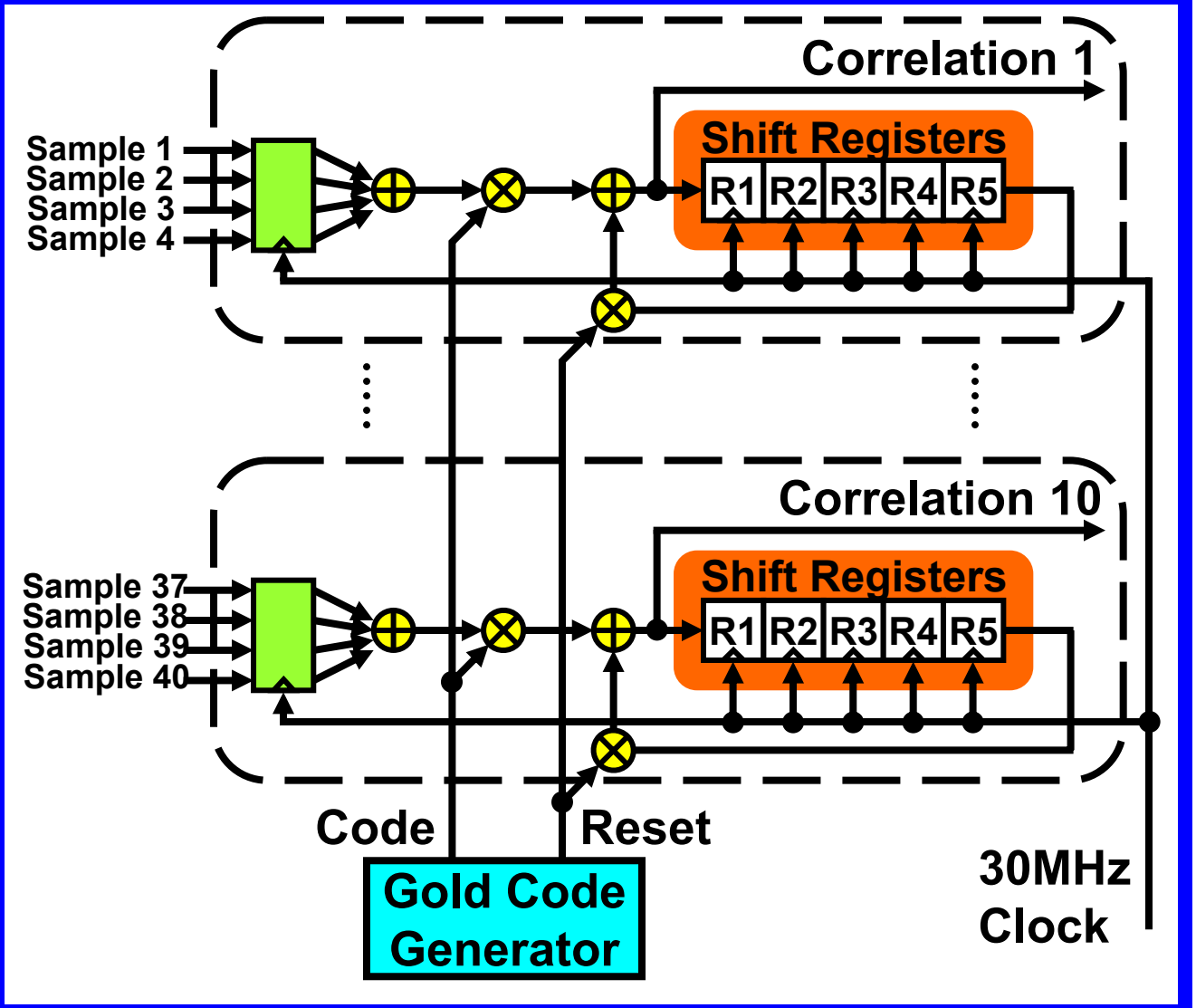
Correlators

1 Correlation:

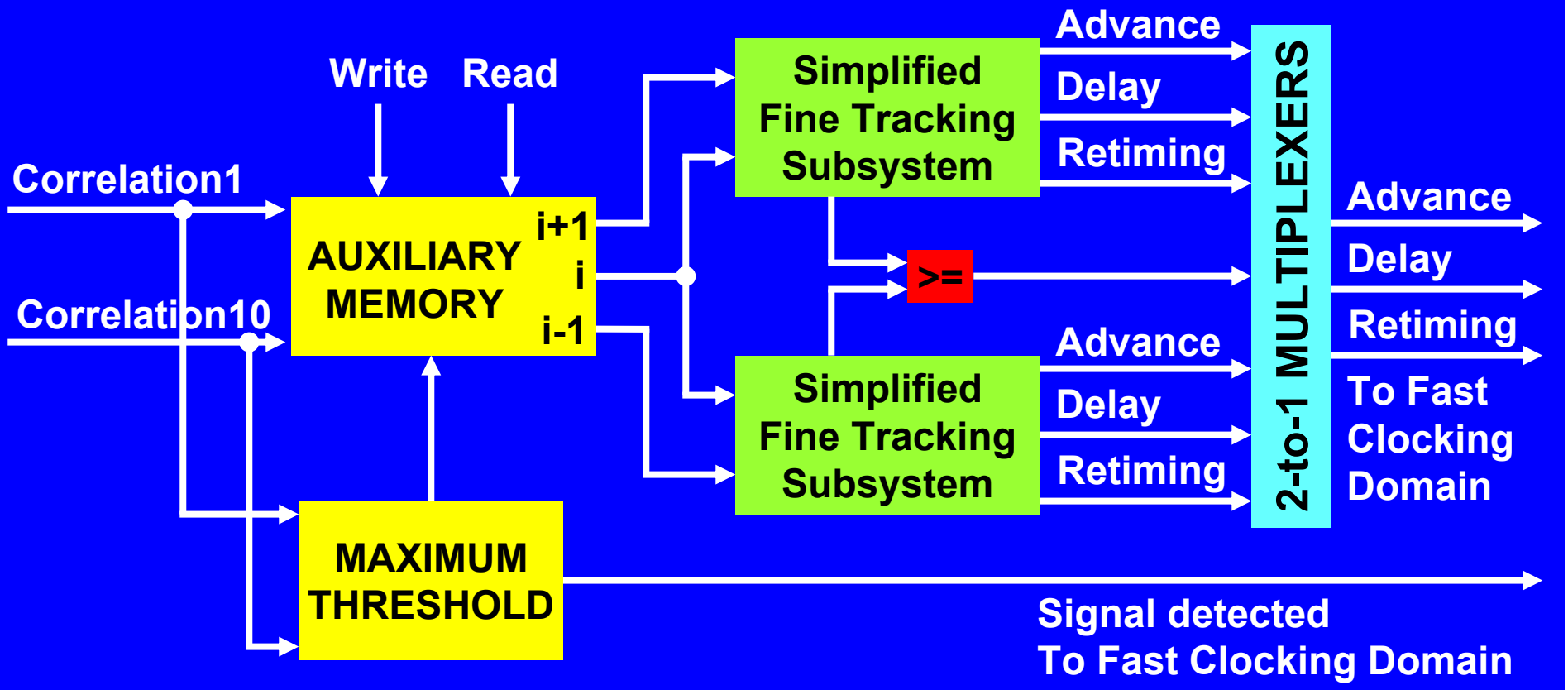
200 samp/frame
31 frames

= 6200
FIR coeffs

50 Correlations in parallel

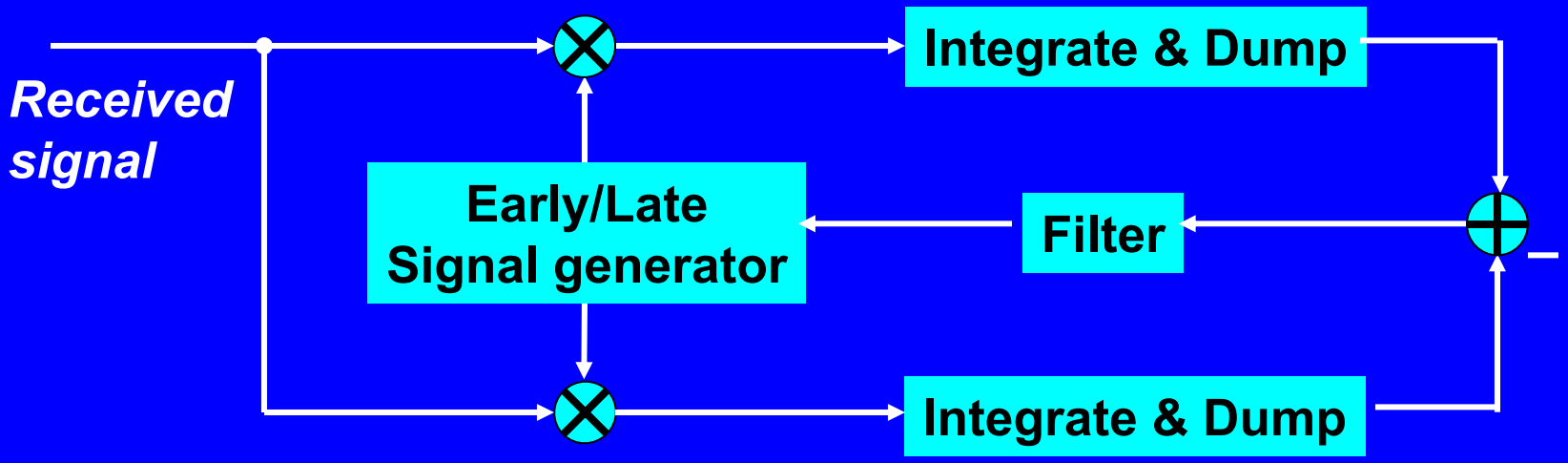


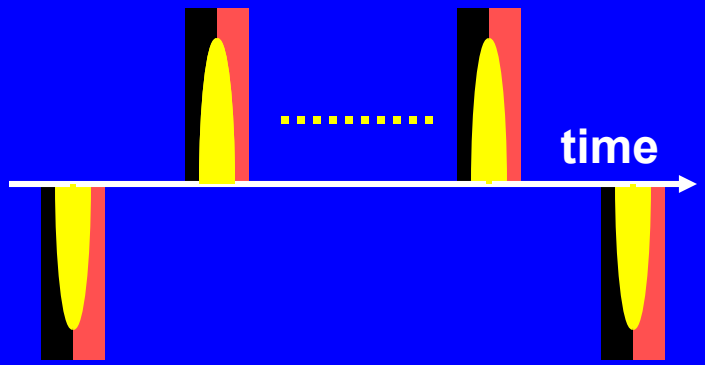
Coarse Acquisition



Signal Detection: 6 cycles
Delay Estimation: 7 cycles

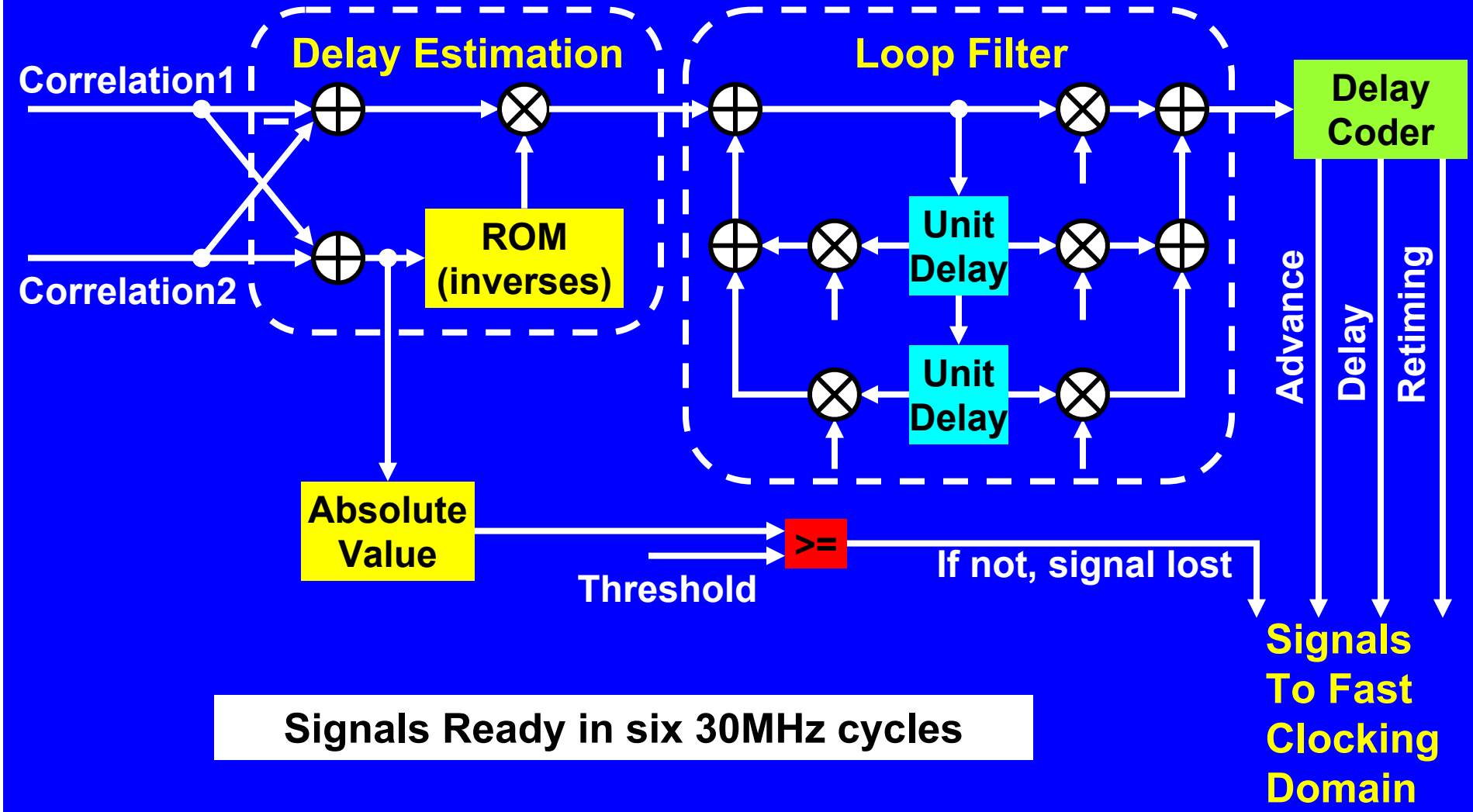
Fine Tracking Algorithm





- 20 ppm, width = 2ns ⇒ 25μs for static users.
- Granularity: An integer number of samples

Fine Tracking



Signals Ready in six 30MHz cycles

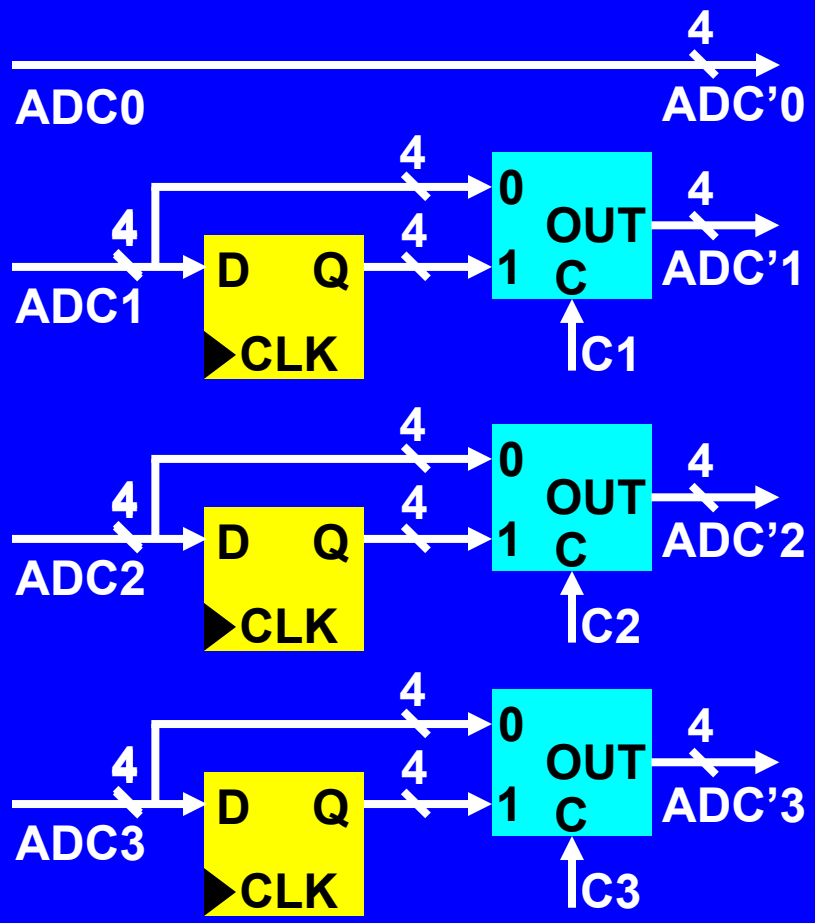
Retiming Block

- Data received
  4 samples at a time.

ADC0[n]	ADC1[n]	ADC2[n]	ADC3[n]

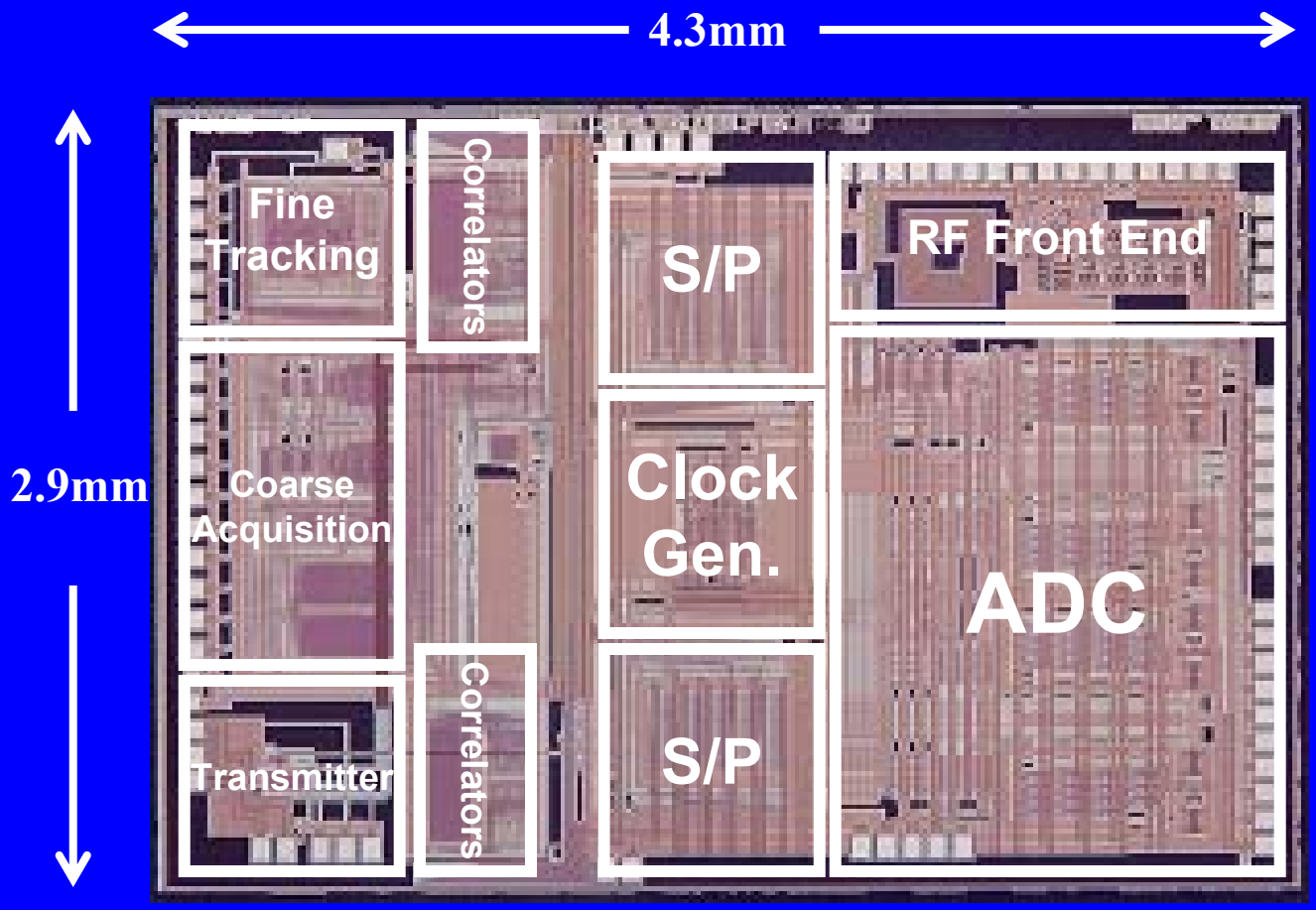
- Timing precision required :
  1 sample

ADC1[n-1]	ADC2[n-1]	ADC3[n-1]	ADC0[n]
ADC2[n-1]	ADC3[n-1]	ADC0[n]	ADC1[n]
ADC3[n-1]	ADC0[n]	ADC1[n]	ADC2[n]



$$m[i] = 4n[i]+\Delta[i] \Rightarrow \Delta[i+1] = \mathrm{mod}(\Delta[i]+d[i],4)$$

UWB System on a Chip



1.8 V - 0.18µm non-epi

Summary

Chip Specifications		
Process Tech.	0.18μm non-epi	
Bit Rate	193kbps	
ADC Performance	Abs. Accuracy	Rel. Accuracy
Static Perform.	3.1bits	3.9bits
Dynamic Perform.	3.0bits	3.4bits
Power Consumption		
ADC + PLL	135mW	
CLK Buffers	65mW	
Backend	75mW	
Total	275mW	

Conclusions

- Implementation issues :
  - ADC with 2 comparators for metastability resolution
  - Ring oscillator enough for jitter specification
  - Extensive parallelization required
  - Synchronization in digital domain
- 193kbps wireless link demonstrated