Device Sizing for Minimum Energy Operation in Subthreshold Circuits

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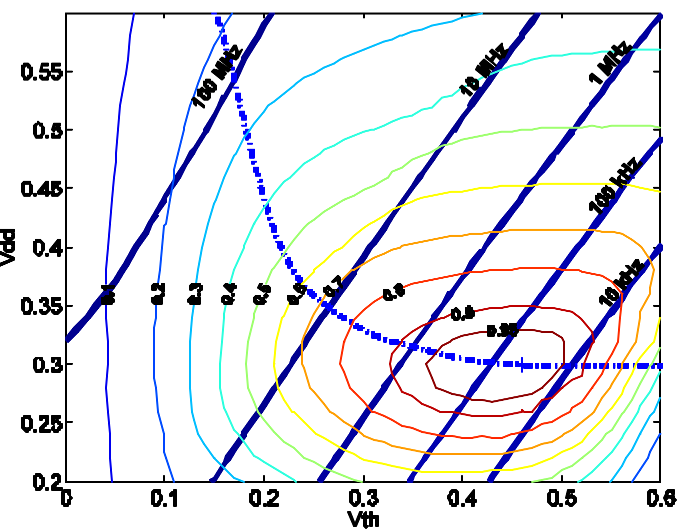
Outline

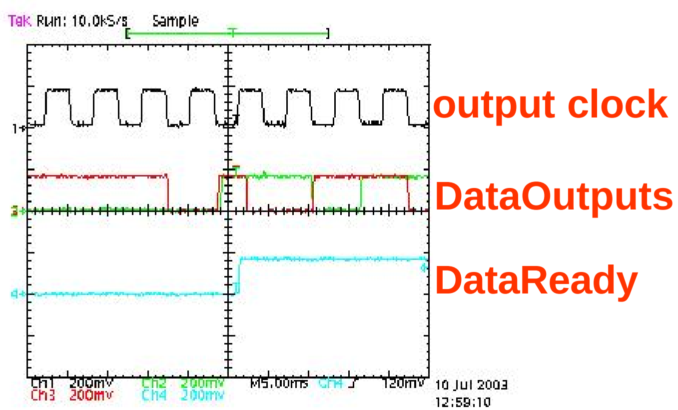
- Subthreshold operation
- Energy Consumption in subthreshold
- Optimum low-energy sizing
- Sizing to minimize operating voltage (V_{DD})
- Test chip measurements

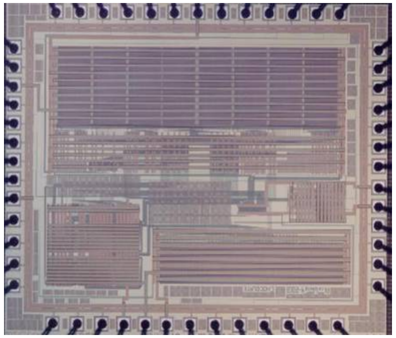
Previous Work

- Analog circuits
  - e.g. - E. Vittoz & J. Fellrath, *JSSC*'77
- Digital circuits
  - e.g. – H. Soeleman & K. Roy, *ISLPED*'99
  - J. Kao, M. Miyazaki, & A. Chandrakasan, *ISSCC*'02
  - J. Burr & J. Shott, *ISSCC*'94 (low voltage, but not subthreshold)
- Theoretical Minimum Energy
  - e.g. – R. Swanson & J. Meindl, *JSSC*'72
- Minimum Energy Point Demonstrated
  - Theoretical – e.g. - A. Wang, S. Kosonocky, & A. Chandrakasan, *ISVLSI*'03
  - 180mV FFT processor - A. Wang and A. Chandrakasan, *ISSCC*'04
  - Model; applied to off-the-shelf processors – Zhai, Blaauw, Sylvester, & Flautner, *DAC*'04



A. Wang, S, Kosonocky, and A. Chandrakasan, ISVLSI, 2003



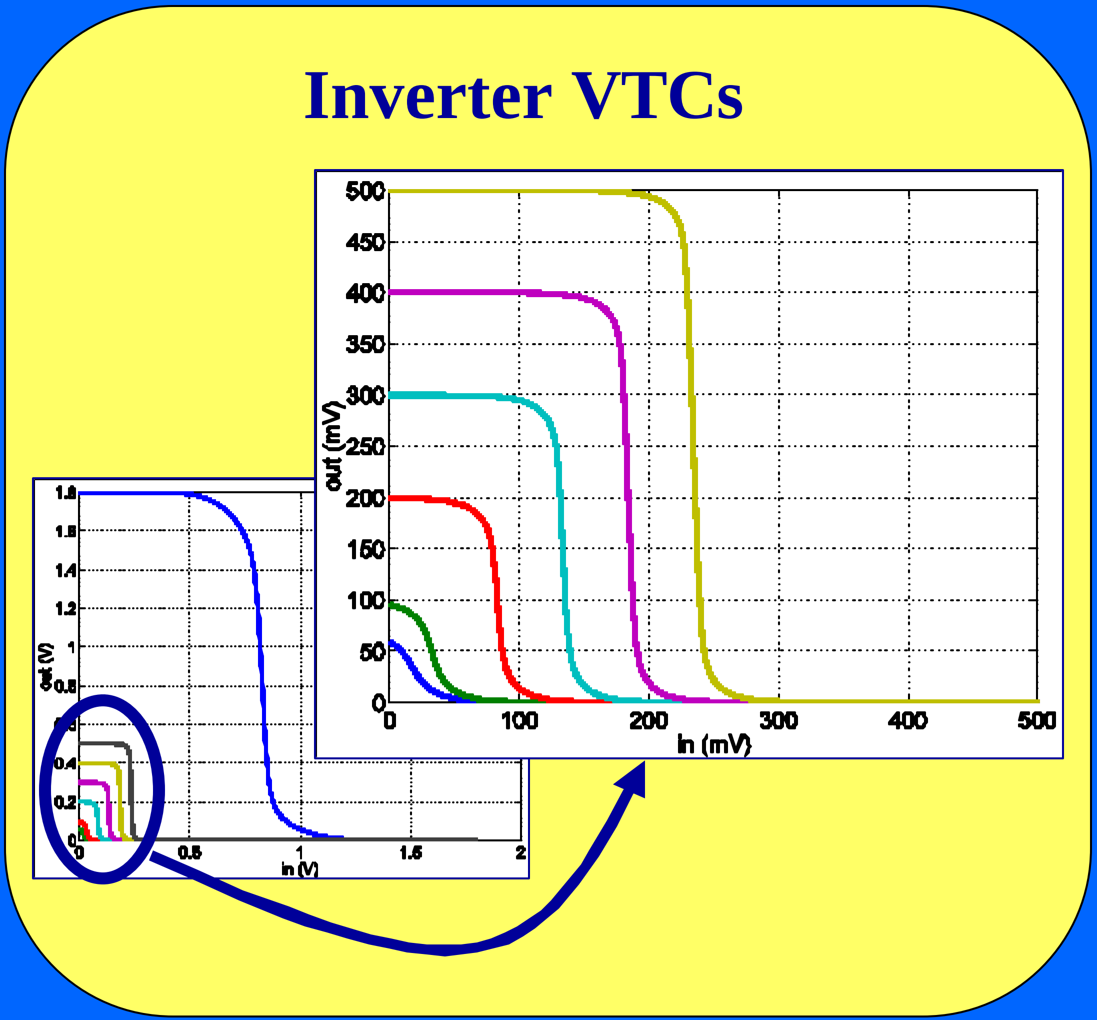


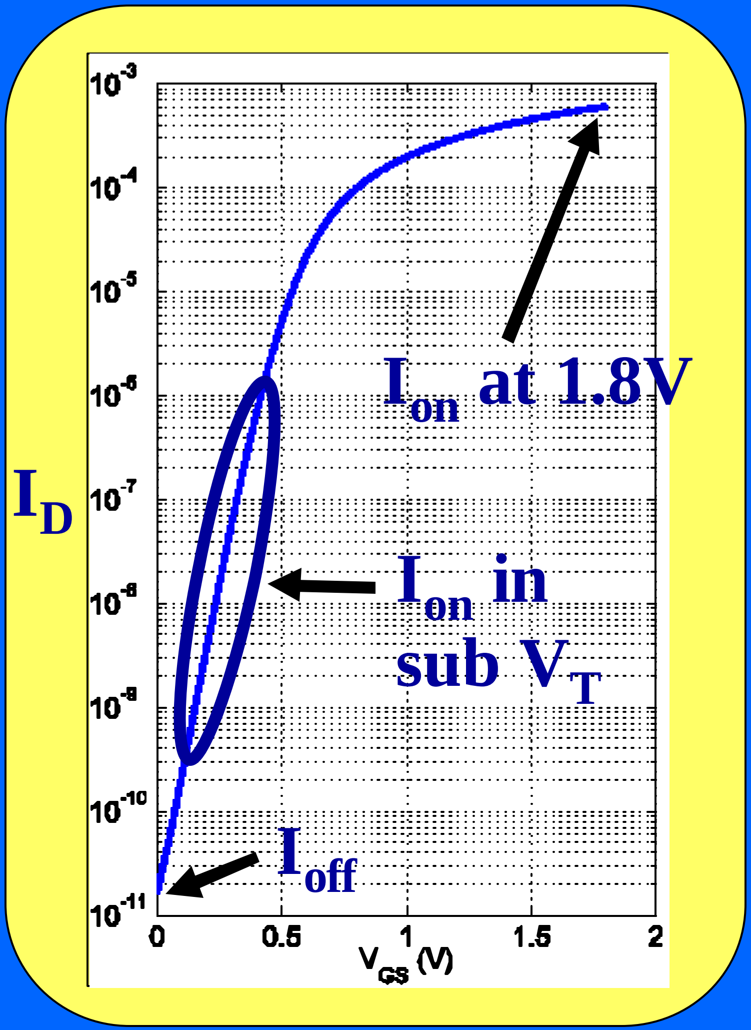
180mV FFT Processor

A. Wang and A. Chandrakasan, ISSCC. 2004

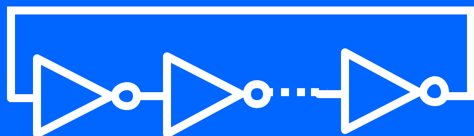
Subthreshold Operation Basics

- Subthreshold logic operates with $V_{DD} < V_T$
- Both on and off current are subthreshold “leakage”

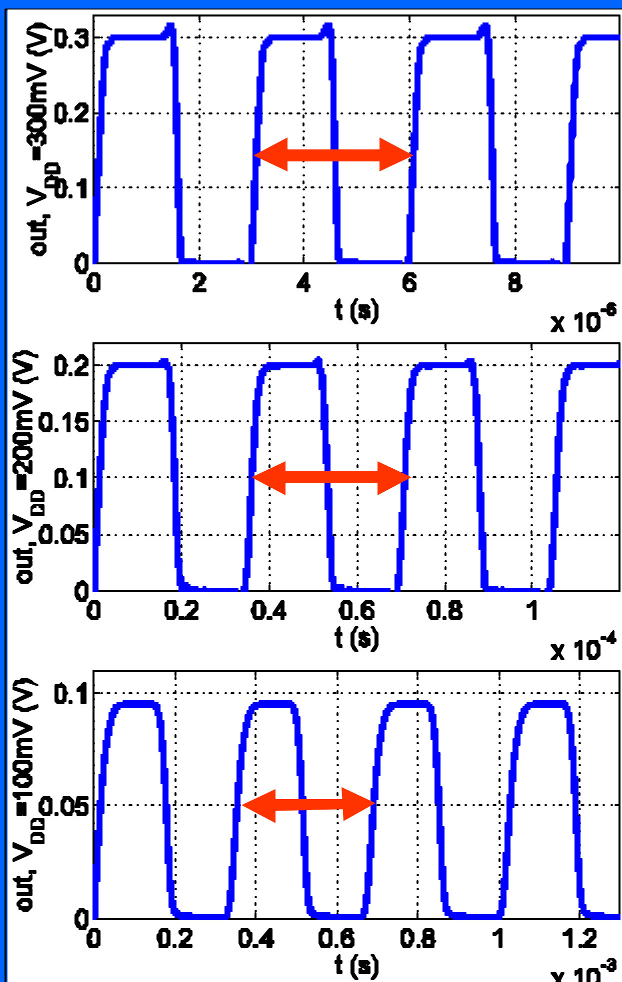




Subthreshold Operation Basics



11 stages



330kHz
300mV

29kHz
200mV

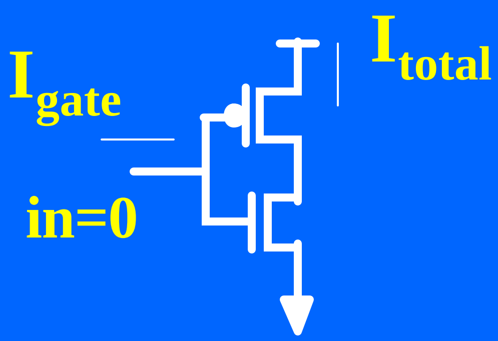
3kHz
100mV

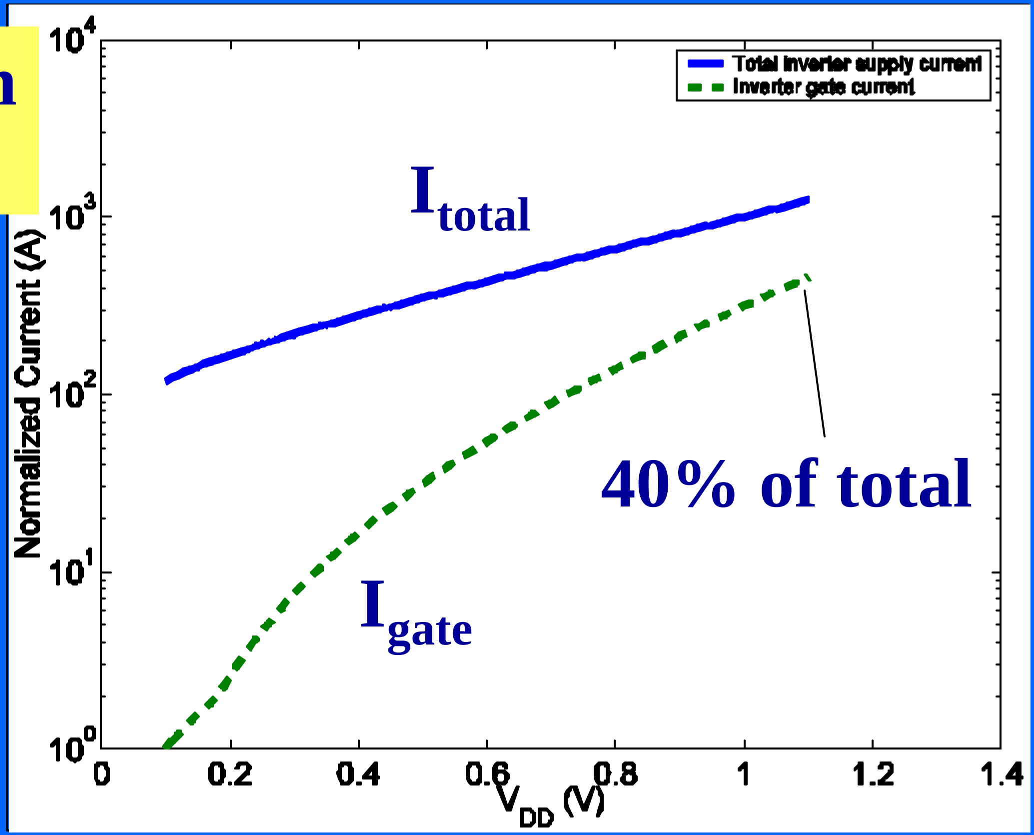
- Simple ring oscillator shows functionality in deep sub V_T
- Delay increases exponentially in sub V_T
- Static CMOS is robust for sub V_T operation

Sources of Leakage and V_{DD} Scaling

- Components of Transistor Off-Current
  - Subthreshold current – the focus of this presentation
  - Gate leakage – rolls of with V_{DD} faster than sub V_T current
  - GIDL – a problem at low V_{GS}, high V_{DS} (Keshavarzi, et al., ITC'97)
  - Junction leakage – negligible at low V_{DD} for 0.18um

Gate leakage contribution to Ioff for 90nm





Problem

- Subthreshold operation offers energy savings
- Some changes are required to minimize operating voltage

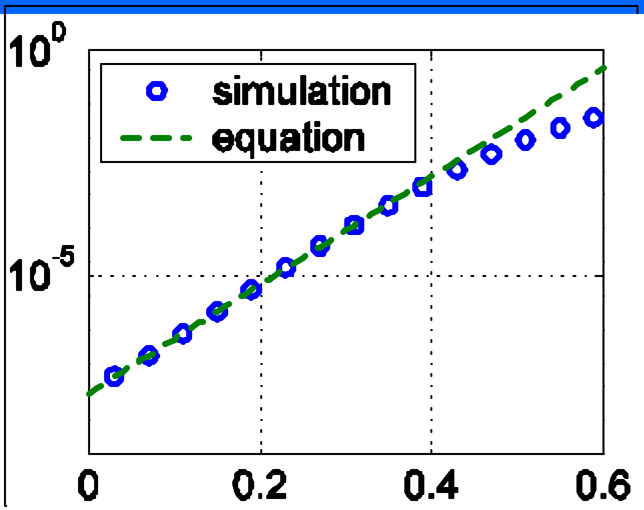
- Is minimum voltage operation the same as minimum energy operation?

Modeling Subthreshold Current

Subthreshold current:

$$I_{SUB} = I_o e^{\frac{V_{GS} - V_T + \eta V_{DS}}{n V_{th}}} \left(1 - e^{-\frac{V_{DS}}{V_{th}}}\right)$$

Optional DIBL and low-V_{DS} roll-off modeling



Generic Equation for Energy per Operation

$$E_{TOTAL} = E_{ACTIVE} + E_{LEAKAGE}$$

$$E_{TOTAL} = C \cdot V_{DD}^2 + I_{OFF} V_{DD} T_D$$

Switched capacitance

Off-current

Delay per operation

Modeling Characteristic Inverter

Equation for Inverter Delay

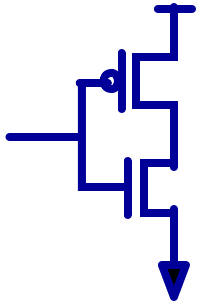
Parameters for the gate account for both NMOS and PMOS

Fitting Parameter

Inverter Switched Cap

On Current

$$t_d = \frac{KC_g V_{DD}}{I_{on}} = \frac{KC_g V_{DD}}{I_{o,g} e^{\frac{V_{GS} - V_{T.g}}{nV_{th}}}}$$



Normalize total using Ceff

Normalize total Ioff to characteristic inverter using Weff:

$$I_{OFF} = W_{eff} I_{o,g} e^{\frac{-V_{T.g}}{nV_{th}}}$$

Normalize total delay to characteristic inverter using Logic Depth (L_{DP}):

$$T_D = t_d \cdot L_{DP}$$

$$E_{TOTAL} = C \cdot V_{DD}^2 + I_{OFF} V_{DD} T_D$$

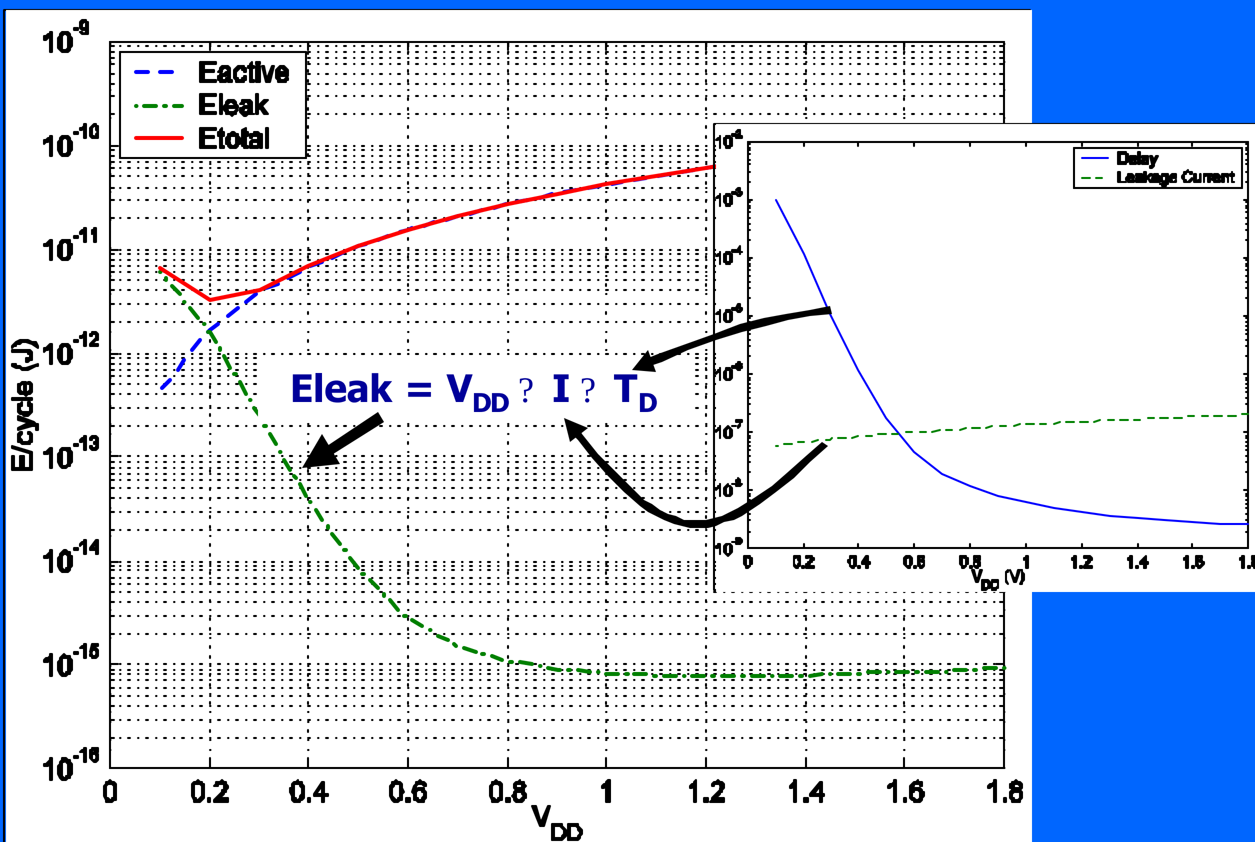
Sizing for Subthreshold Digital Circuits

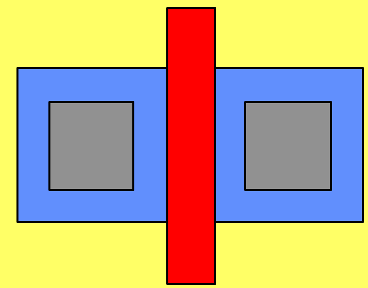
Active Energy / **Leakage Energy**

$$E_{Total} = C_{eff} V_{DD}^2 + W_{eff} L_{DP} K C_g V_{DD}^2 e^{-\frac{V_{DD}}{nV_{th}}}$$

Sizing Affects Minimum Operating Voltage

Sizing Affects Switched Cap and Leakage

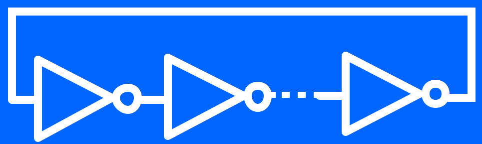




Smaller size lowers C_{eff}, W_{eff}, C_g

How do you Minimize energy?

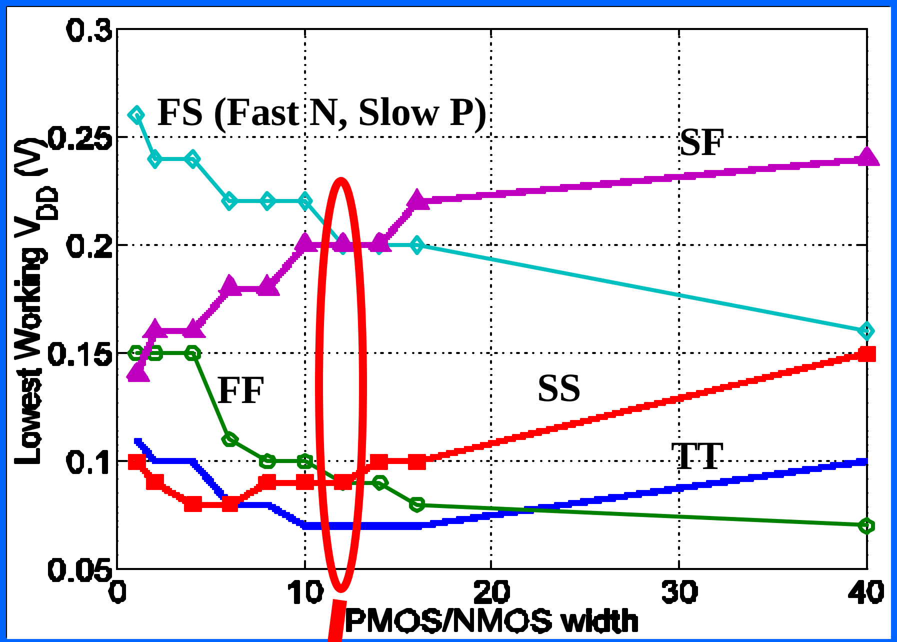
Sizing for Minimum Operating V_{DD}

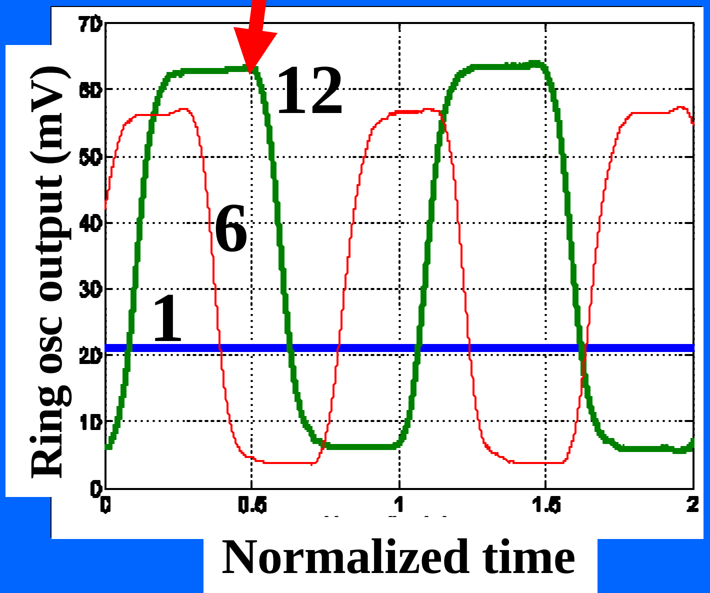


Check the minimum V_{DD} for a ring oscillator

- Require 10% to 90% swing of output
- Look at all process corners

Minimum Operating V_{DD}

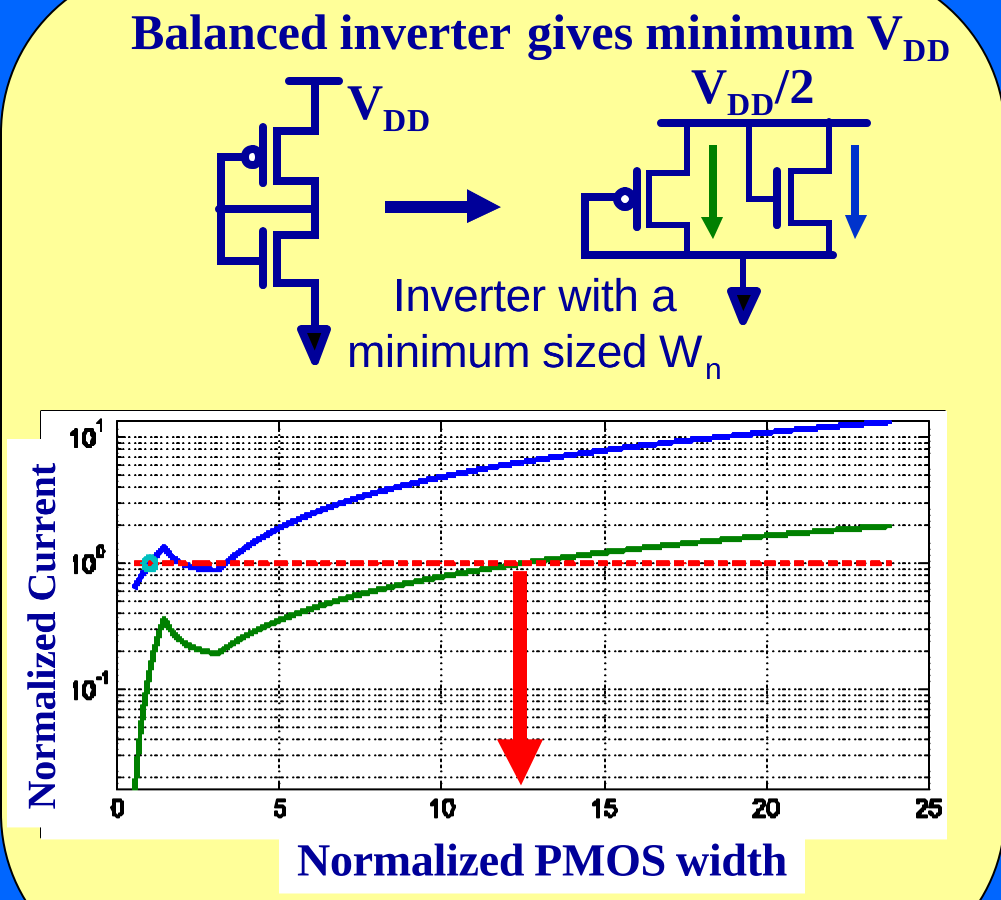




Sizing for Minimum Operating V_{DD}

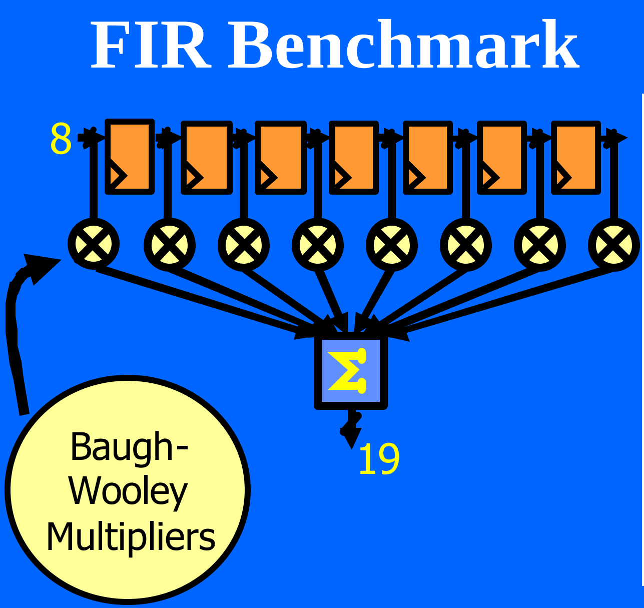
Balanced PMOS and NMOS currents is the key to minimum voltage operation

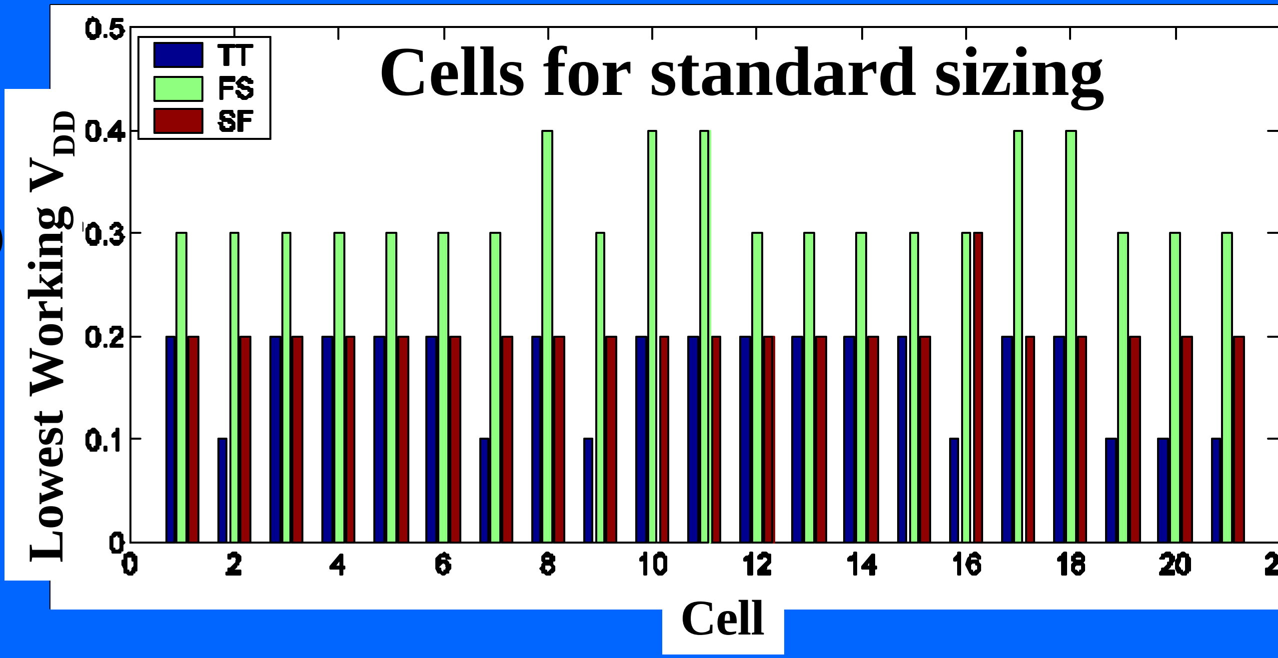
- **Most processes are not balanced in subVT**



P/N of 12 minimizes V_{DD}
For 0.18mm process

Standard Cells and Minimum Energy



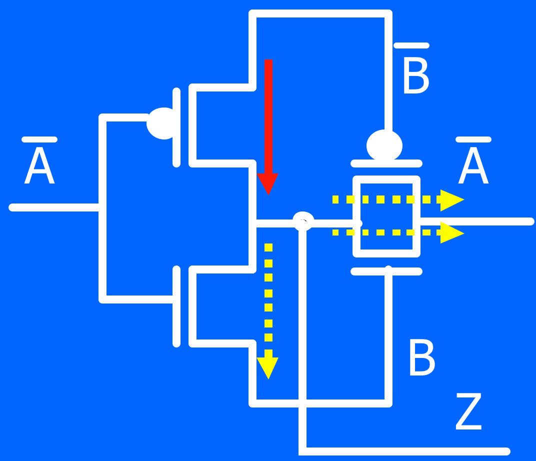


- In standard synthesis, some cells fail at higher V_{DD} at process corners
- "Fixing" them by changing the sizes or not using the cell increases switched capacitance, but allows lower VDD operation

Example Problematic Cell

Parallel leakage

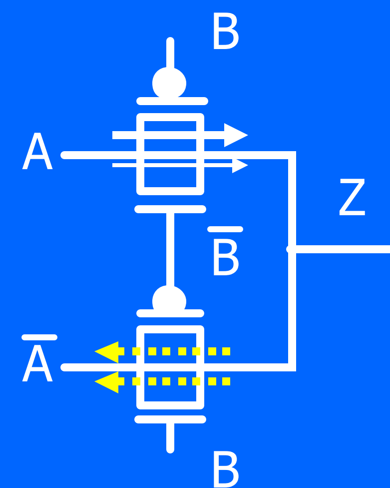
standard cell library
tiny XOR

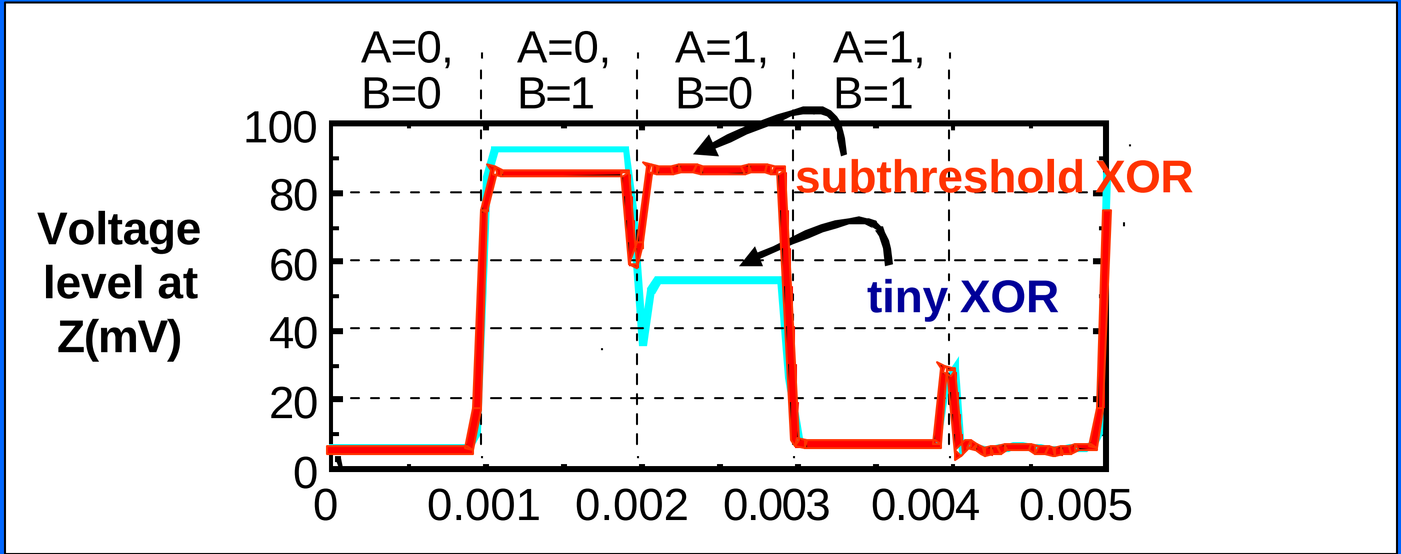


A	B	A xor B
0	0	0
0	1	1
1	0	1
1	1	0

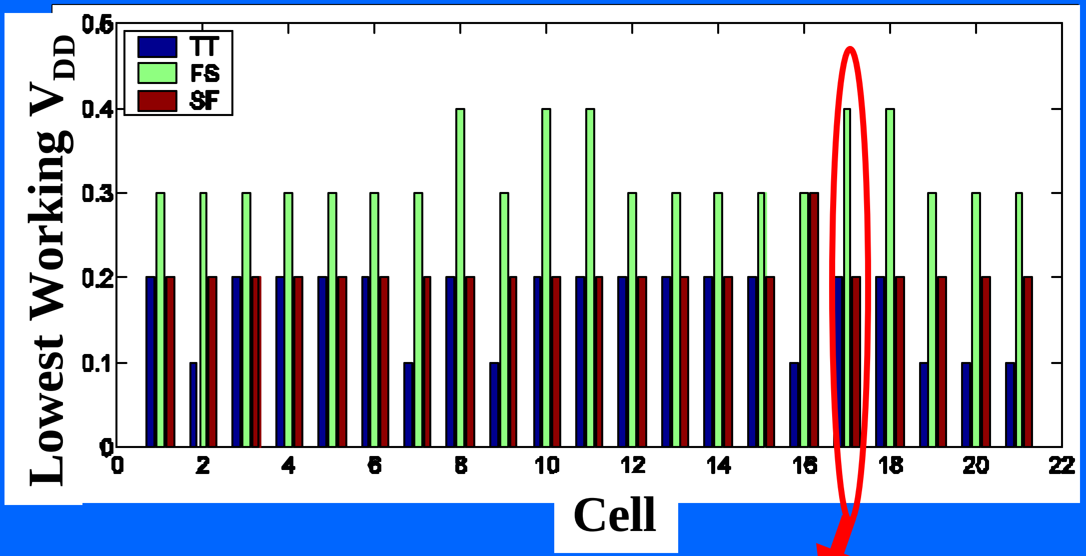
leakage current
drive current

subthreshold XOR

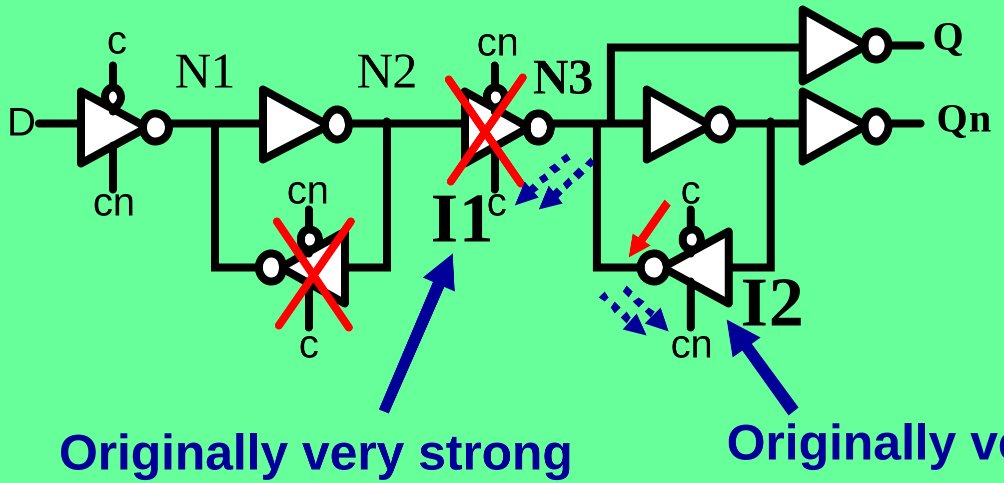




Example Problematic Cell



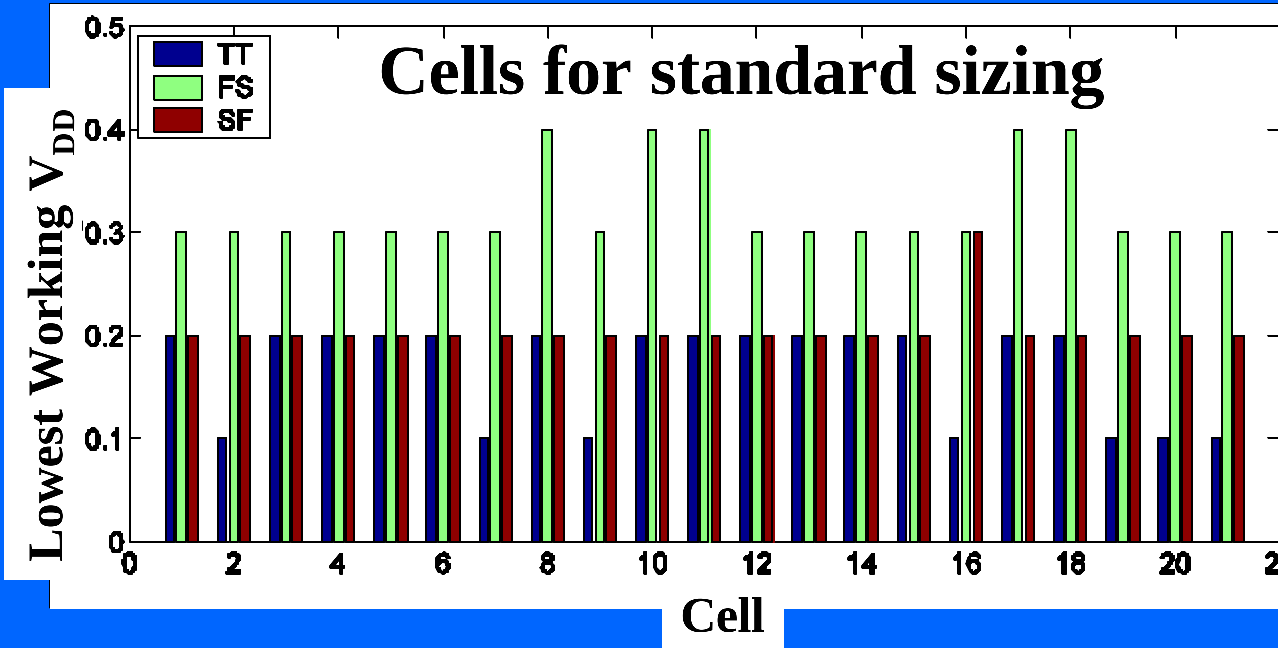
"Fixing" the standard Cell flip-flop with Sizing

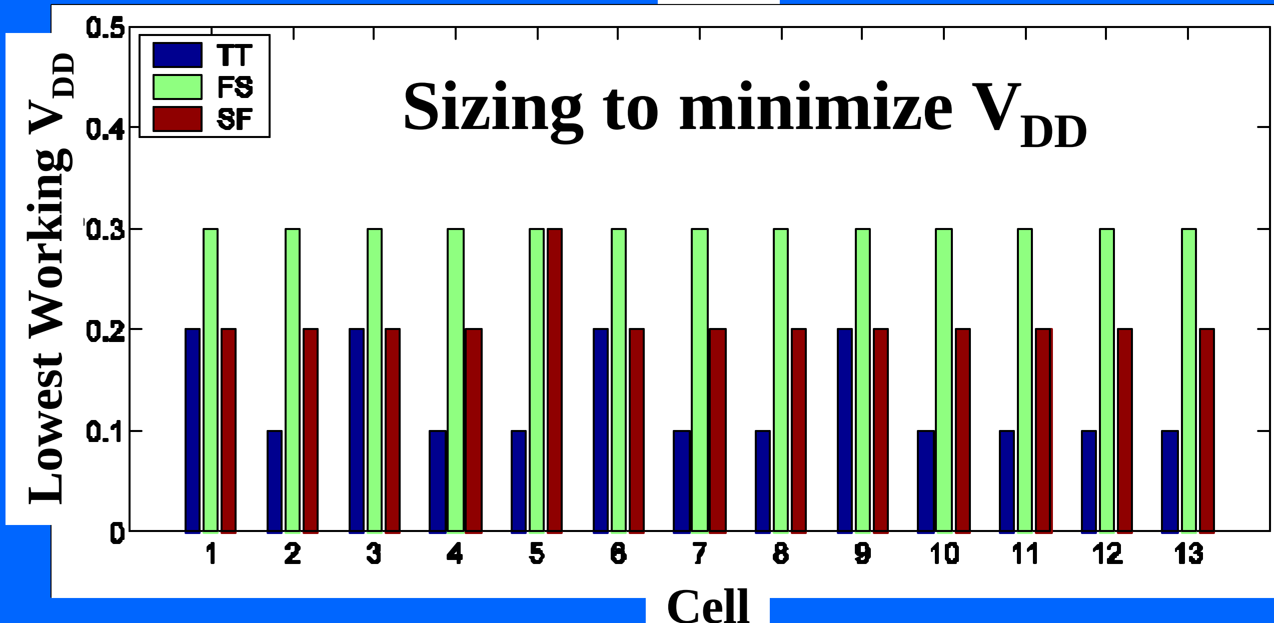


- FS Corner (strong NMOS, weak PMOS) – N3 cannot hold a 1 when c=0
- Fix by reducing I1 size and increasing I2 size

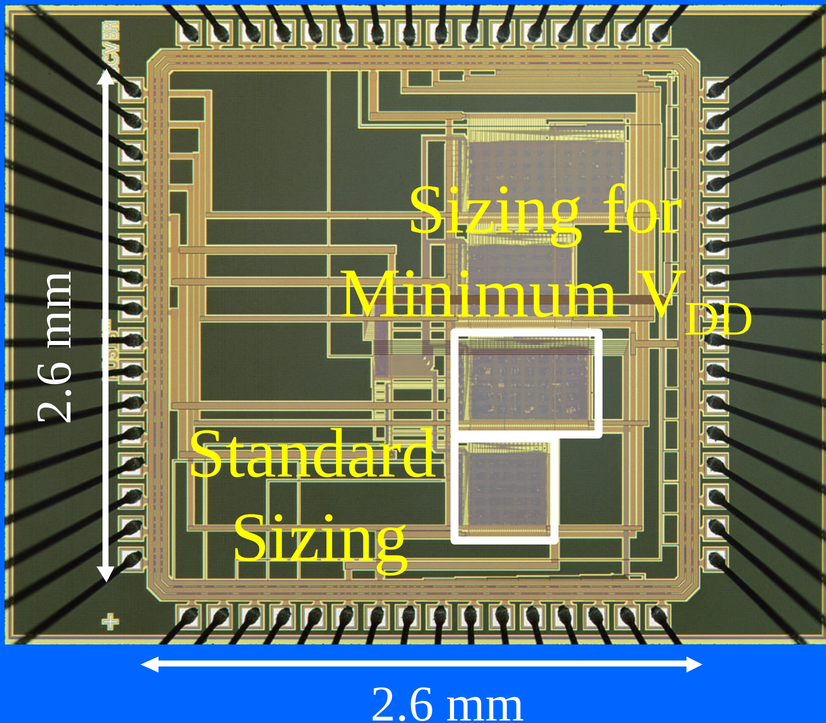
Standard Cells and Minimum Energy

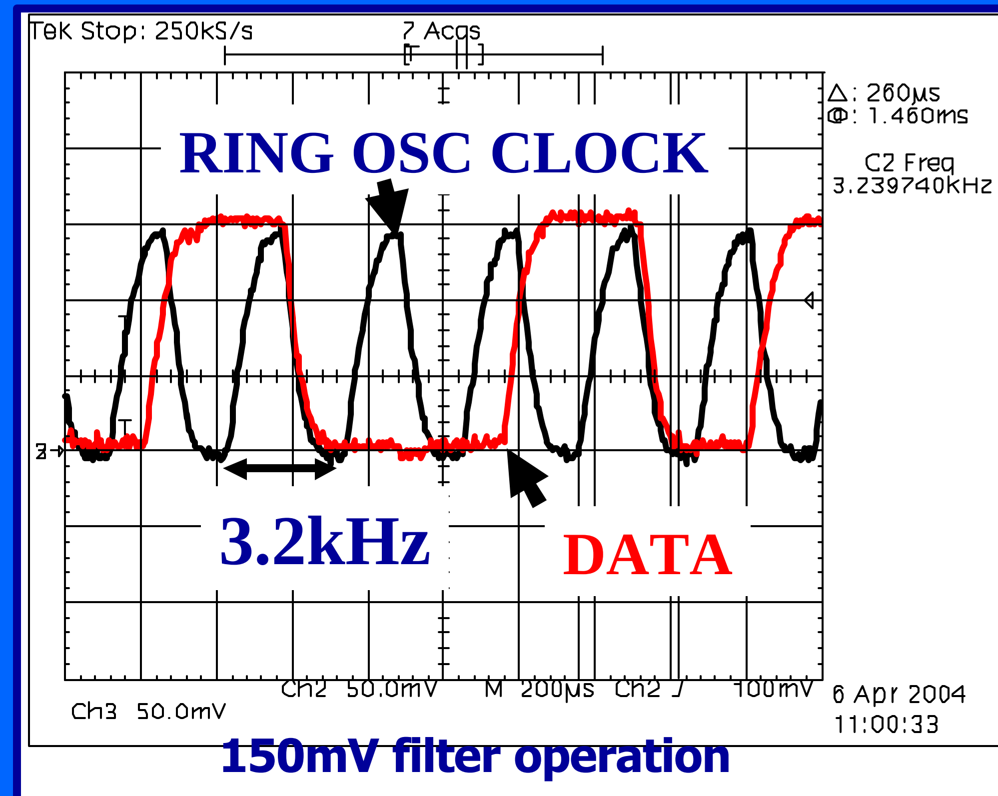
- Sizing for minimum V_{DD}
  - Prevent inclusion of cells having large stacks that cause early failure (e.g. AOI)
  - Resize some cells
- Fabricate test chip to evaluate overhead

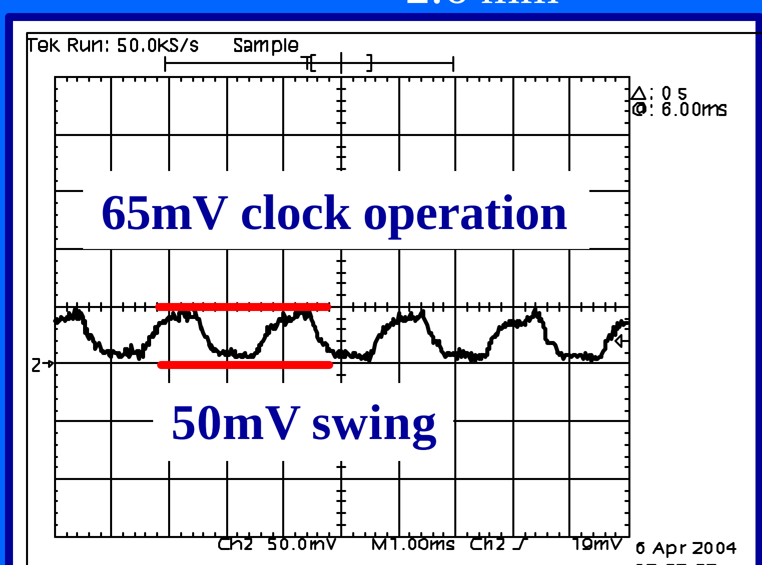




Subthreshold Sizing Test Chip

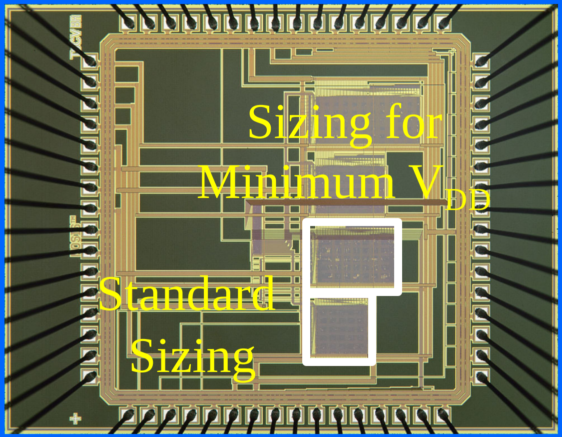


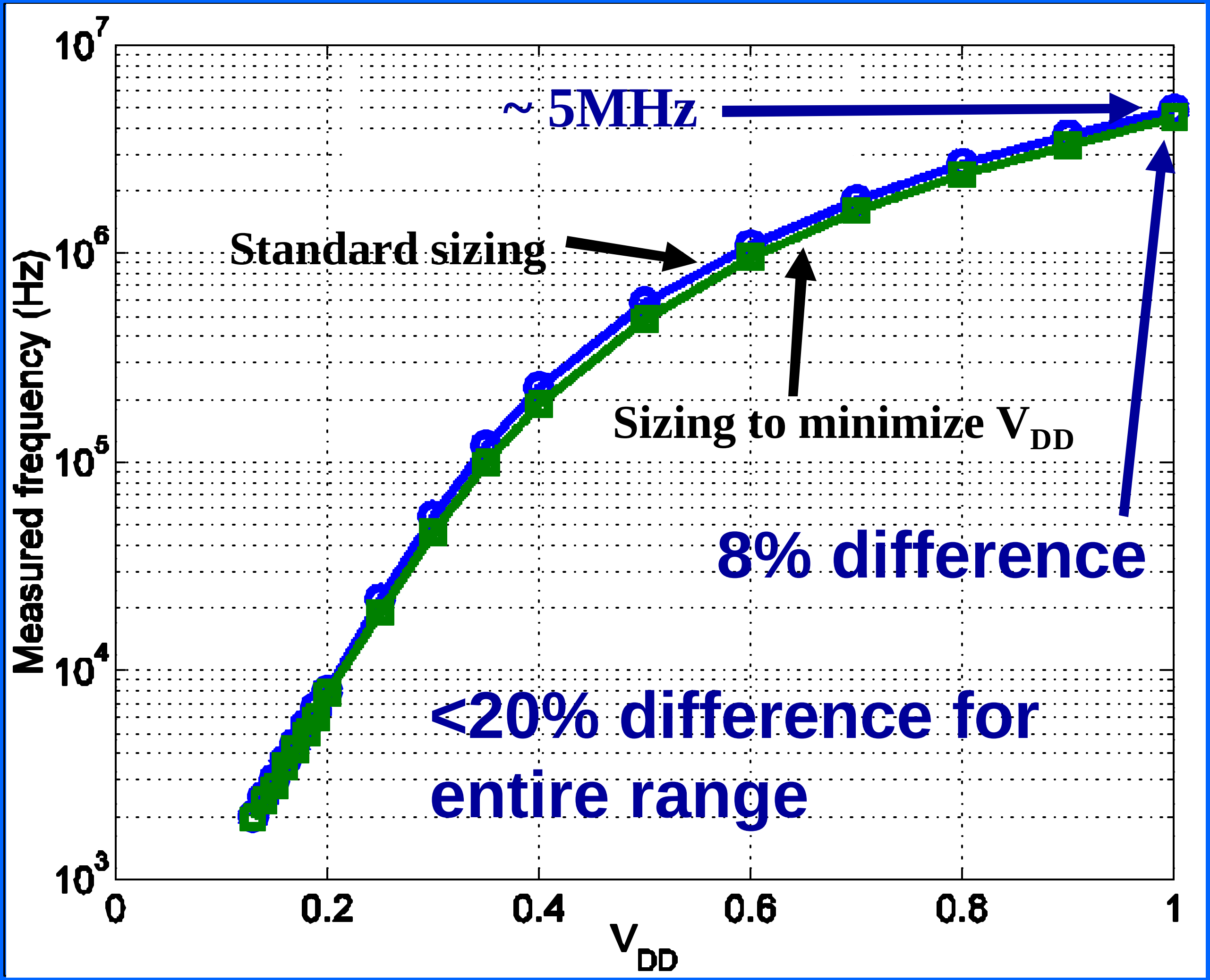




- 0.18μm, 6M test chip
- Filters use external or internal (LFSR) data
- External or internal (ring osc) clocks
- Both filters operate to below 200mV - typical corner

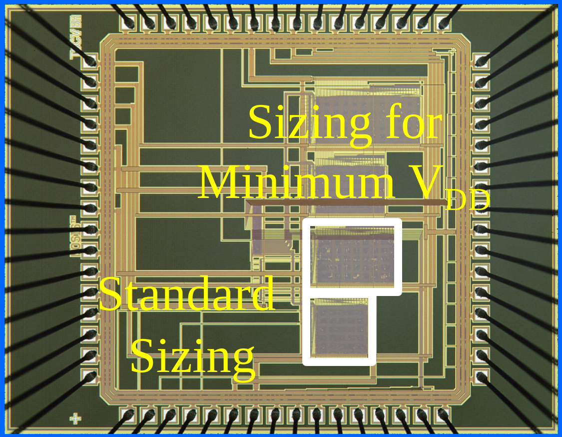
Sub-threshold Sizing Test Chip

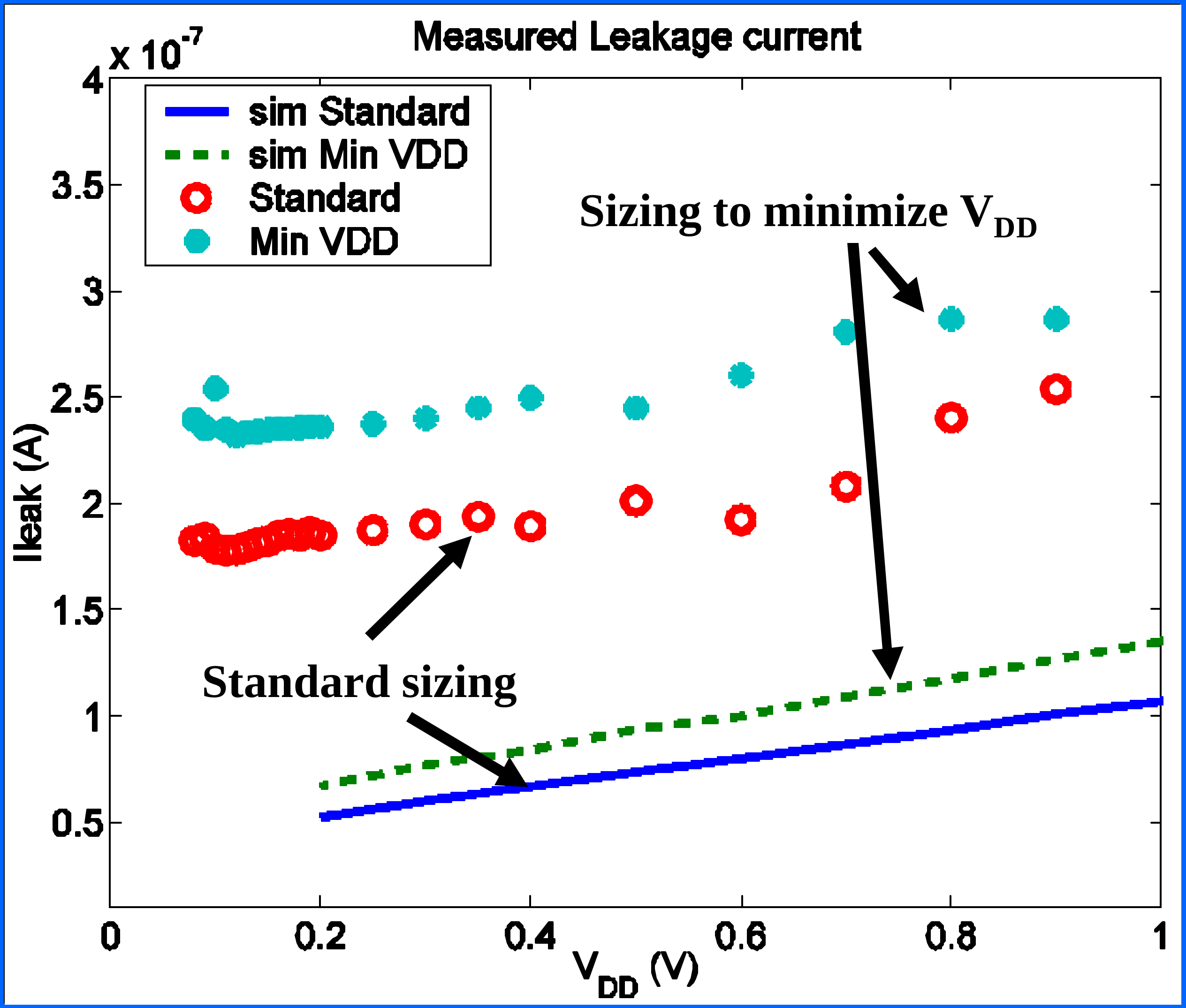




- Measured frequency versus V_{DD} of the ring oscillators

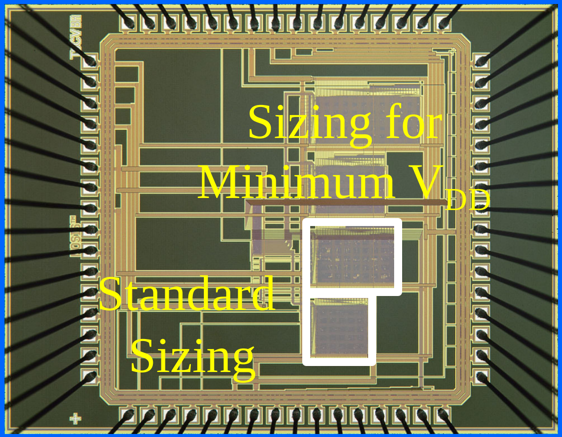
Sub-threshold Sizing Test Chip

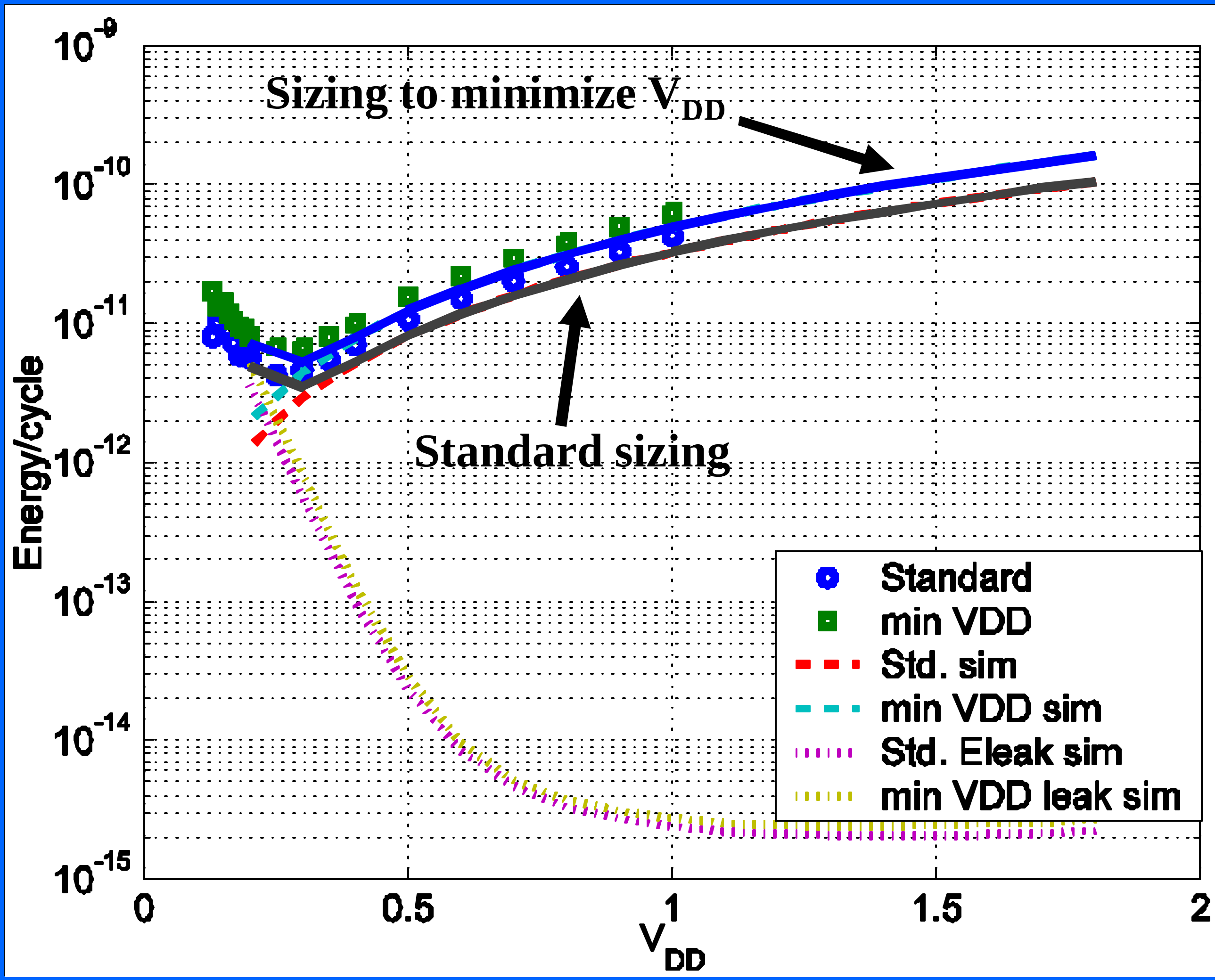




- Measured leakage current versus simulation across V_{DD}

Sub-threshold Sizing Test Chip

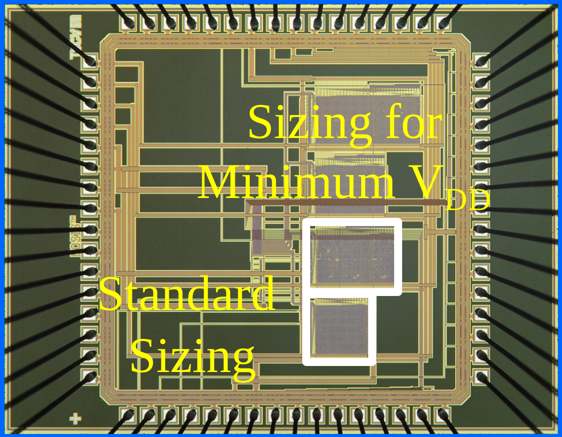


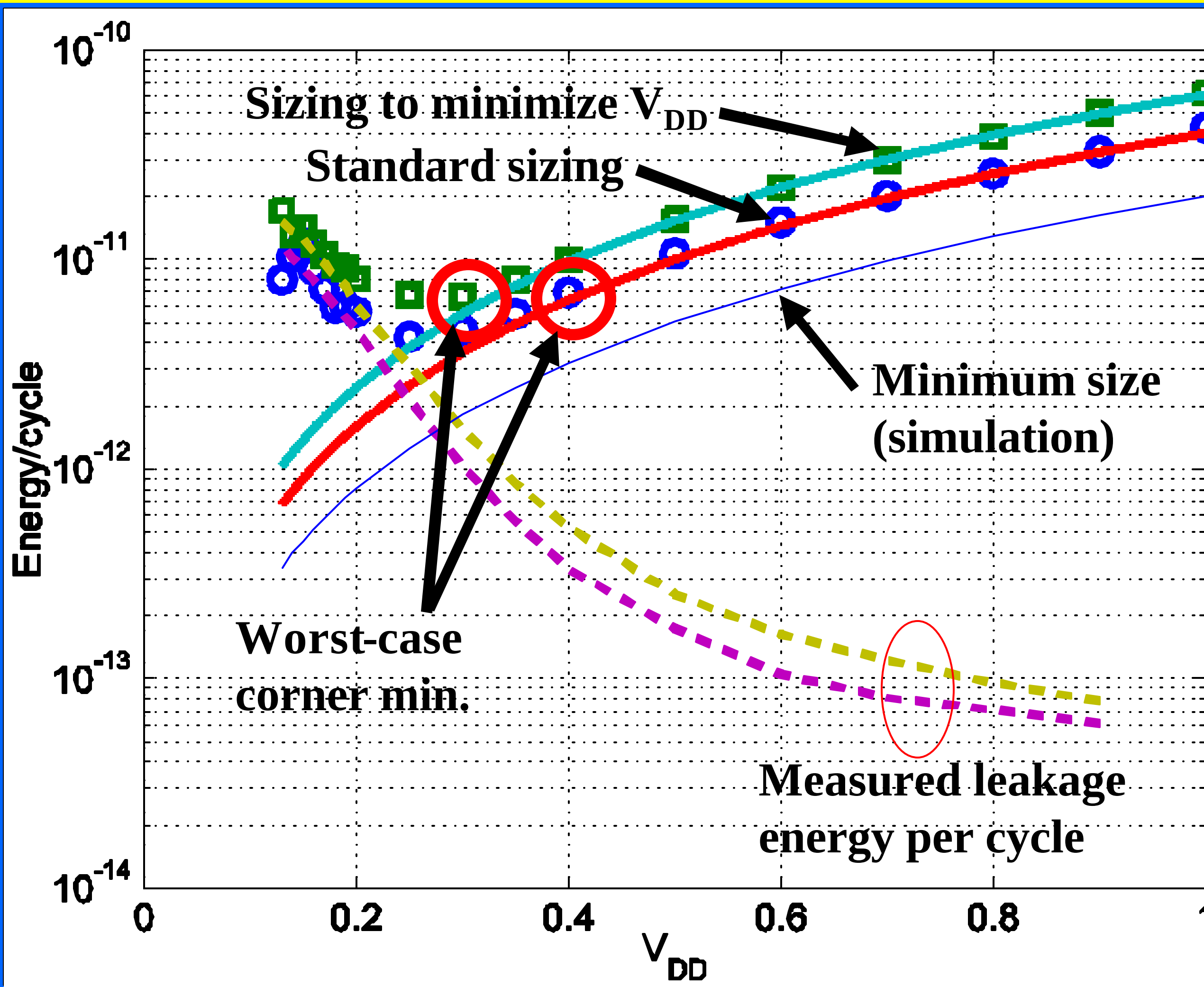


- min E at 250mV for both filters
- Standard sizing FIR 22kHz at opt.
- Min V_{DD} sizing FIR 19kHz at opt.

- Measured energy per cycle versus simulation across V_{DD}

Sub-threshold Sizing Test Chip





- Sizing for min. V_{DD} has 50% overhead at typical corner and <10% savings at worst corner

- Sizing to minimize capacitance is lower energy than sizing to minimize V_{DD}

Conclusions

- Sizing can decrease minimum operating V_{DD}
- When subV_T P/N currents are unbalanced, smaller devices tend to minimize energy per operation

Thank You

- Thank you
- Any Questions?