


Characterizing and Modeling Minimum Energy Operation for Subthreshold Circuits

Benton H. Calhoun and Anantha Chandrakasan

ISLPED

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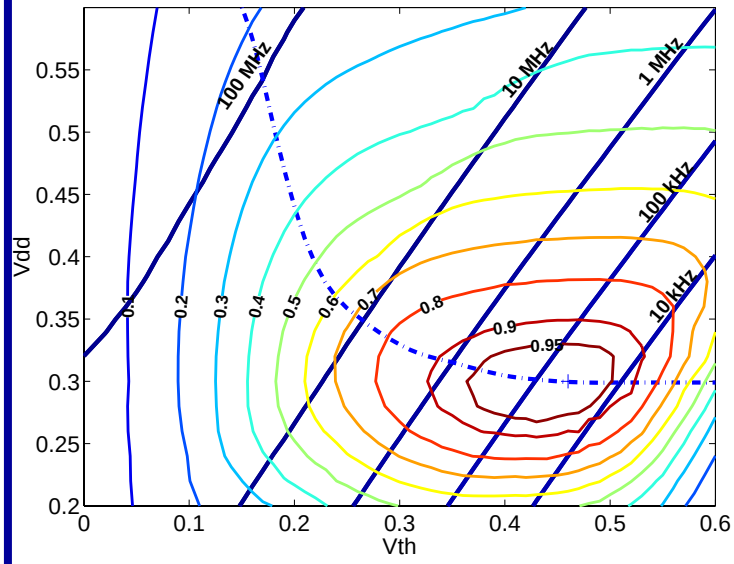
Outline

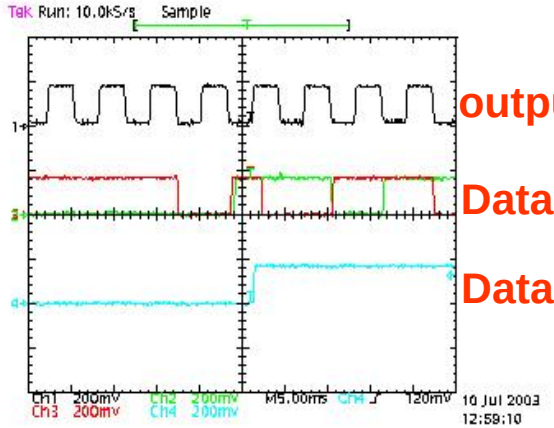
- Introduction to subthreshold operation
- Modeling subthreshold operation
- Minimum energy operation
- Movement of minimum energy point
- Test chip measurements
- Conclusions

Previous Work

- Analog circuits
  - e.g. - E. Vittoz & J. Fellrath, *JSSC*'77
- Digital circuits
  - e.g. – H. Soeleman & K. Roy, *ISLPED*'99
  - J. Kao, M. Miyazaki, & A. Chandrakasan, *ISSCC*'02
  - J. Burr & J. Shott, *ISSCC*'94 (low voltage, but not subthreshold)
- Theoretical Minimum Energy
  - e.g. – R. Swanson & J. Meindl, *JSSC*'72
- Minimum Energy Point Demonstrated
  - Theoretical – e.g. - A. Wang & A. Chandrakasan, *ISVLSI*'03
  - 180mV FFT processor - A. Wang and A. Chandrakasan, *ISSCC*'04
  - Model; applied to off-the-shelf processors – Zhai, Blaauw, Sylvester, & Flautner, *DAC*'04



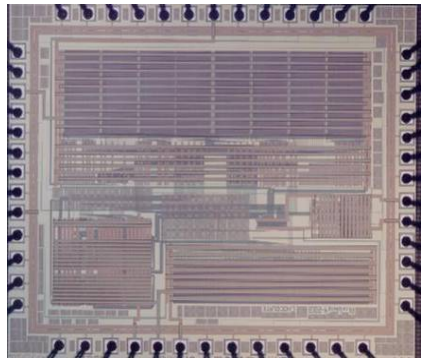
A. Wang and A. Chandrakasan, ISVLSI, 2003



output clock

DataOutputs

DataReady



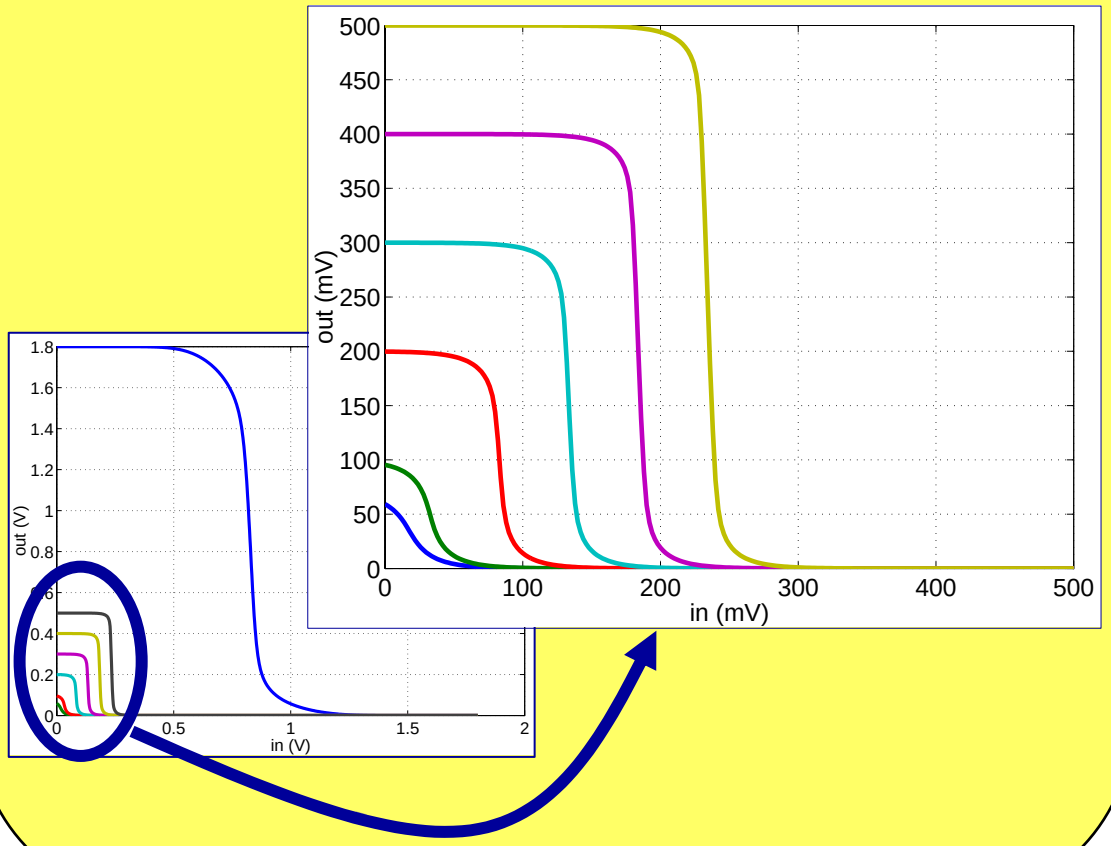
180mV FFT Processor

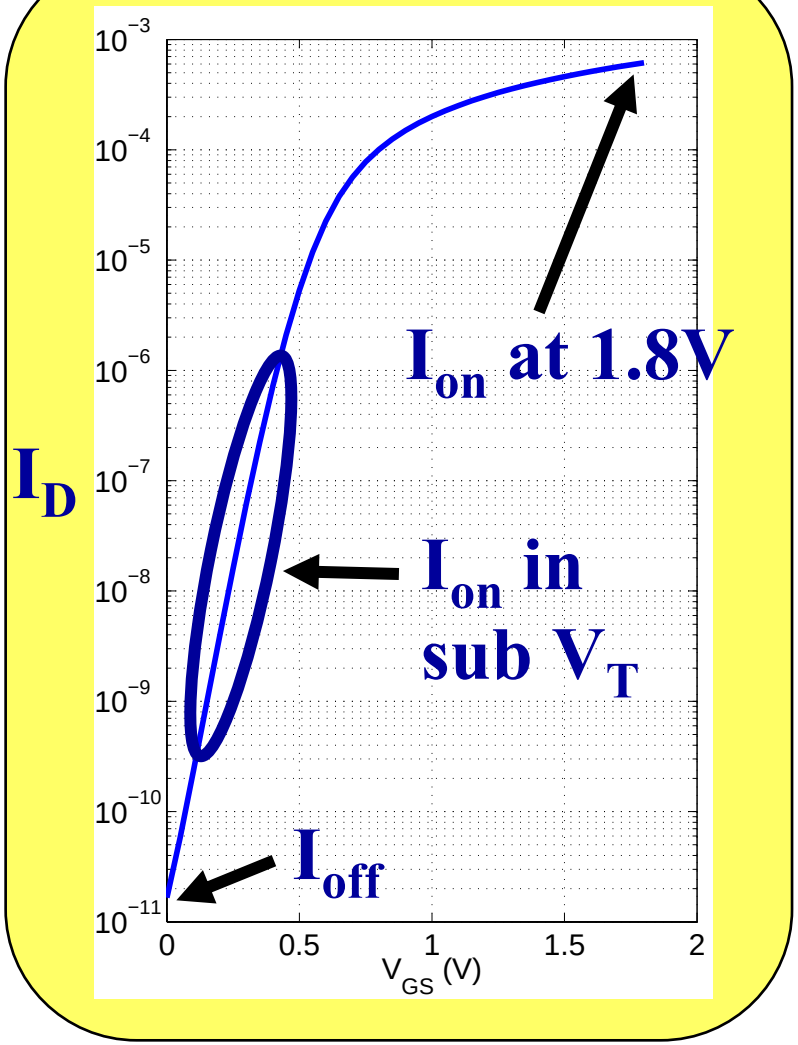
A. Wang and A. Chandrakasan, ISSCC. 2004

Subthreshold Operation Basics

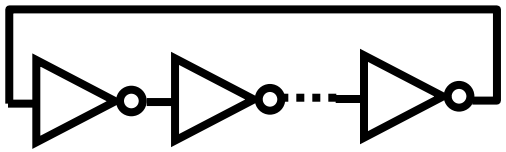
- Subthreshold logic operates with $V_{DD} < V_T$
- Both on and off current are subthreshold "leakage"

Inverter VTCs

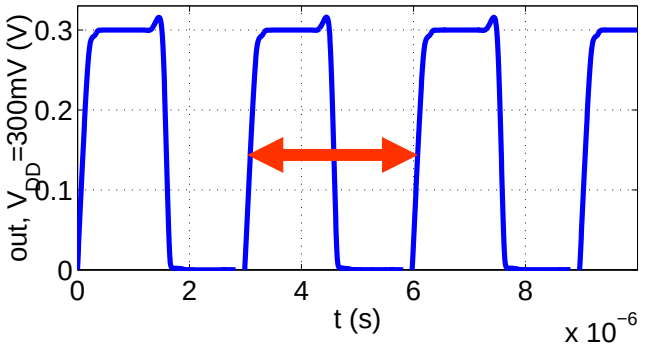




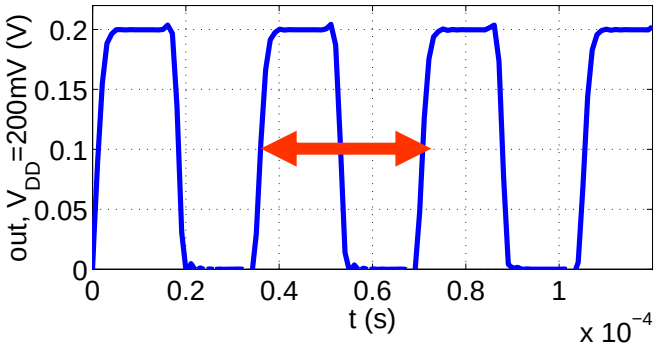
Subthreshold Operation Basics



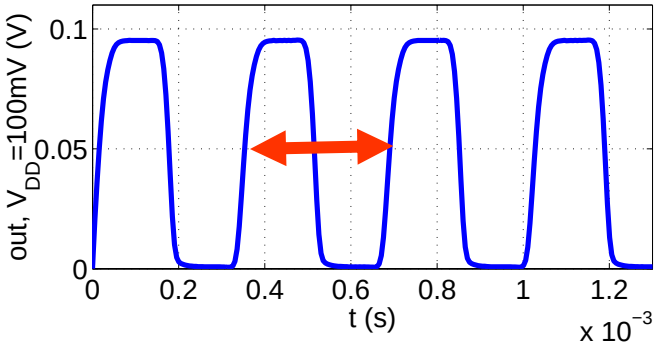
11 stages



330kHz
300mV



29kHz
200mV



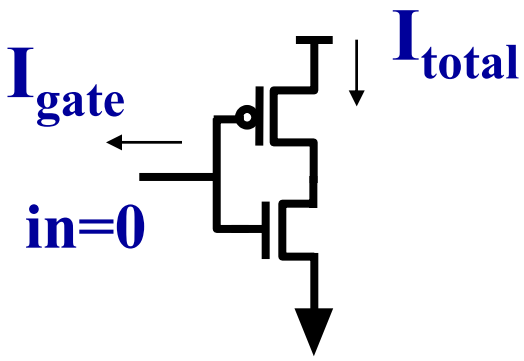
3kHz
100mV

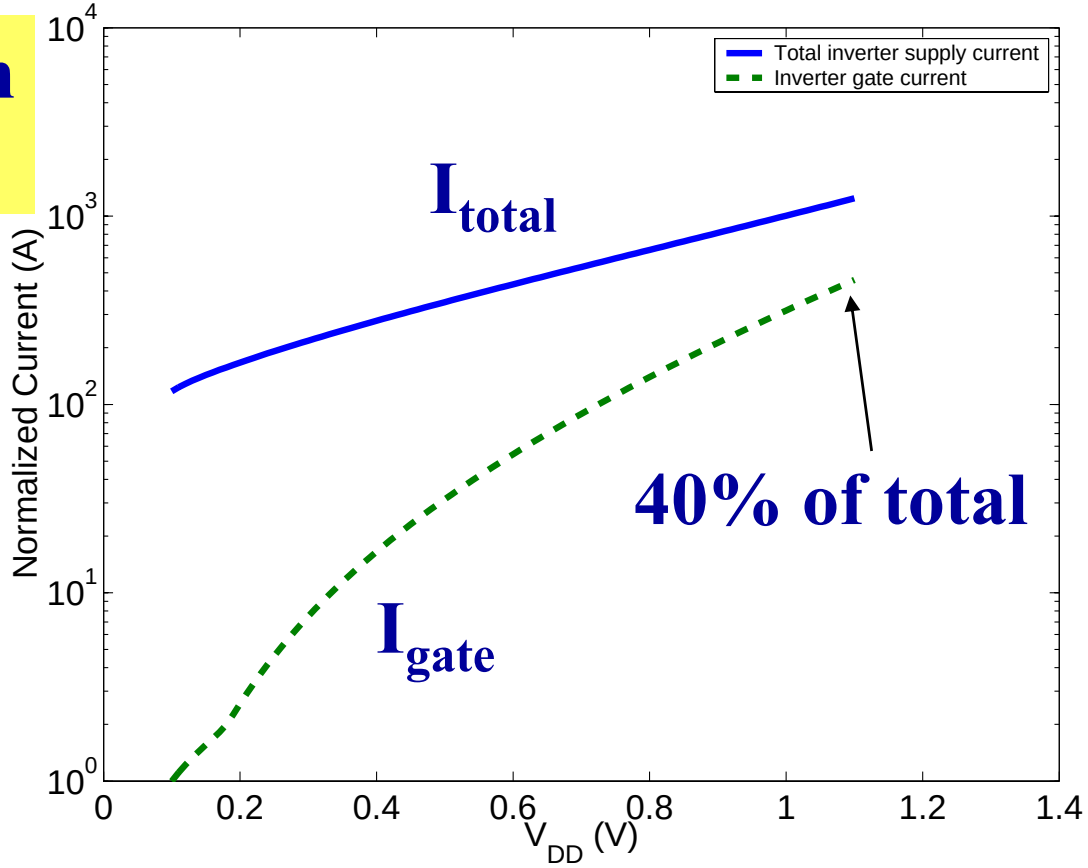
- Simple ring oscillator shows functionality in deep sub V_T
- Delay increases exponentially in sub V_T

Sources of Leakage and V_{DD} Scaling

- Components of Transistor Off-Current
  - Subthreshold current – the focus of this presentation
  - Gate leakage – rolls of with V_{DD} faster than sub V_T current
  - GIDL – a problem at low V_{GS}, high V_{DS} (Keshavarzi, et al., ITC'97)
  - Junction leakage – negligible at low V_{DD}

Gate leakage contribution to Ioff for 90nm



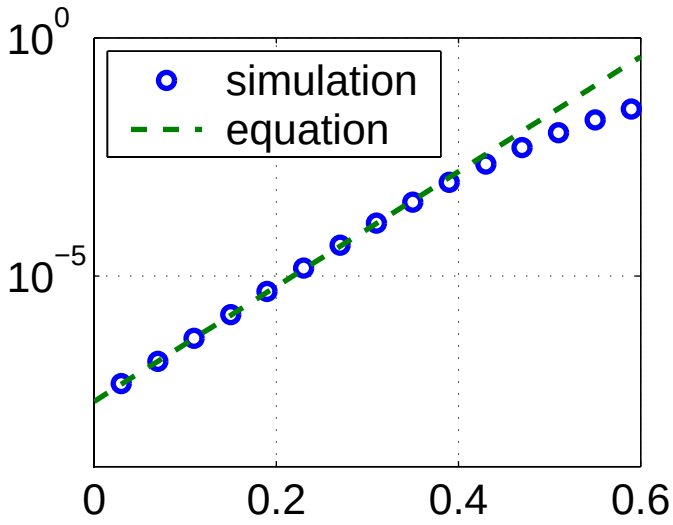


Modeling Subthreshold Current

- **Subthreshold current:**

$$I_{SUB} = I_o e^{\frac{V_{GS} - V_T + \eta V_{DS}}{nV_{th}}} \left(1 - e^{-\frac{V_{DS}}{V_{th}}}\right)$$

  - Optional DIBL and low-V_{DS} roll-off modeling



Generic Equation for Energy per Operation

$$E_{TOTAL} = E_{ACTIVE} + E_{LEAKAGE}$$

$$E_{TOTAL} = C \cdot V_{DD}^2 + I_{OFF} V_{DD} T_D$$

Switched capacitance

Off-current

Delay per operation

Modeling Characteristic Inverter

Equation for Inverter Delay

Parameters for the gate account for both NMOS and PMOS

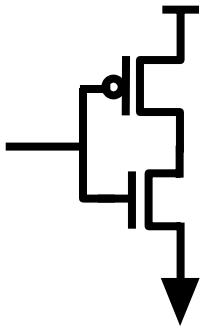
Fitting Parameter

Inverter Switched Cap

On Current

$$t_d = \frac{KC_g V_{DD}}{I_{on}}$$

$$= \frac{KC_g V_{DD}}{I_{o,g} e^{\frac{V_{GS} - V_{T.g}}{nV_{th}}}}$$



Normalize total using Ceff

Normalize total Ioff to characteristic inverter using Weff:

$$I_{OFF} = W_{eff} I_{o,g} e^{\frac{-V_{T.g}}{nV_{th}}}$$

Normalize total delay to characteristic inverter using Logic Depth (L_{DP}):

$$T_D = t_d \cdot L_{DP}$$

$$E_{TOTAL} = C \cdot V_{DD}^2 + I_{OFF} V_{DD} T_D$$

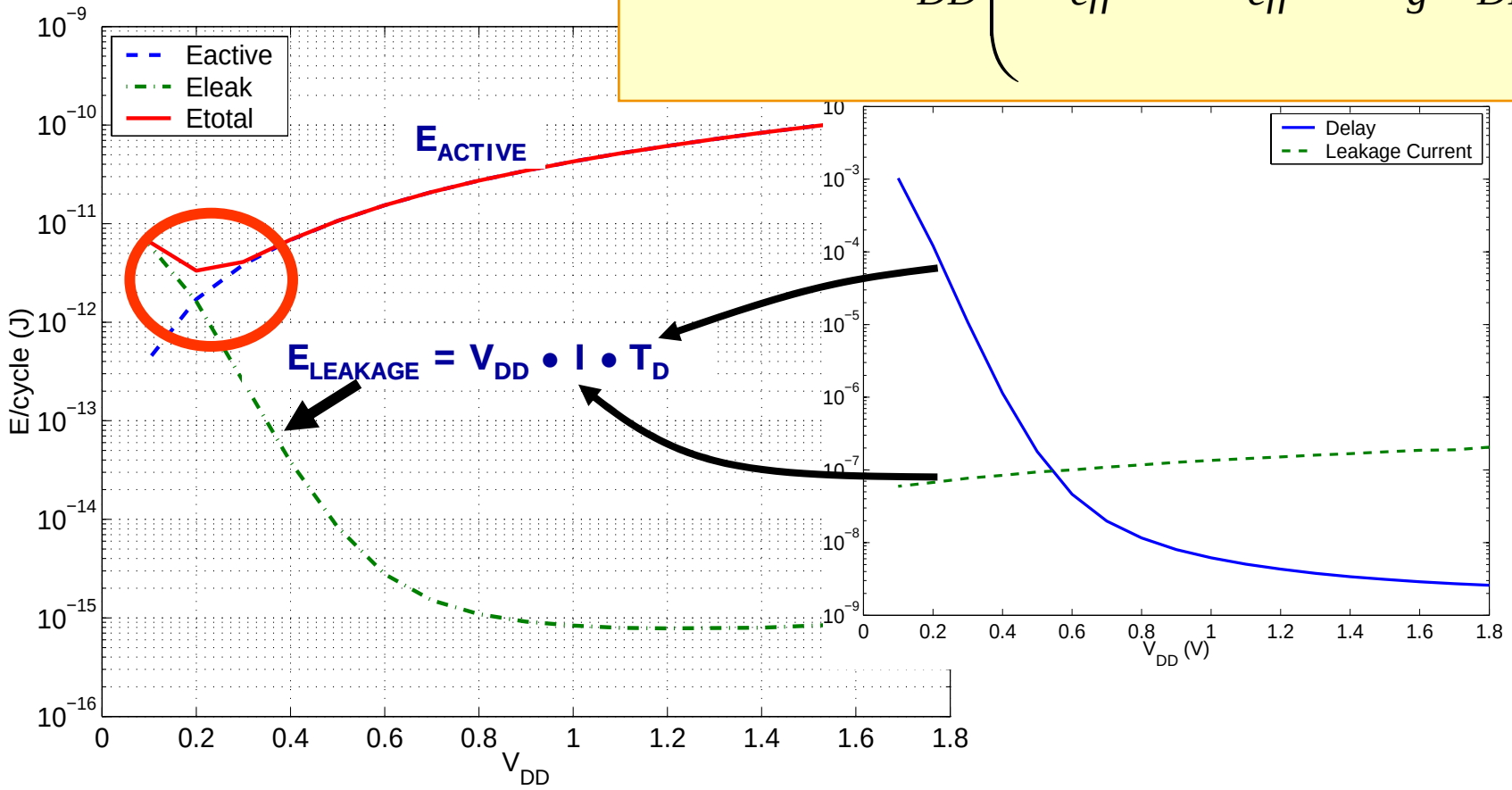
Minimum Energy Point for Digital Circuits

Active Energy **Leakage Energy**

After substituting,

$$E_{Total} = C_{eff} V_{DD}^2 + W_{eff} L_{DP} K C_g V_{DD}^2 e^{-\frac{V_{DD}}{nV_{th}}}$$

$$= V_{DD}^2 \left(C_{eff} + W_{eff} K C_g L_{DP} e^{-\frac{V_{DD}}{nV_{th}}} \right)$$



Solving for Minimum Energy Point

$$E_{Total} = C_{eff} V_{DD}^2 + W_{eff} L_{DP} K C_g V_{DD}^2 e^{-\frac{V_{DD}}{nV_{th}}}$$

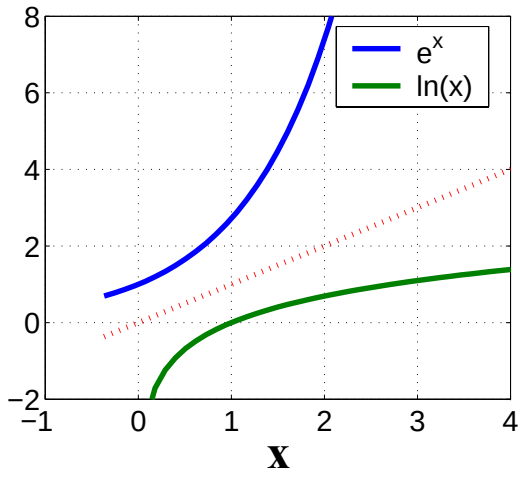
Solve for optimum V_{DD}: set derivative equal to 0

$$\frac{\partial E_{TOTAL}}{\partial V_{DD}} = 2C_{eff} V_{DD} + 2W_{eff} L_{DP} K C_g V_{DD} e^{\frac{V_{DD}}{nV_{th}}} + \frac{-W_{eff} L_{DP} K C_g V_{DD}^2}{nV_{th}} e^{\frac{V_{DD}}{nV_{th}}} = 0$$

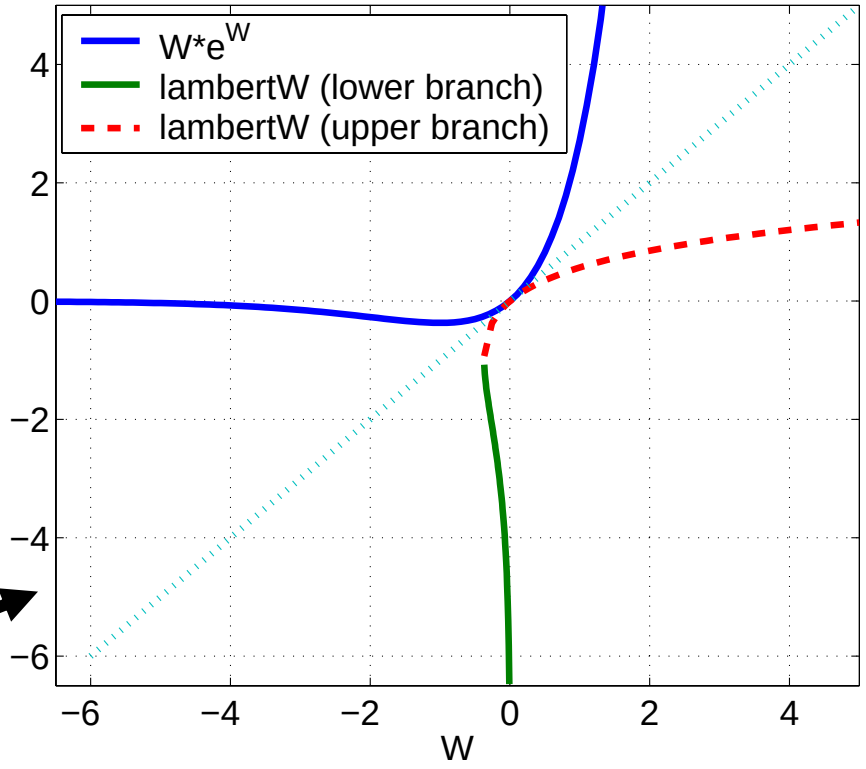
Solving yields (independent of V_T) :

$$V_{DDopt} = nV_{th}(2 - \text{lambertW}(\beta))$$

with: $$\beta = \frac{-2C_{eff}}{W_{eff} L_{DP} K C_g} e^2 > -e^{-1}$$



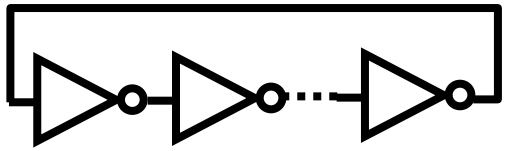
Analogous to e^x and ln(x)



LambertW is the inverse of $f(W)=We^W$

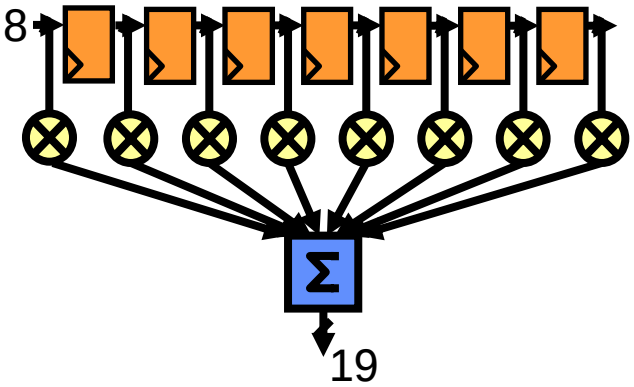
Examples of Optimum

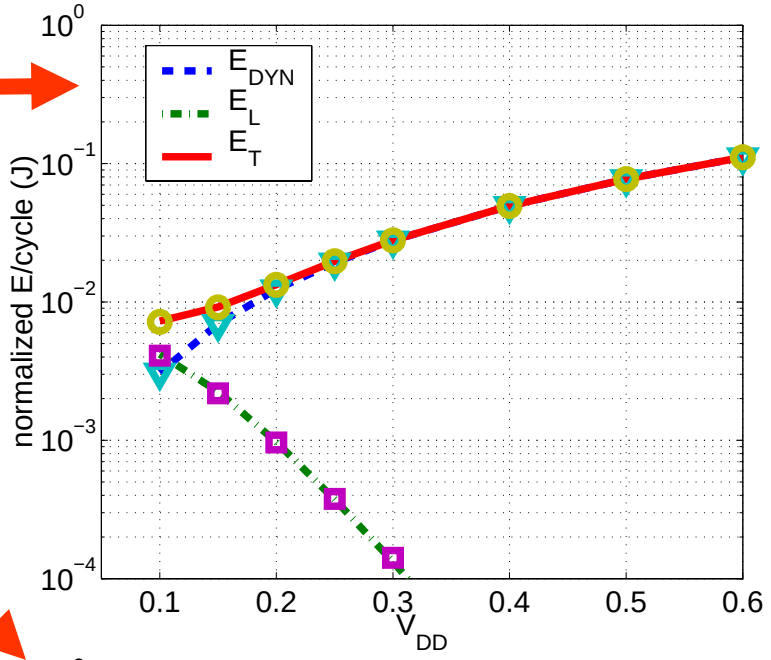
Unloaded Ring Oscillator

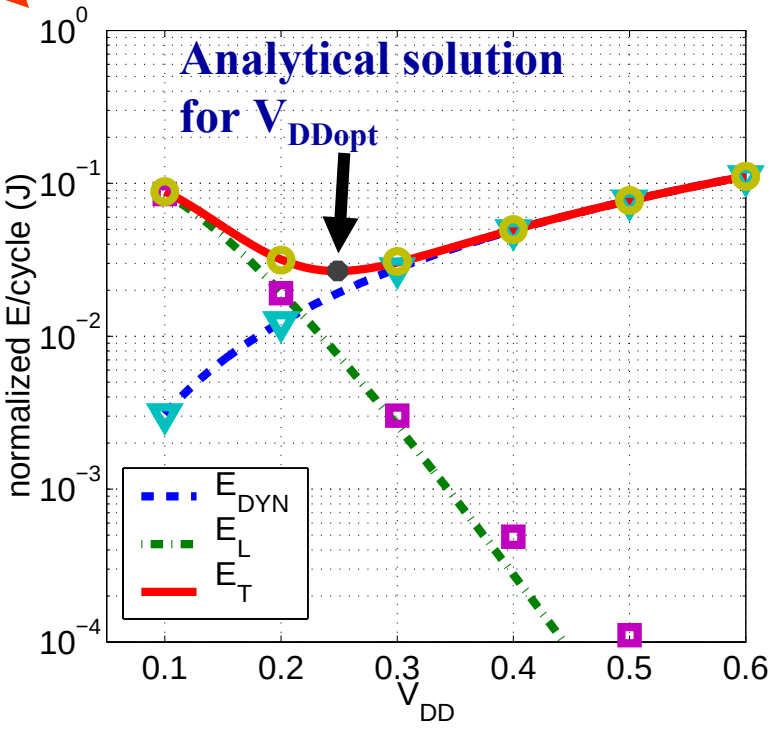


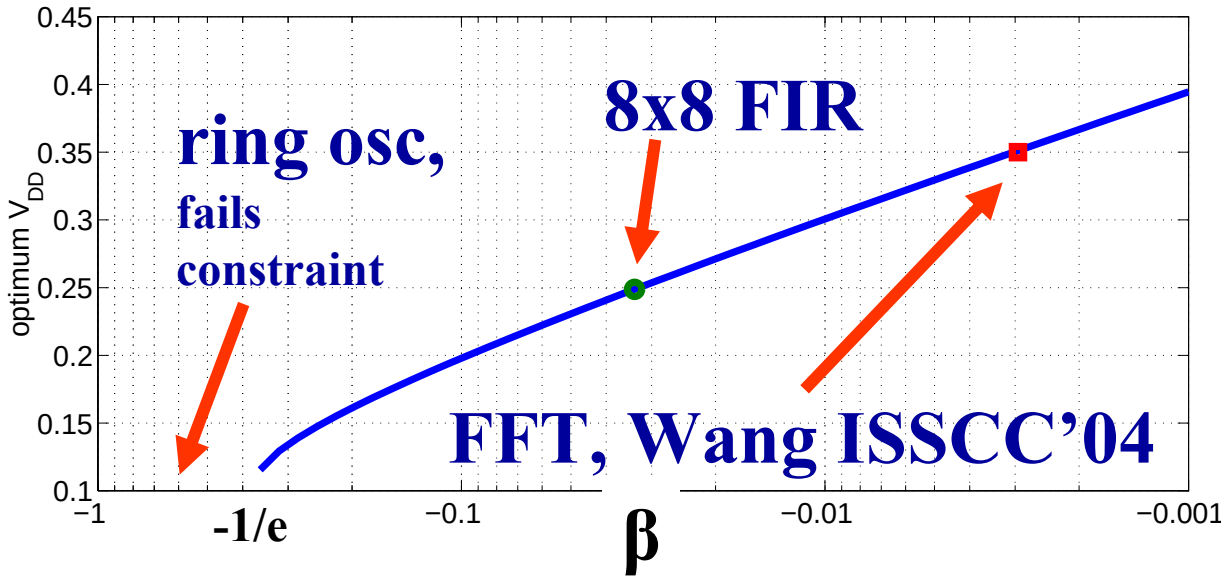
8b,8tap FIR filter

Baugh-Wooley Multipliers









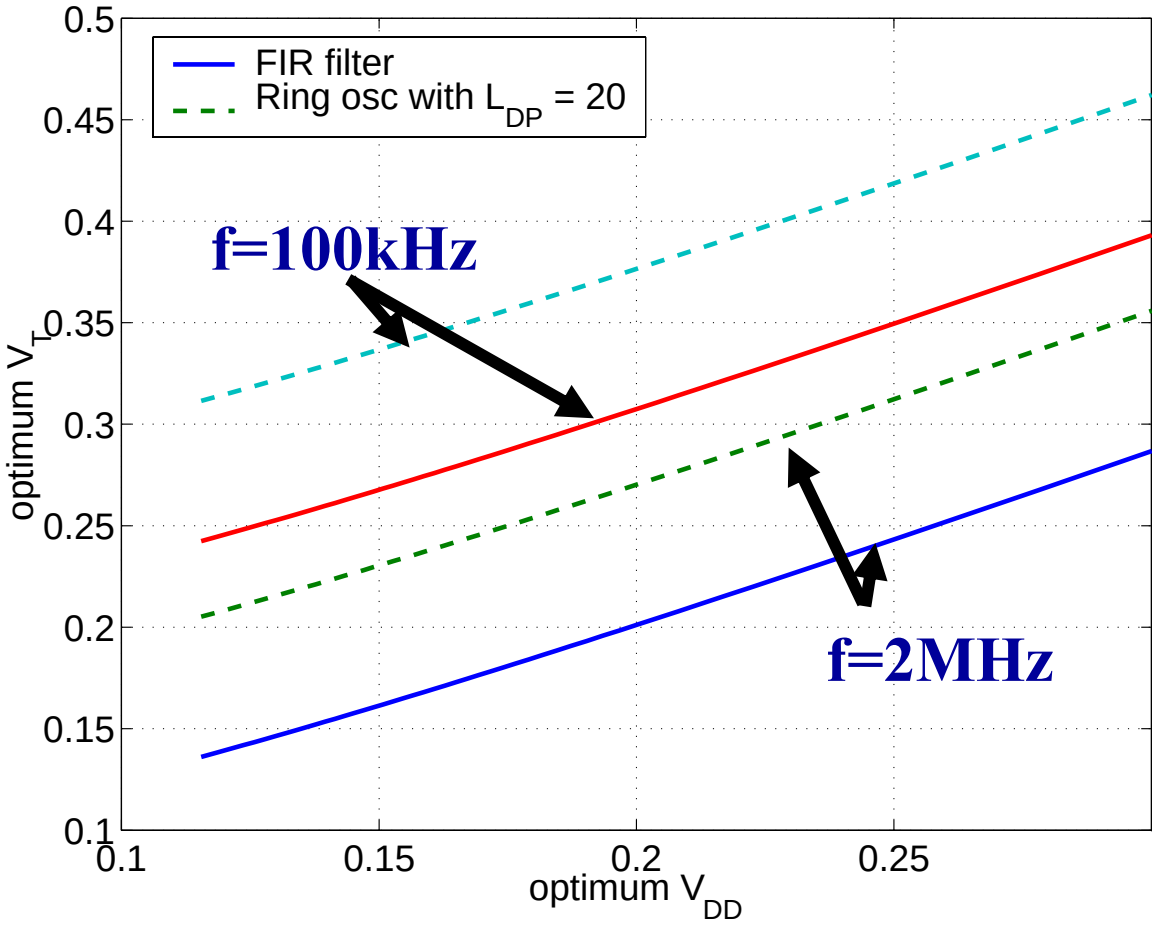
Optimum V_T

Plugging V_{DDopt} into the equation $f=(t_d L_{DP})^{-1}$ for a given f gives:

$$V_{Topt} = V_{DDopt} - nV_{th} \ln\left(\frac{fKC_g L_{DP} V_{DDopt}}{I_{o,g}}\right)$$

Select V_T based on the desired frequency, BUT

- **In standard bulk CMOS, V_T is difficult to change**
- **Body bias requires SOI or triple well**



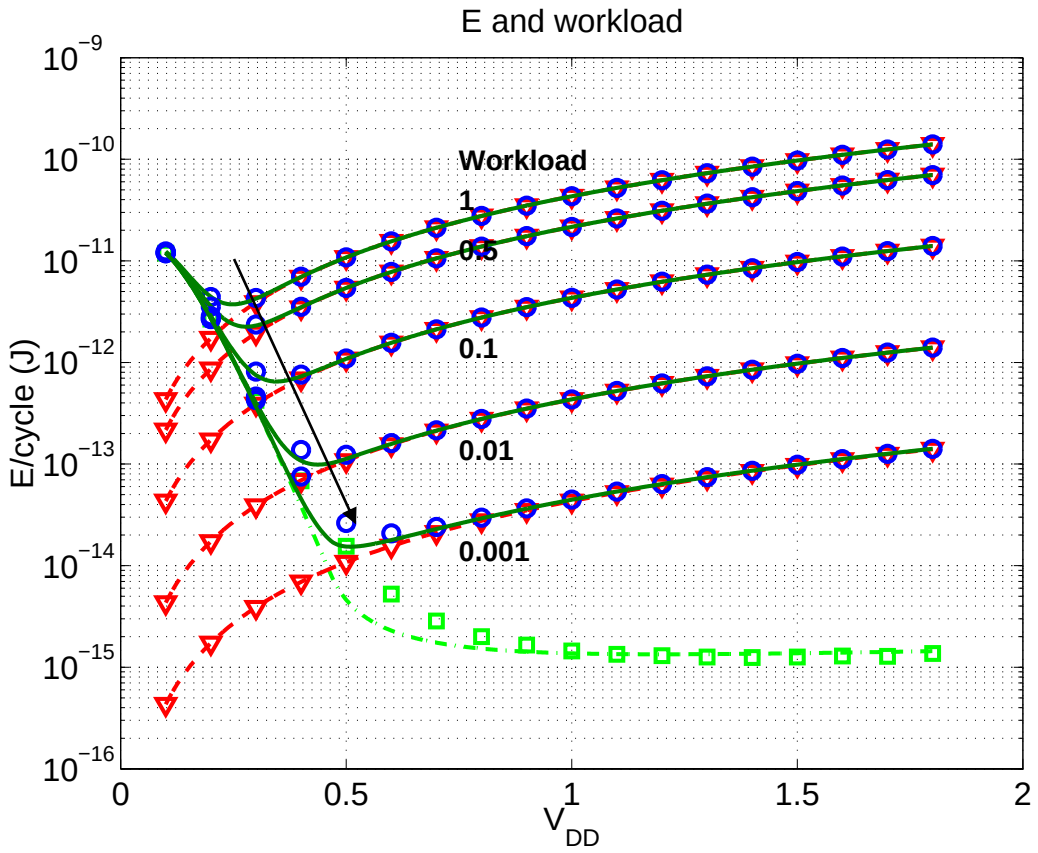
Workload

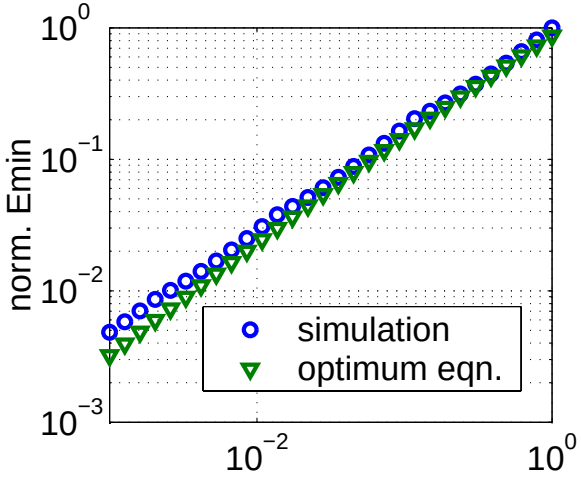
Workload: Amount of work (active energy) per operation relative to worst-case

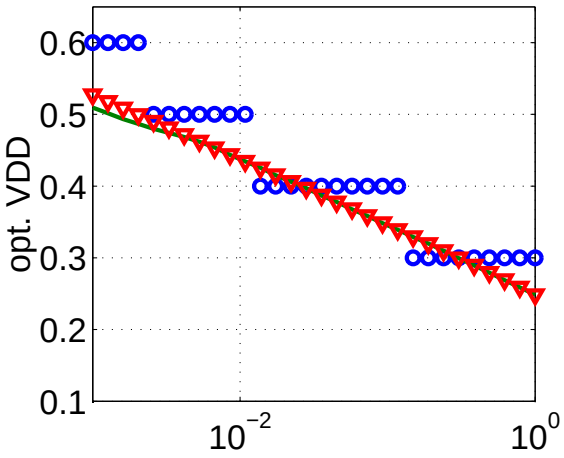
Examples of workload reduction:
- **Filter precision is reduced**
- **Video frame changes minimally relative to previous frame**

Ceff scales with workload, ω

$$\beta = \frac{-2\omega C_{eff}}{W_{eff} L_{DP} K C_g} e^2 > -e^{-1}$$







Duty Cycle

Duty Cycle: Percentage of active operation versus idle

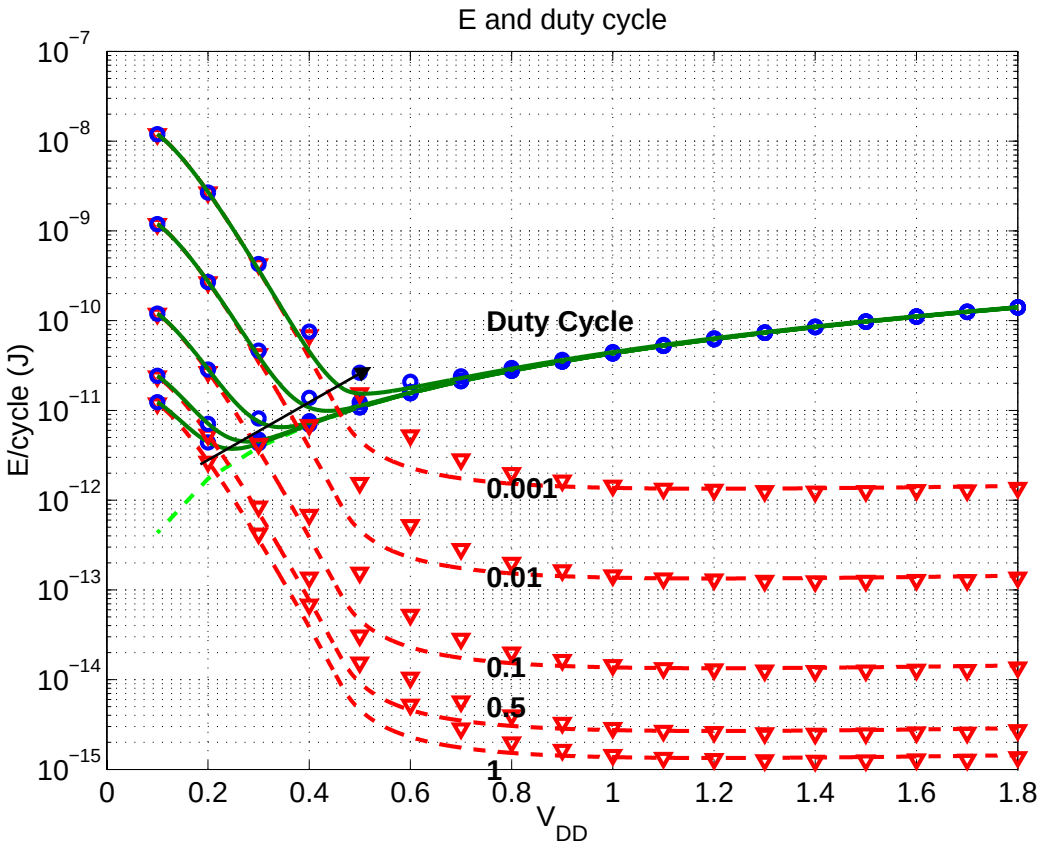
Examples of duty cycle reduction:
- **Waiting for data**

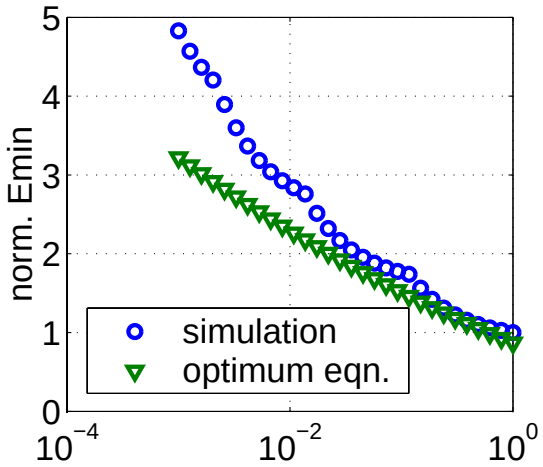
Weff scales inversely with duty cycle, d

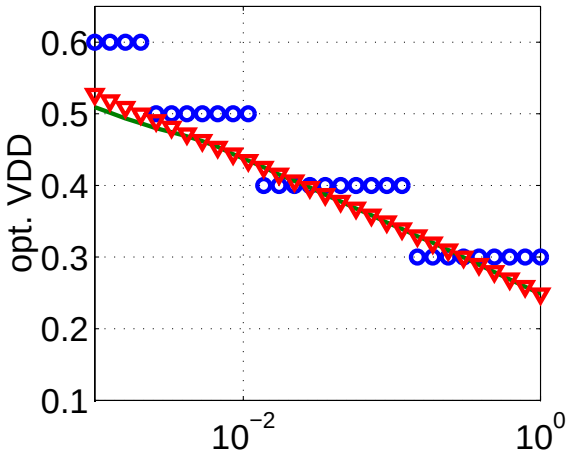
$$\beta = \frac{-2C_{eff}}{\frac{W_{eff}}{d} L_{DP} K C_g} e^2 > -e^{-1}$$

Incorporating duty cycle and workload: same effect on V_{DDopt}

$$\beta = \frac{-2\omega C_{eff}}{\frac{W_{eff}}{d} L_{DP} K C_g} e^2 > -e^{-1}$$







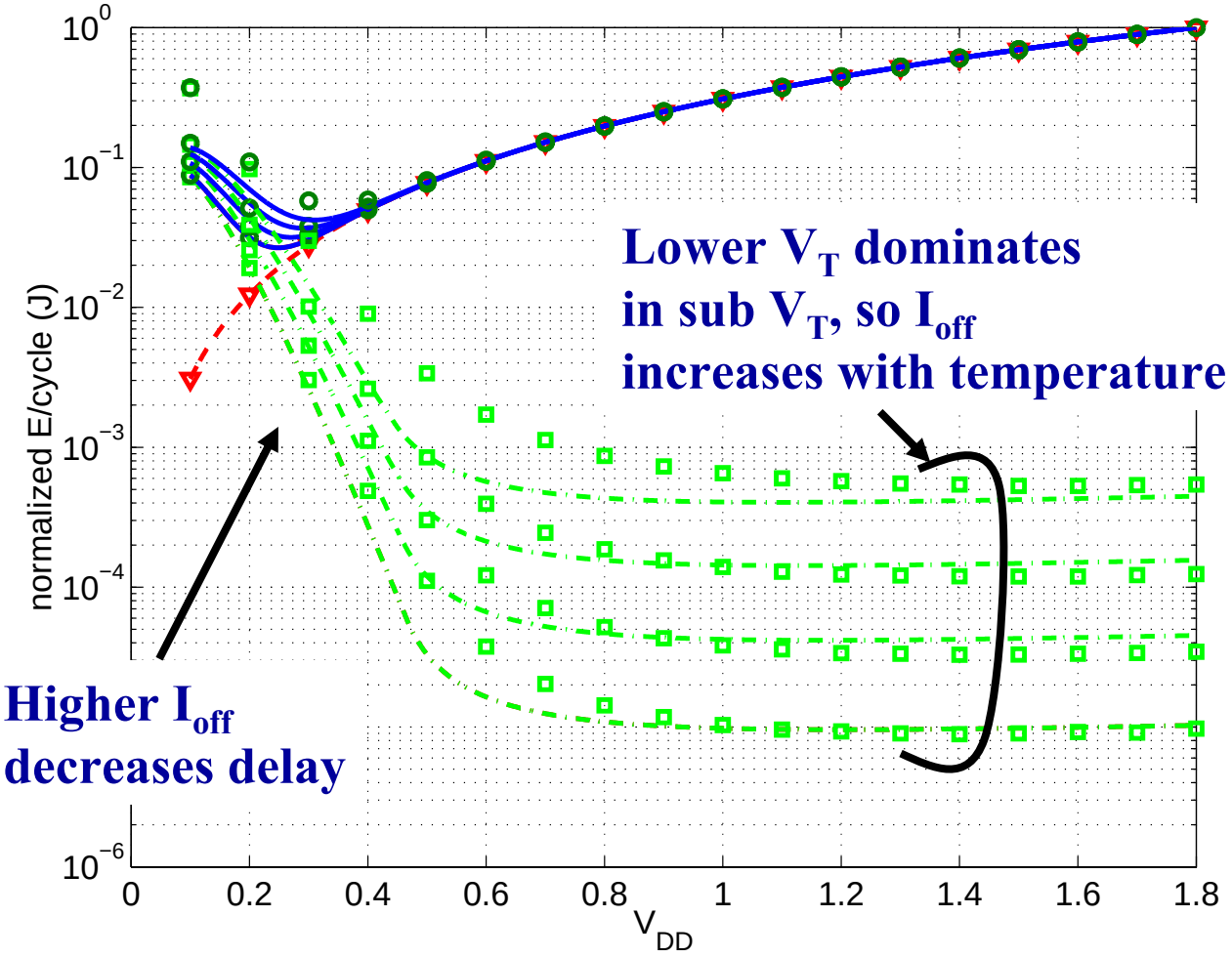
Temperature Variation

- Modeled Temperature effect numerically using:

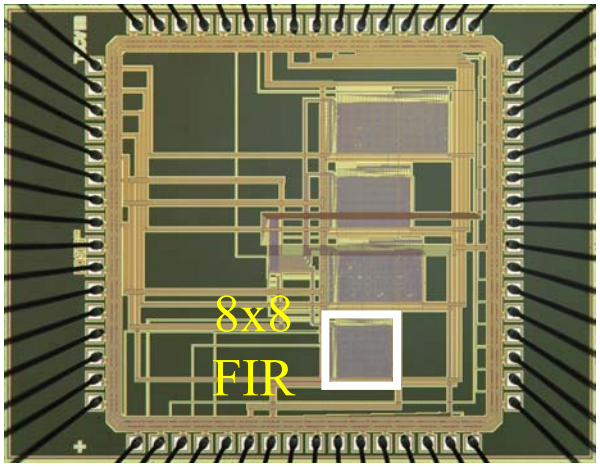
$$V_T(T)=V_T(T_0)-K_T T \quad \& \quad \mu(T)=\mu(T_0)(T/T_0)^{-M}$$

A. Bellaouar, et al., *Trans. on Circuits and Systems*, 1998.

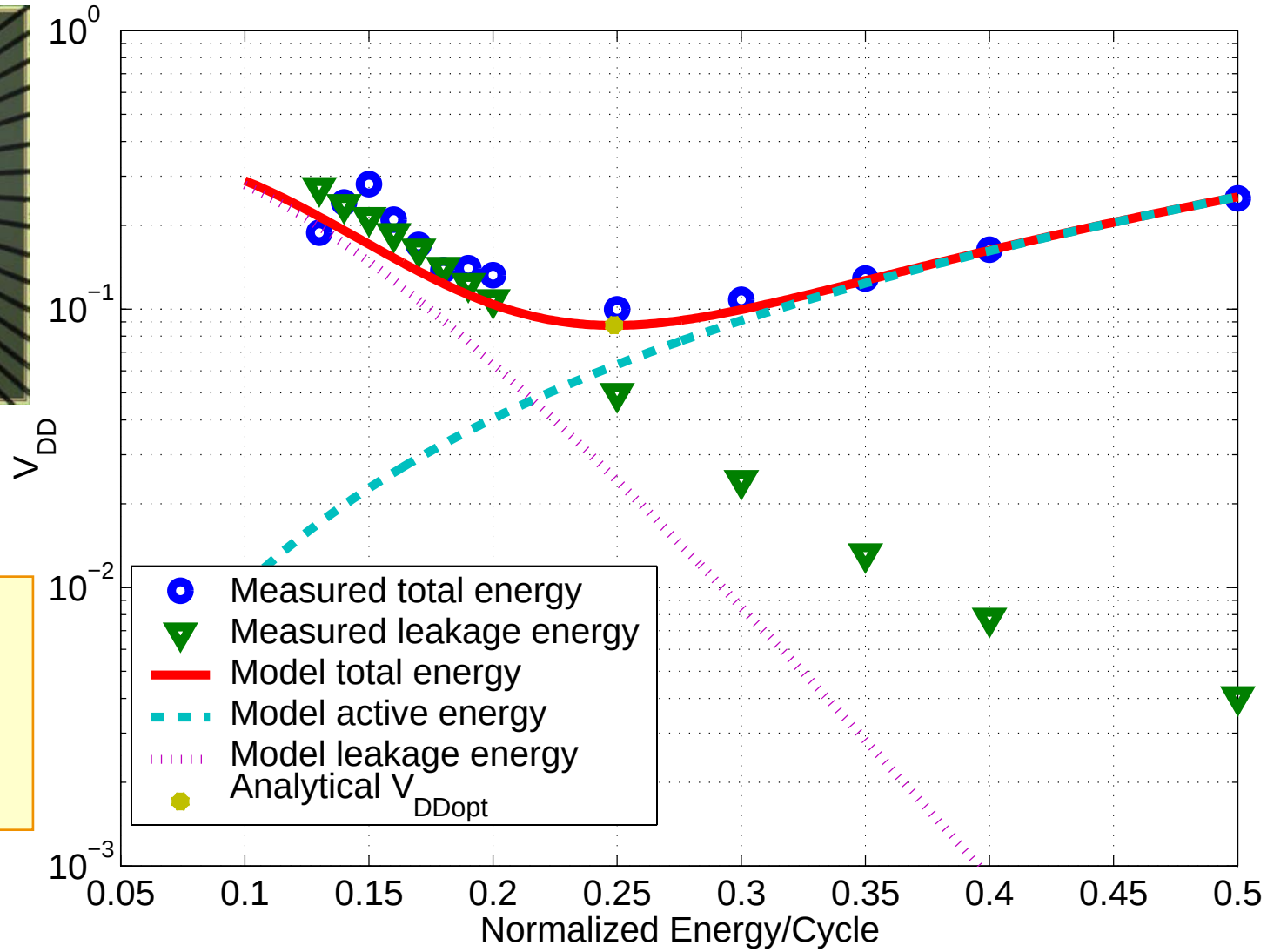
Net impact of T on V_{DDopt} is small, but would increase at lower duty cycle or workload.



Comparison with FIR chip



CICC'04 to appear



Model matches measured data quite well

- **Difference in fabricated V_T from simulated V_T causes the mismatch for leakage energy (both leakage current and subthreshold frequency measurements differed somewhat from simulations**

Conclusions

- Model shows minimum energy point in subthreshold
- Matches simulated and measured data
- After fitting to a design, useful for fast estimation of behavior under varying environment and operating conditions

Thank You

- Thank you for your attention
- Research supported by TI and DARPA
- Any Questions?