An Oscilloscope Array for High-Impedance Device Characterization

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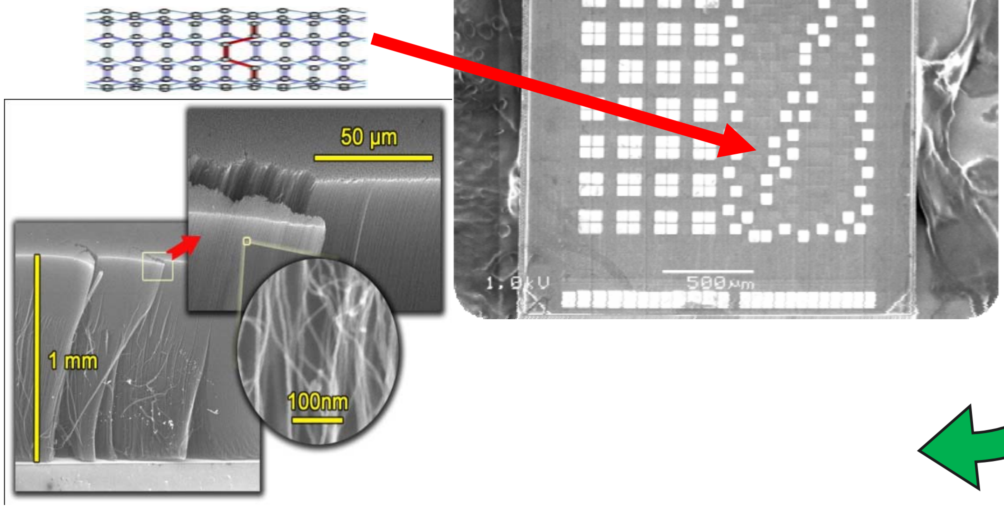
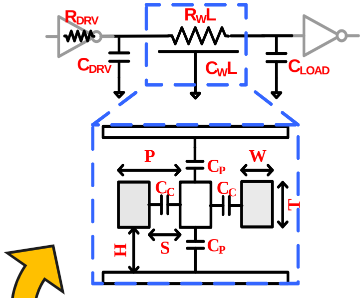
Connecting Systems to Emerging Devices

- **Develop Device Models**
  - Enable use for system level exploration

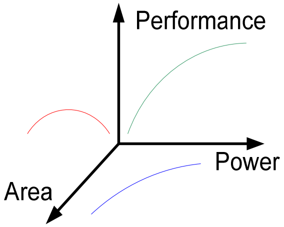
CNT Characterization

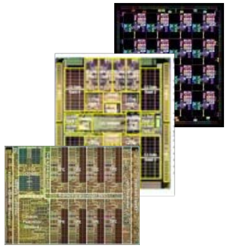


Micro-architect Circuits



Extract Tradeoff Curves



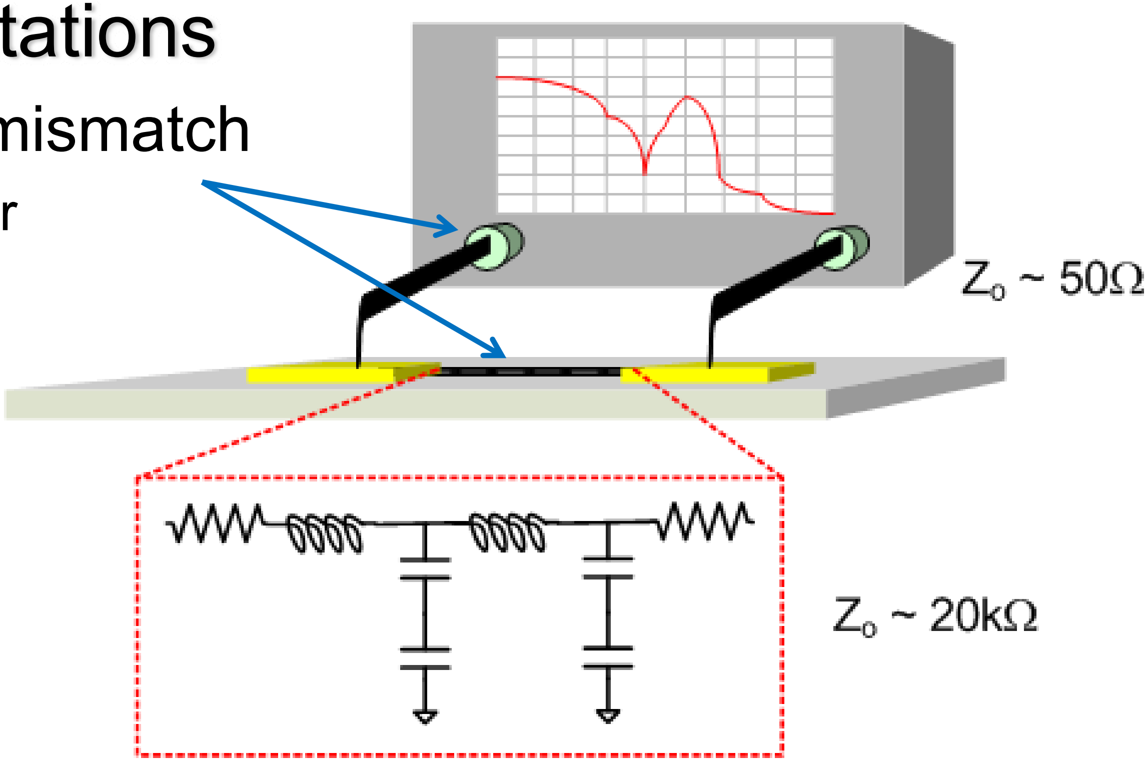


Make Informed Architecture Choices

- **Feedback for device research**
  - Ease new device testing/characterization
  - Enables comparison of emerging devices

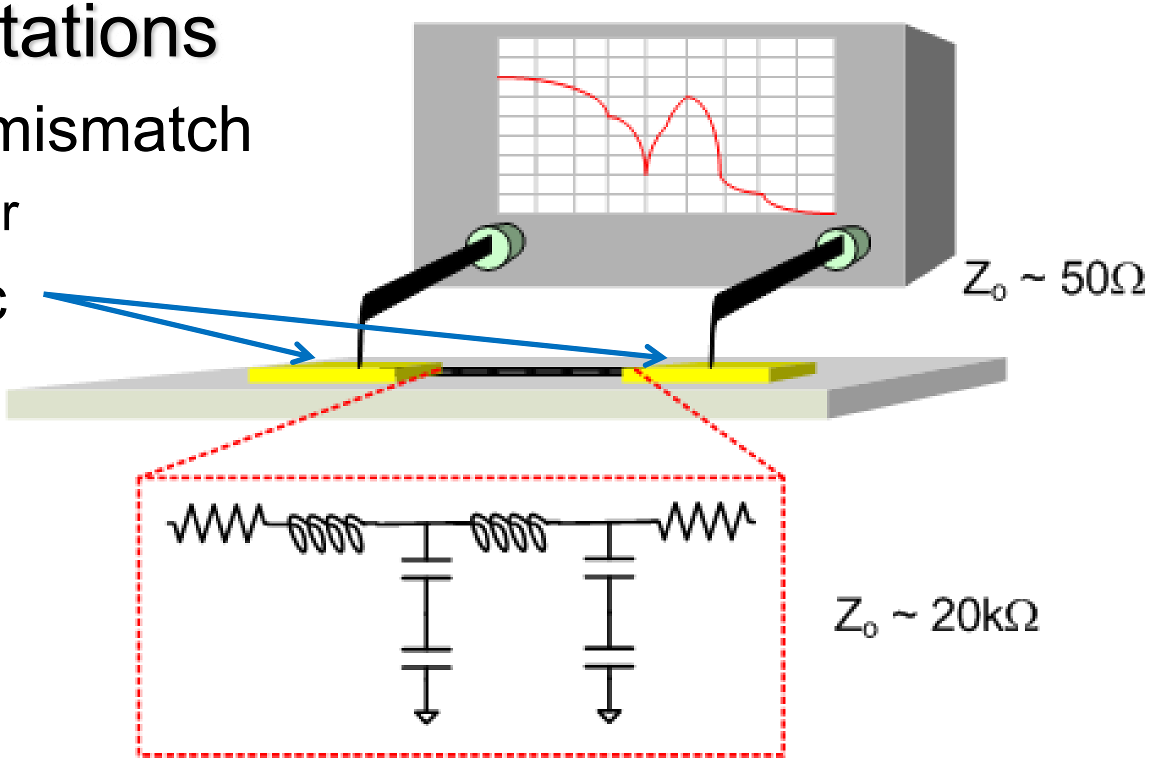
Traditional Measurement Techniques

- Measurement Limitations
  - Large impedance mismatch
    - Poor power transfer



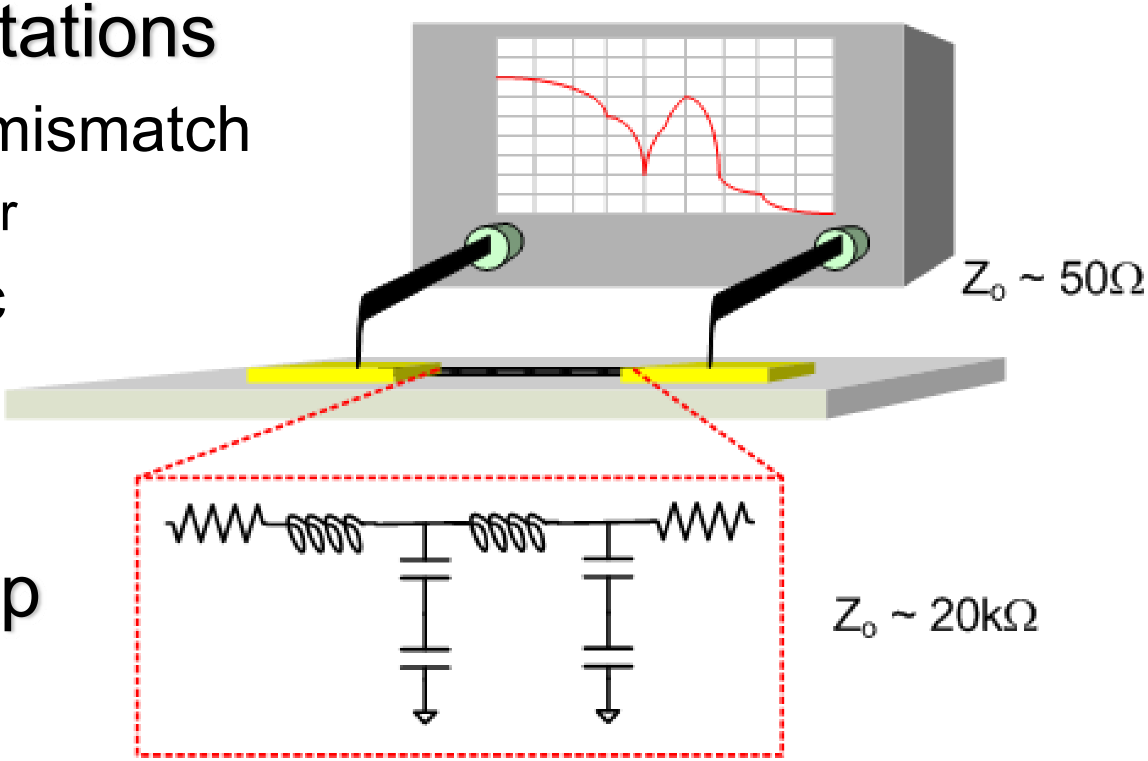
Traditional Measurement Techniques

- Measurement Limitations
  - Large impedance mismatch
    - Poor power transfer
  - Large test parasitic
    - Limits accuracy
    - Limits bandwidth



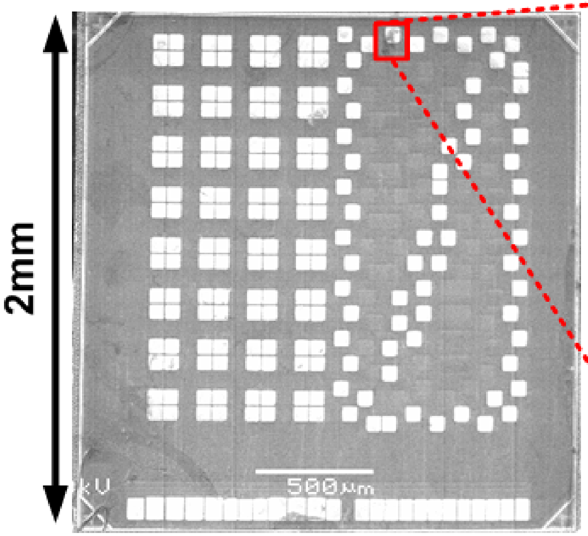
Traditional Measurement Techniques

- Measurement Limitations
  - Large impedance mismatch
    - Poor power transfer
  - Large test parasitic
    - Limits accuracy
    - Limits bandwidth
- Physical Test Setup
  - Cumbersome
  - Difficult to reproduce
  - Limited number of measurements

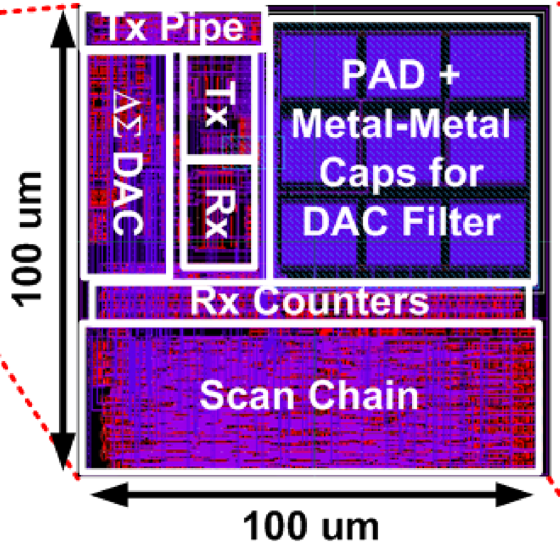


Silicon Sub-sampling Scope

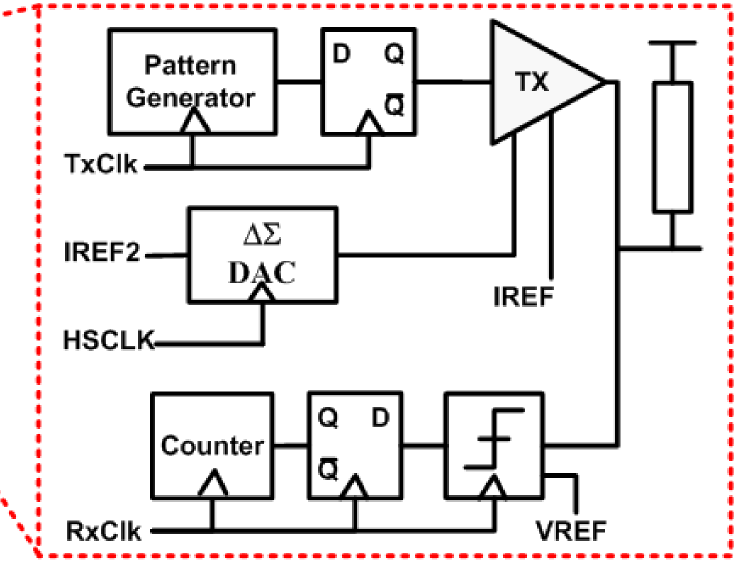
Chip SEM



Transceiver Layout

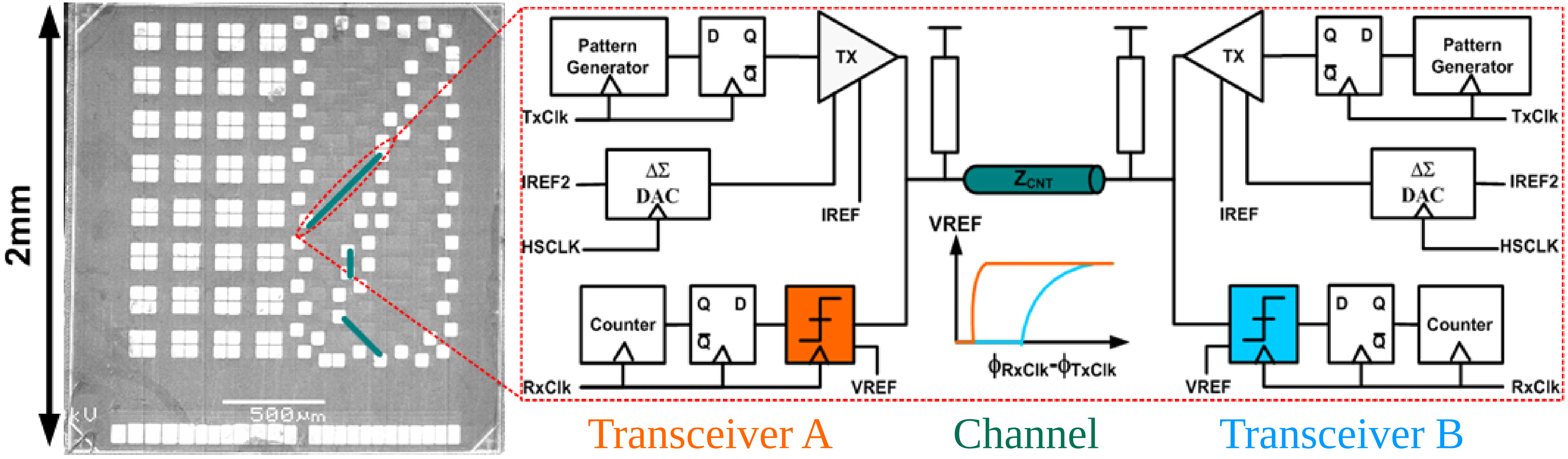


Transceiver Block Diagram



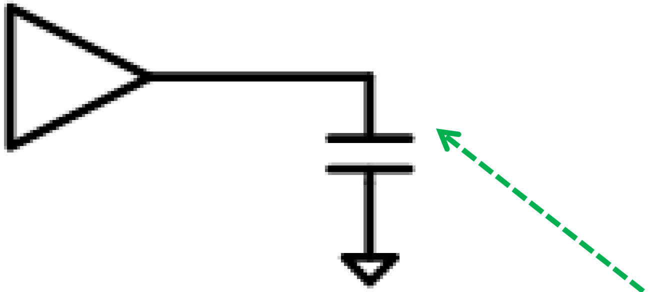
- ❑ Create a flexible pad interface
  - 16 x 16 array of 52x52µm pads
  - Independent 100x100µm transceivers talking to each pad
- ❑ Adjustable termination impedance to improve power transfer
- ❑ Reduce pad/interface parasitic
  - Improve measurement accuracy – less to de-embed

Silicon Sub-sampling Scope



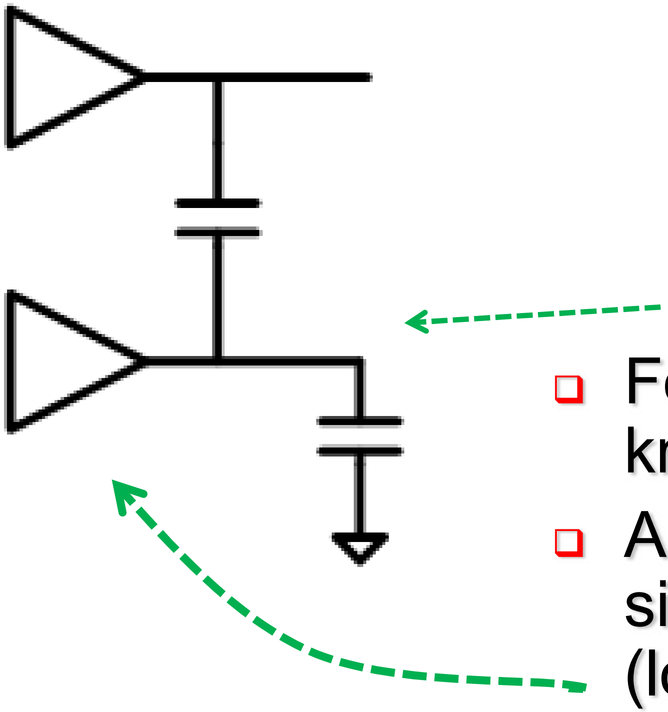
- DUT creates the ‘channel’ for the link
  - Interface allows for arbitrary connections between pads
- Measure step response (TDR, TDT) using sub-sampling
- Key Challenges:
  - Simultaneously enabling wide bandwidth input with high impedance
  - Accurate measurements with small devices
  - Fine time resolution (10’s ps) with large time range (100’s ns)

Transmitter and Pad



- Large pad capacitance

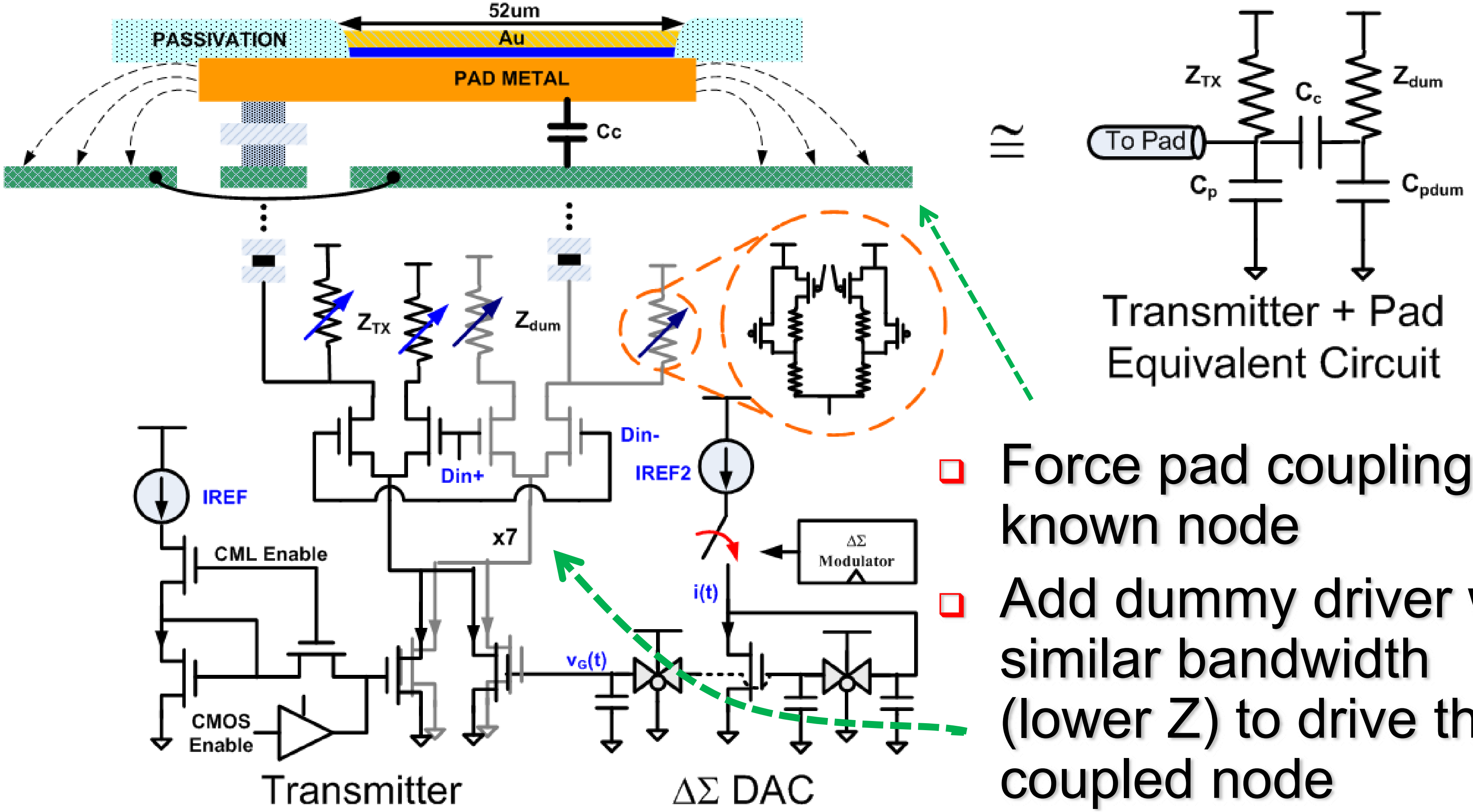
Transmitter and Pad



- Force pad coupling to a known node
- Add dummy driver with similar bandwidth (lower Z) to drive the coupled node

- Effectively null out the ~60fF pad capacitance

Transmitter and Pad

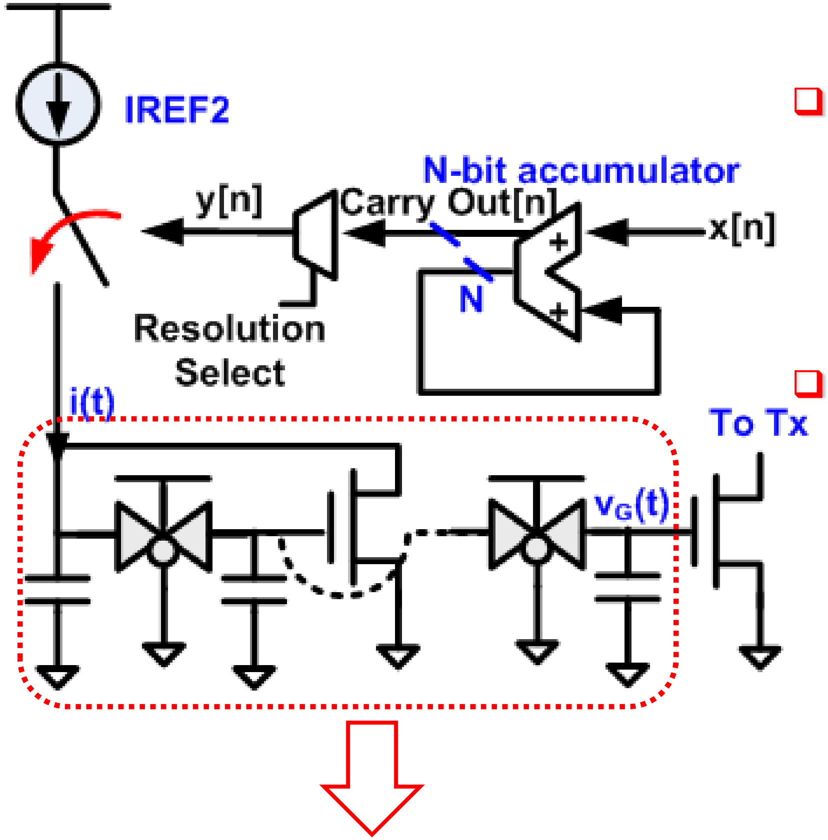


Transmitter + Pad Equivalent Circuit

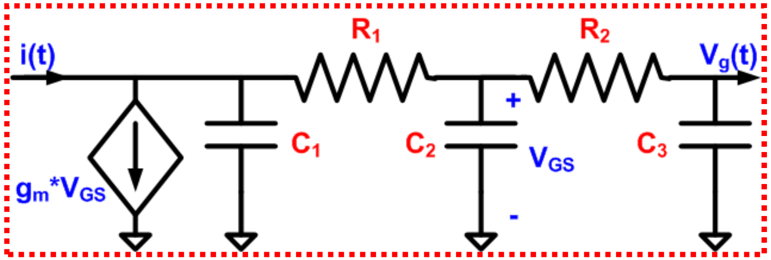
- Force pad coupling to a known node
- Add dummy driver with similar bandwidth (lower Z) to drive the coupled node

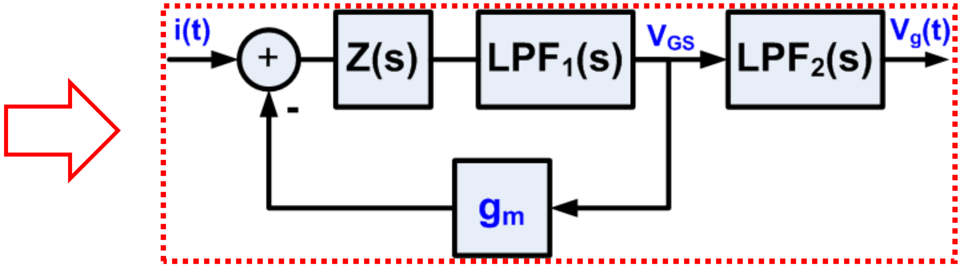
- Effectively null out the ~60fF pad capacitance

Delta-Sigma DAC



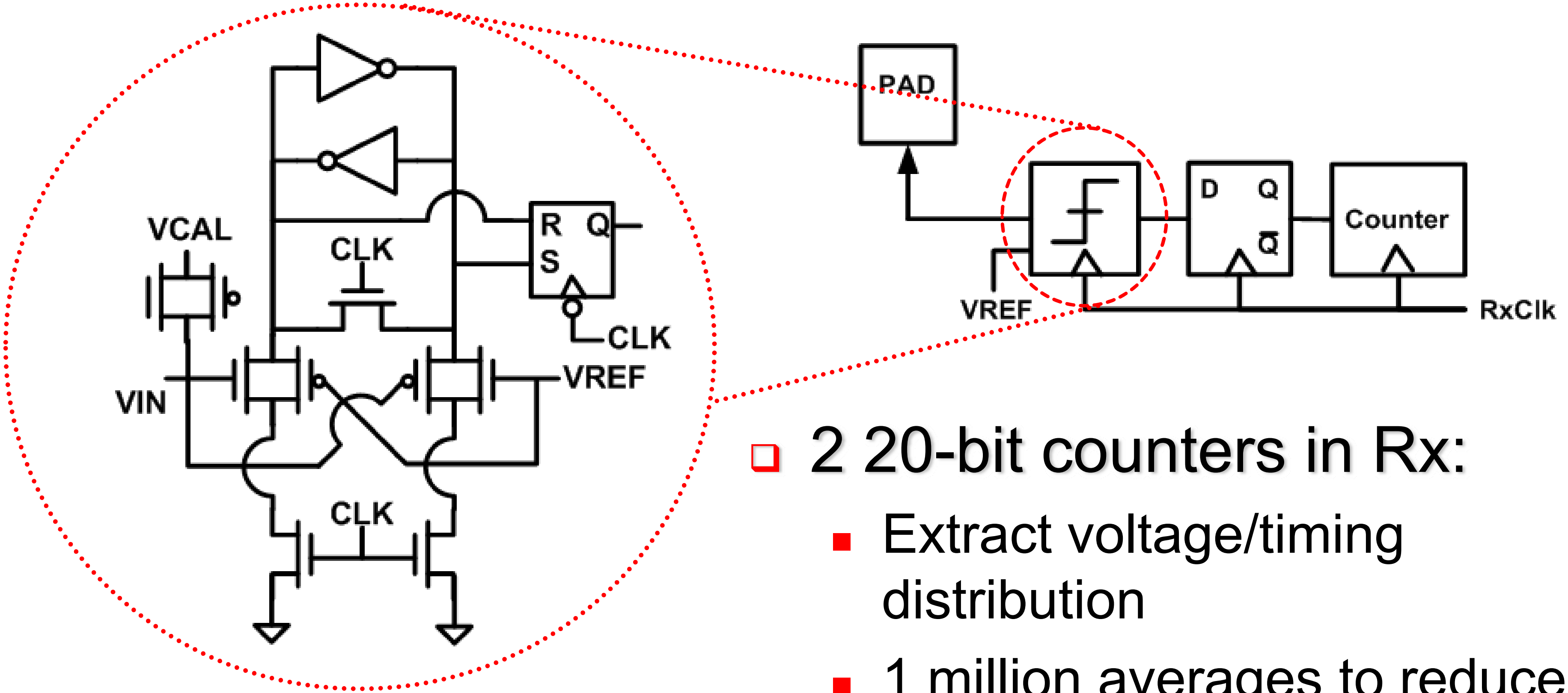
- $\Delta\Sigma$-DAC Current Filter:
  - Traditionally requires very large caps & inductors
- Add voltage filter in current mirror:
  - Enables lower corner frequency using smaller capacitors
  - 1MHz corner for C1, C2 & C3 ~ 340fF
  - Filter bandwidth dependent on bias current (g_m) – wider as for larger g_m





Receiver

- Adopted from [1] to function rail-to-rail
- Calibration port enables off-line offset calibration

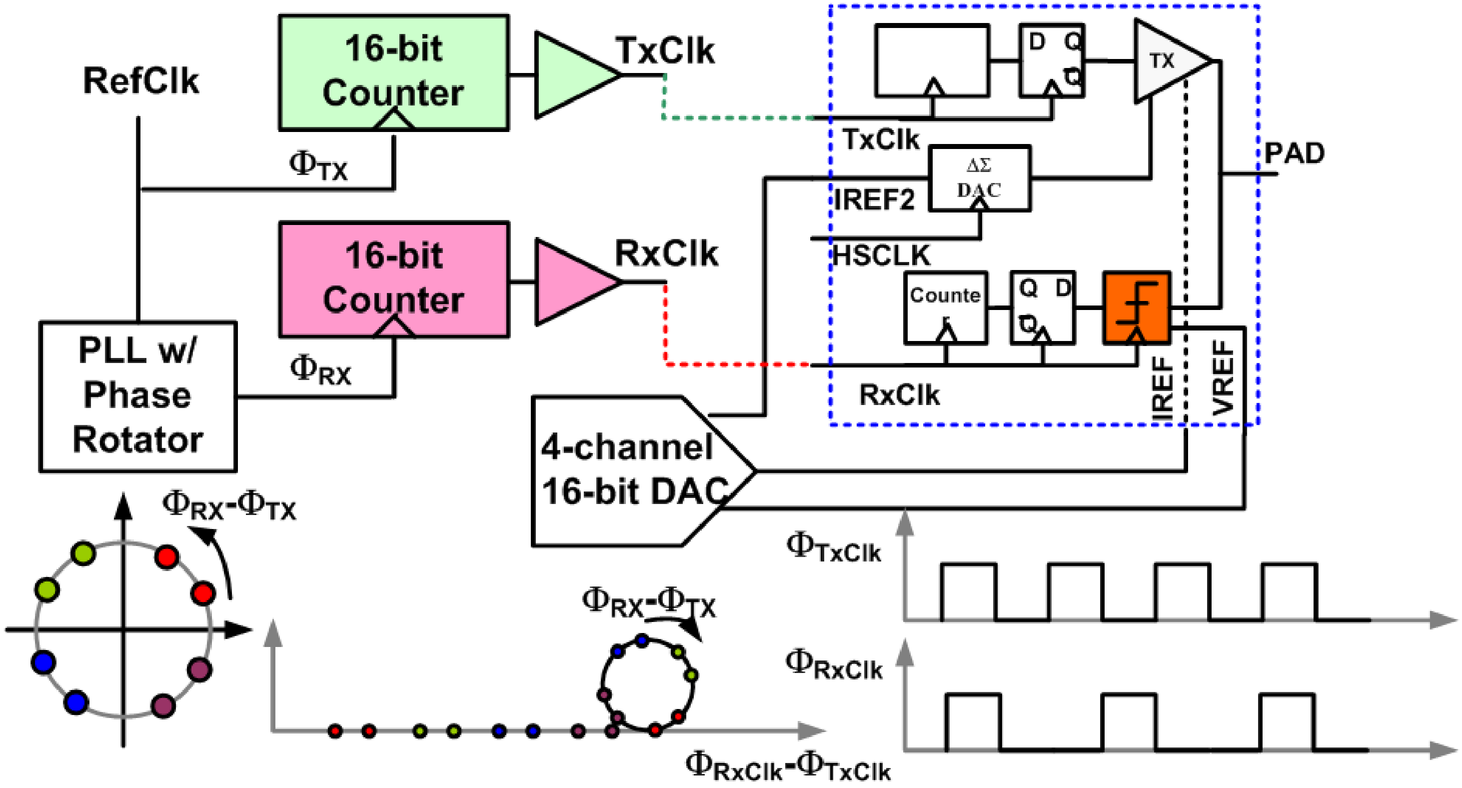


- 2 20-bit counters in Rx:
  - Extract voltage/timing distribution
  - 1 million averages to reduce noise by up to 60dB

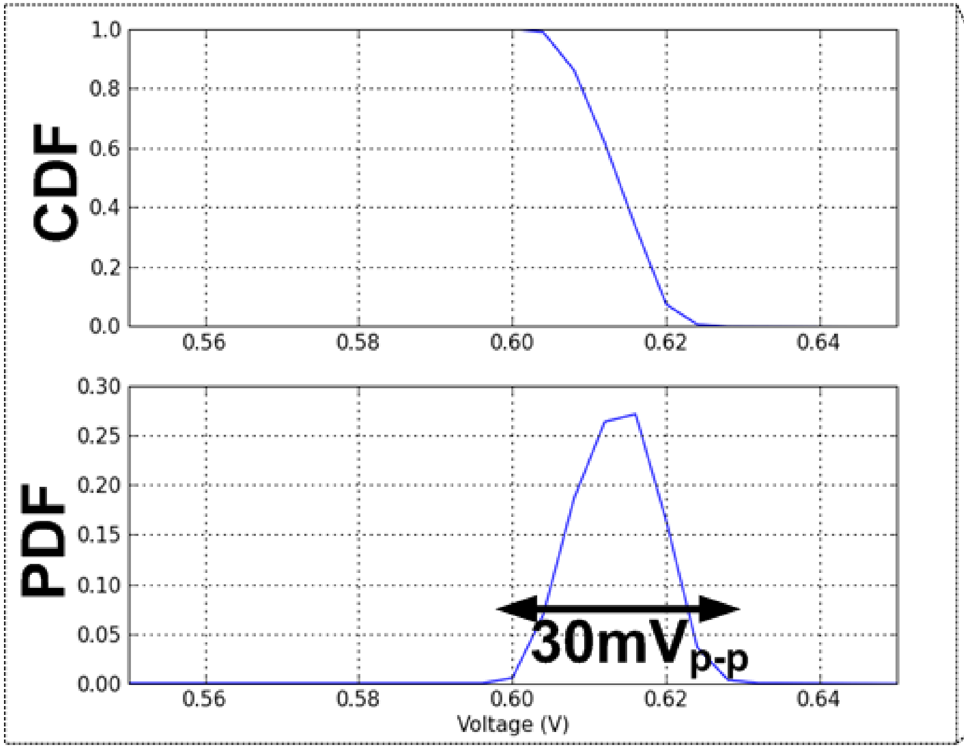
[1] M. Takamiya, Mizuno, M., *Symposium on VLSI Circuits*, 2004.

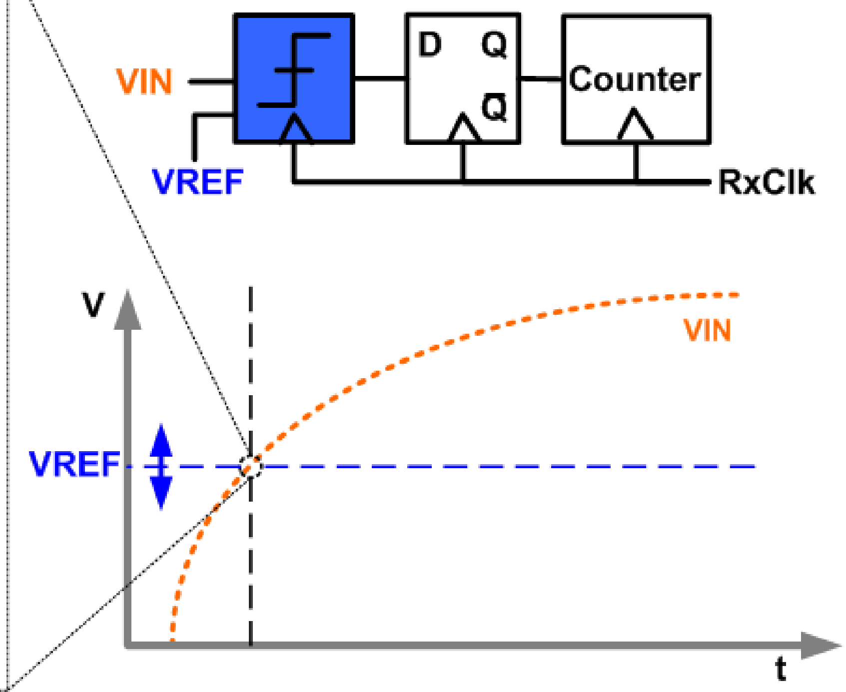
Timing Generation

- Need fine time resolution over a long period
  - PLL → fine resolution, short period
  - Divided clock → coarse resolution, long periods
- Feed fixed and rotating phases of PLL into dividers
  - Accumulate phase differences at the divider outputs



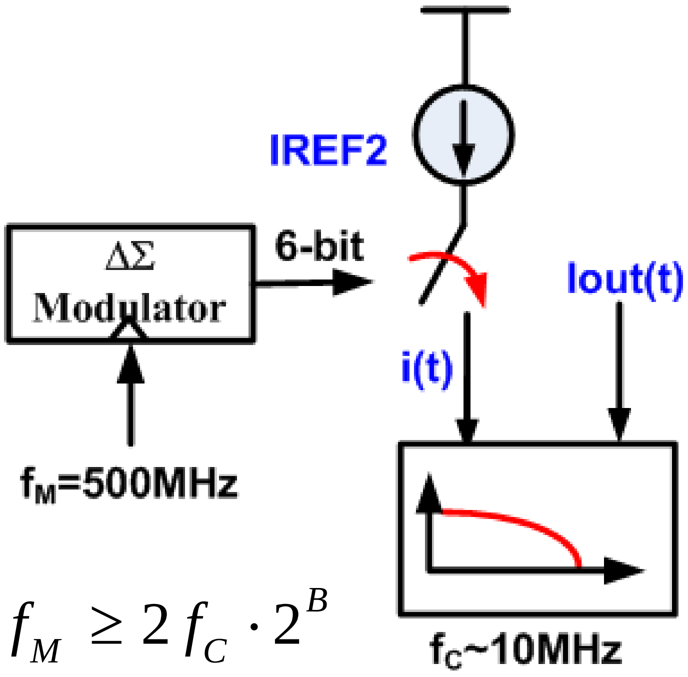
Measurement Noise



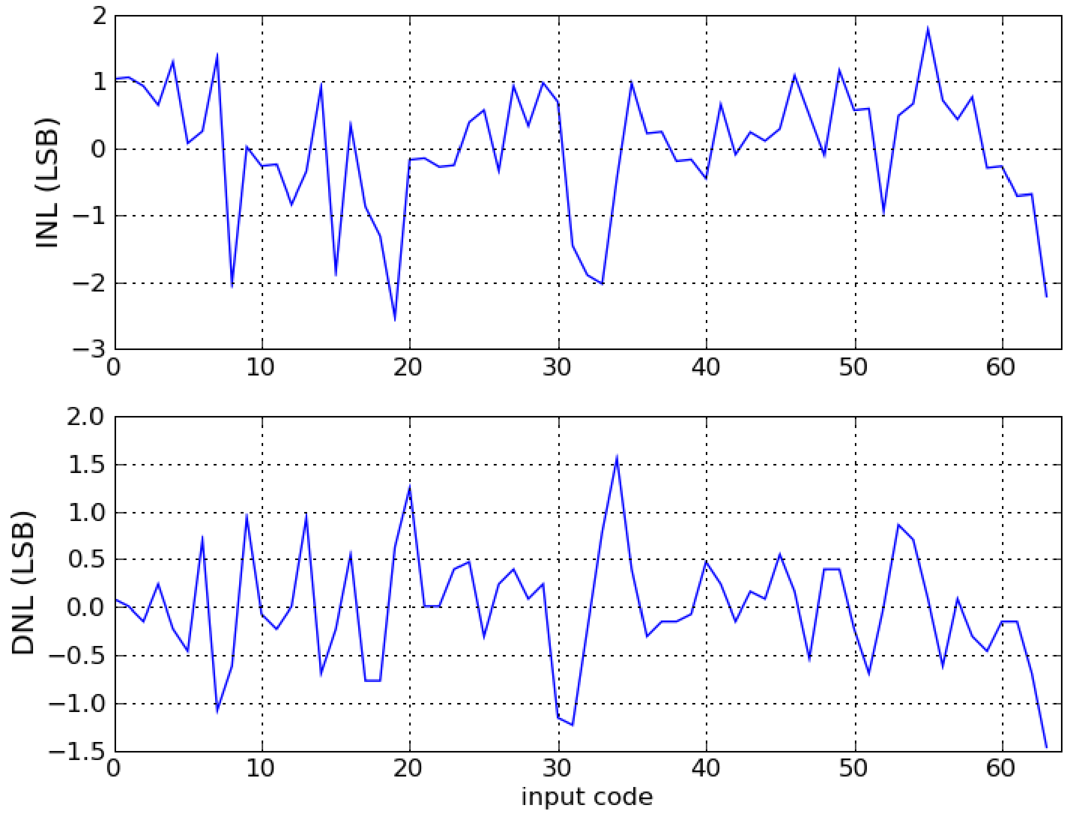


- For each slice in time, sweep voltage to get CDF
- Use PDF to acquire mean voltage
- 30mV$_{p-p}$ ~ 3σ →average down to σ ~10’s uV
- Resolution limited by external reference

Delta-Sigma DAC Linearity



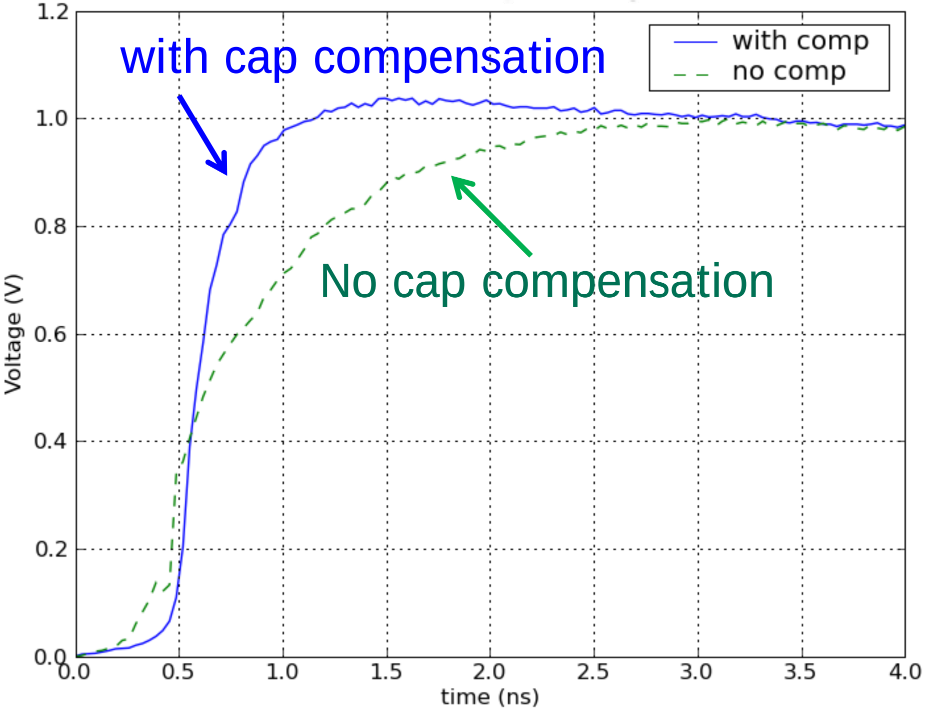
$$f_M \geq 2 f_C \cdot 2^B$$



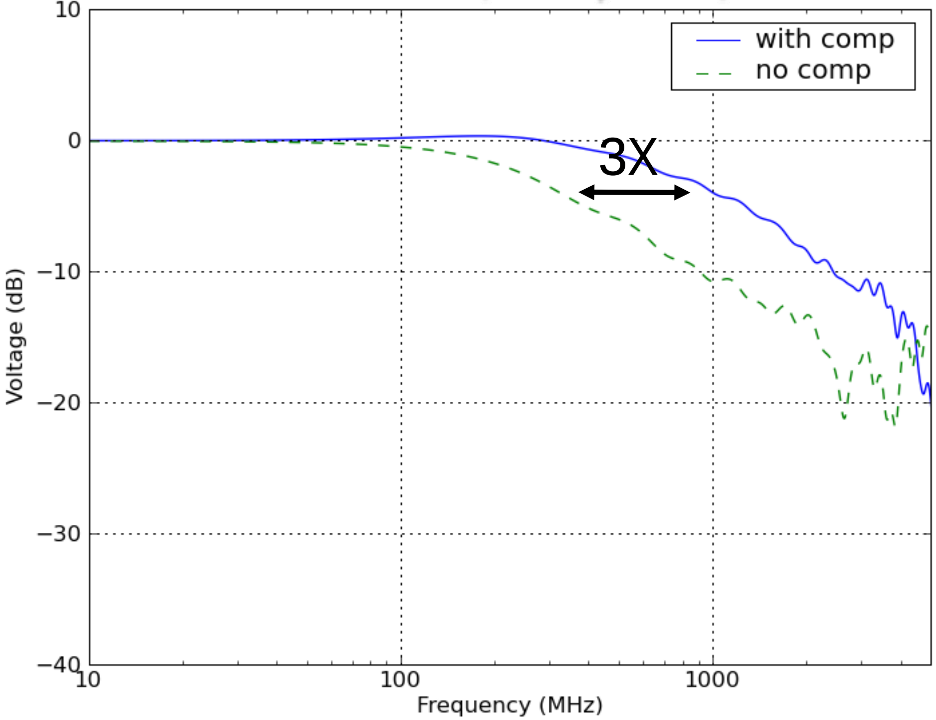
- LSB = 330nA
- ENOB = 4.6 bits @ f_M=500MHz
- Indicates ~ -35dB filter frequency of 10.3MHz

Pad Cap Compensation

Normalized Step Responses

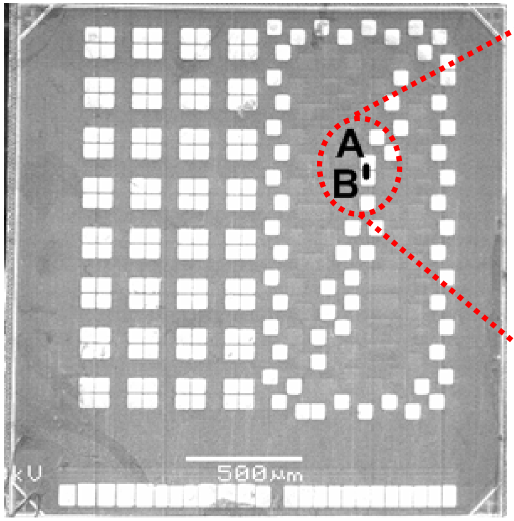


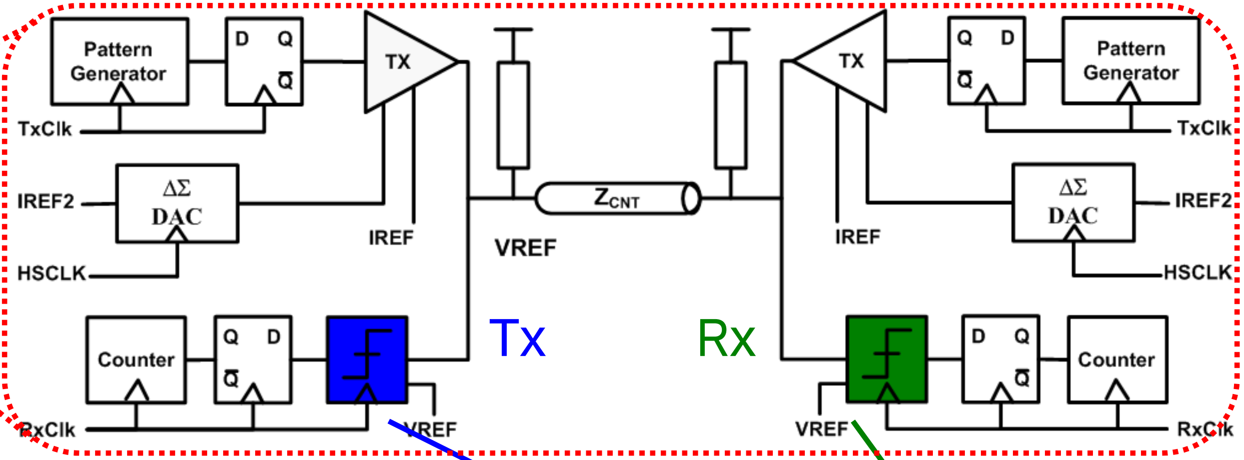
Normalized Frequency Responses

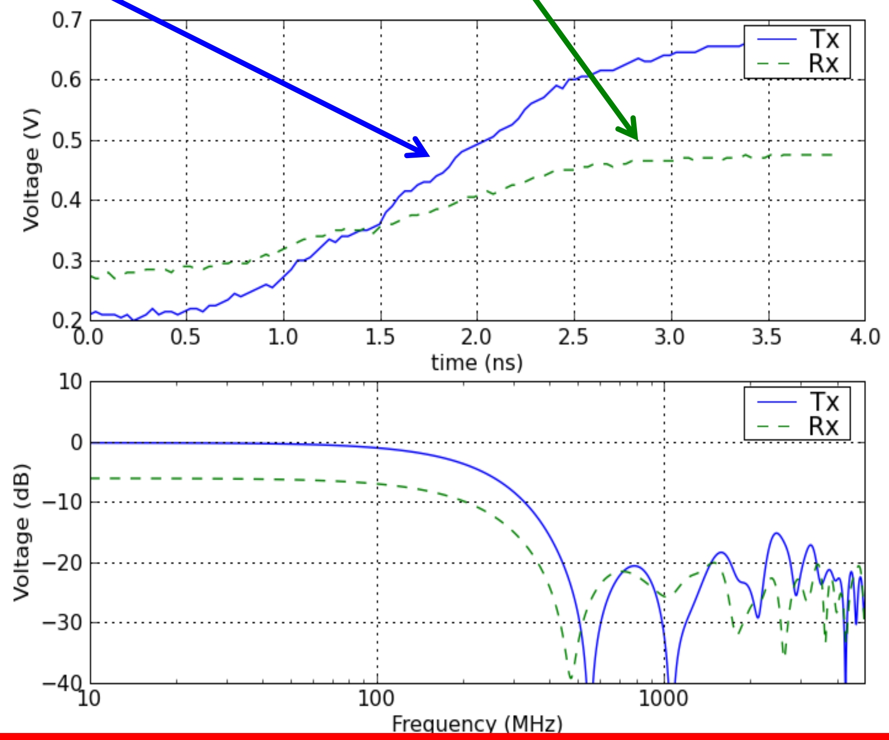


- Step responses at transmitter (7.5kΩ termination):
  - Bandwidth of step with compensation is ~ 3X larger than with no pad capacitance nulling
  - ~5fF of residual pad capacitance & 15fF of device capacitance

Carbon Nanotube Step Response







- Measured step response across a sheet of CNTs
  - 30-50μm each over a > 10μm span (A to B)
  - ~6dB loss at Rx
  - Connection automatically detected

Conclusions

- Silicon test infrastructure for emerging high-impedance devices:
  - Adjustable termination offers better power transfer
  - Interface parasitic can be better controlled
  - Flexible pad interface for faster detection and repeatable measurements
- Minimizing Interface Capacitance
  - Requires small devices → larger variation
  - Variation/error can be corrected with compact & efficient calibration circuitry