Dual Scalable 500 MS/s, 5b Time-Interleaved SAR ADCs for UWB Applications

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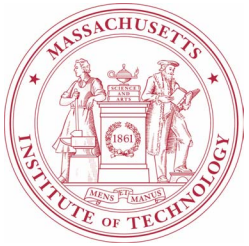


Outline

- Ultra-Wideband Radio
- ADC Architecture
- Circuit Implementation
- Measured Results
- Conclusion

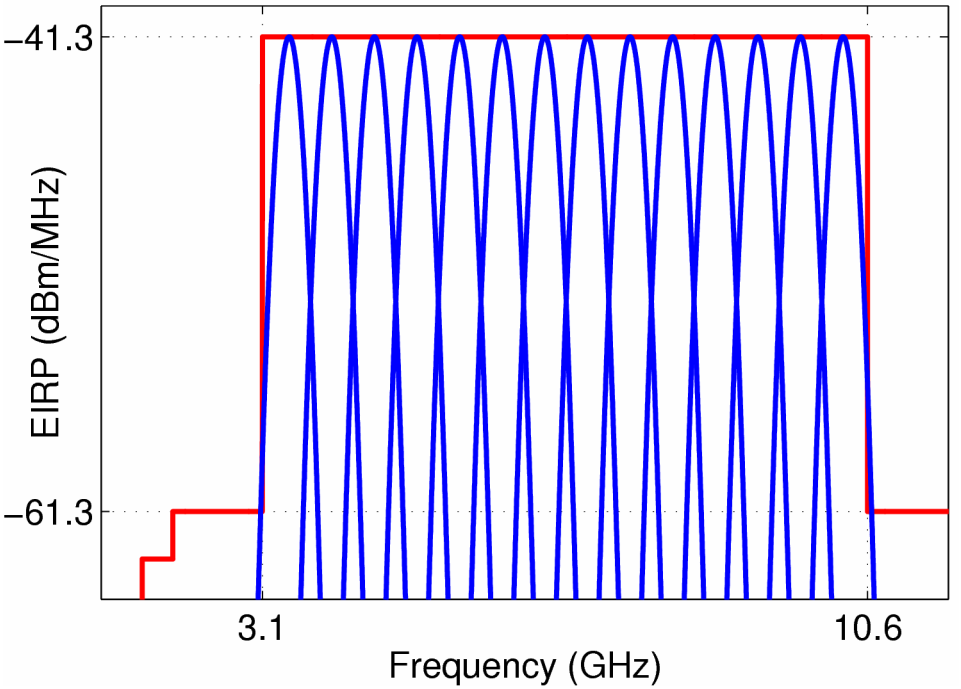
Ultra-Wideband Radio Overview

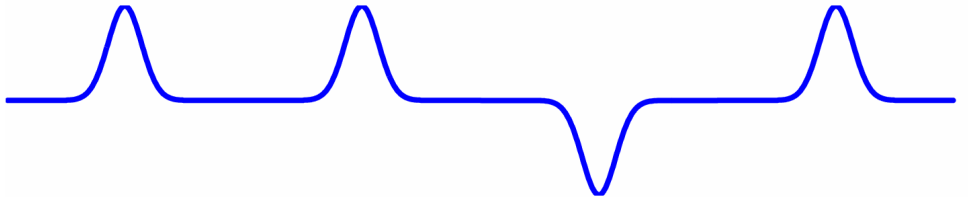
FCC Specifications

- >500MHz 10dB bandwidth
- Very low average power density (see mask at right)

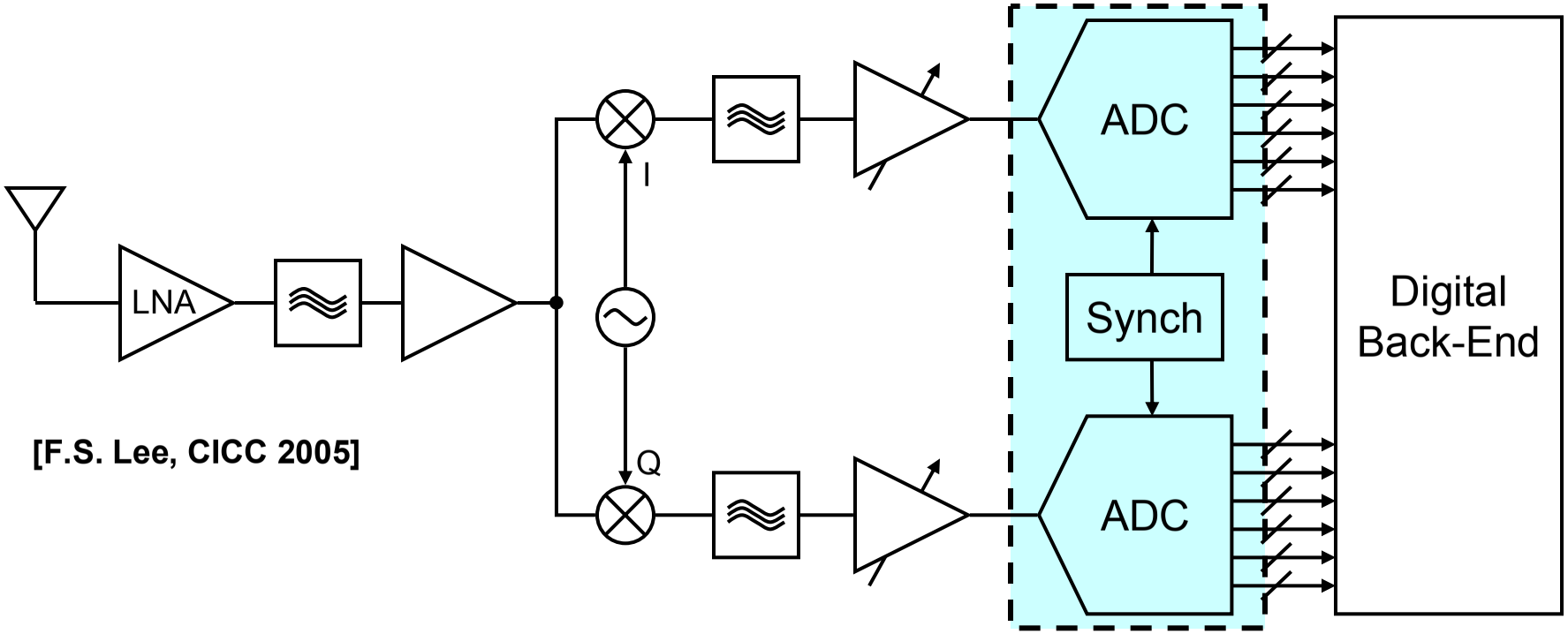
- IEEE 802.15.3a is developing a high data rate (≥480Mb/s) UWB for PAN.
- Both OFDM and pulse-based solutions are proposed.

FCC Spectrum Mask and 14-Channel Frequency Plan





UWB Receiver Design

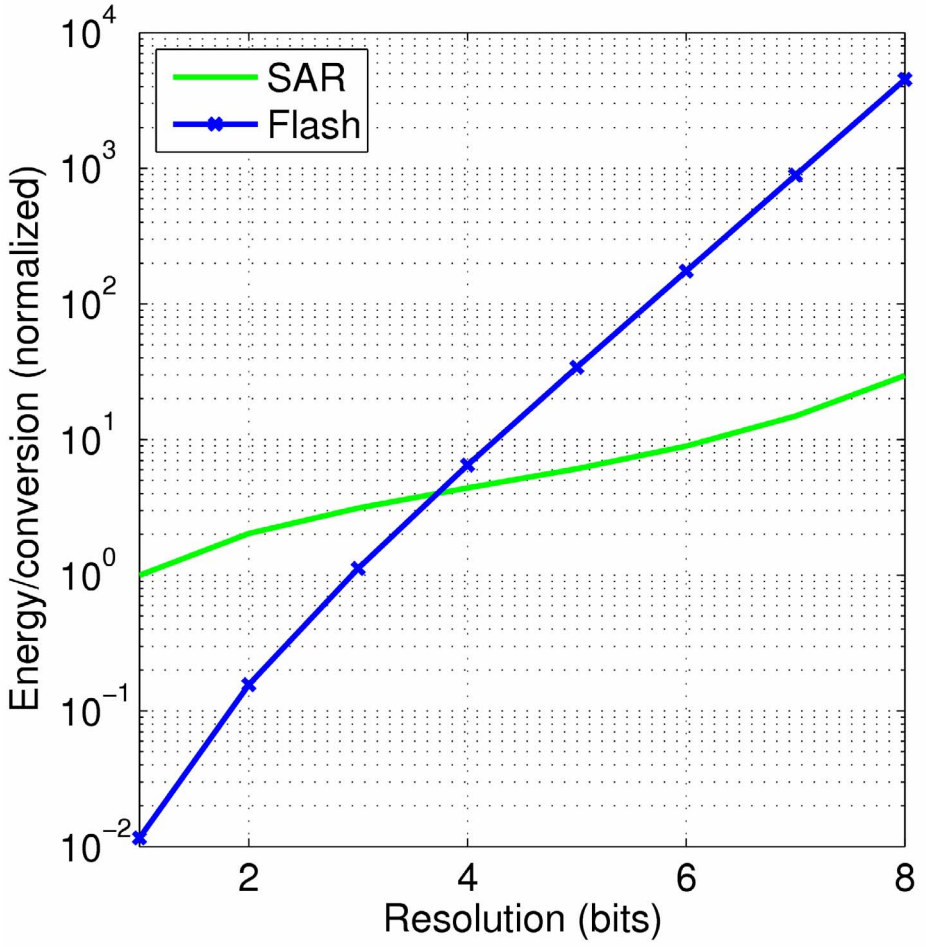


[F.S. Lee, CICC 2005]

- 500MS/s for Nyquist sampling of minimum bandwidth RF signals
- 5 bit resolution sufficient for proper reception; fewer bits possible under favorable channel conditions
- Goal: minimize power dissipation
- Parallel interface to relax I/O requirements and provide parallel data to back-end

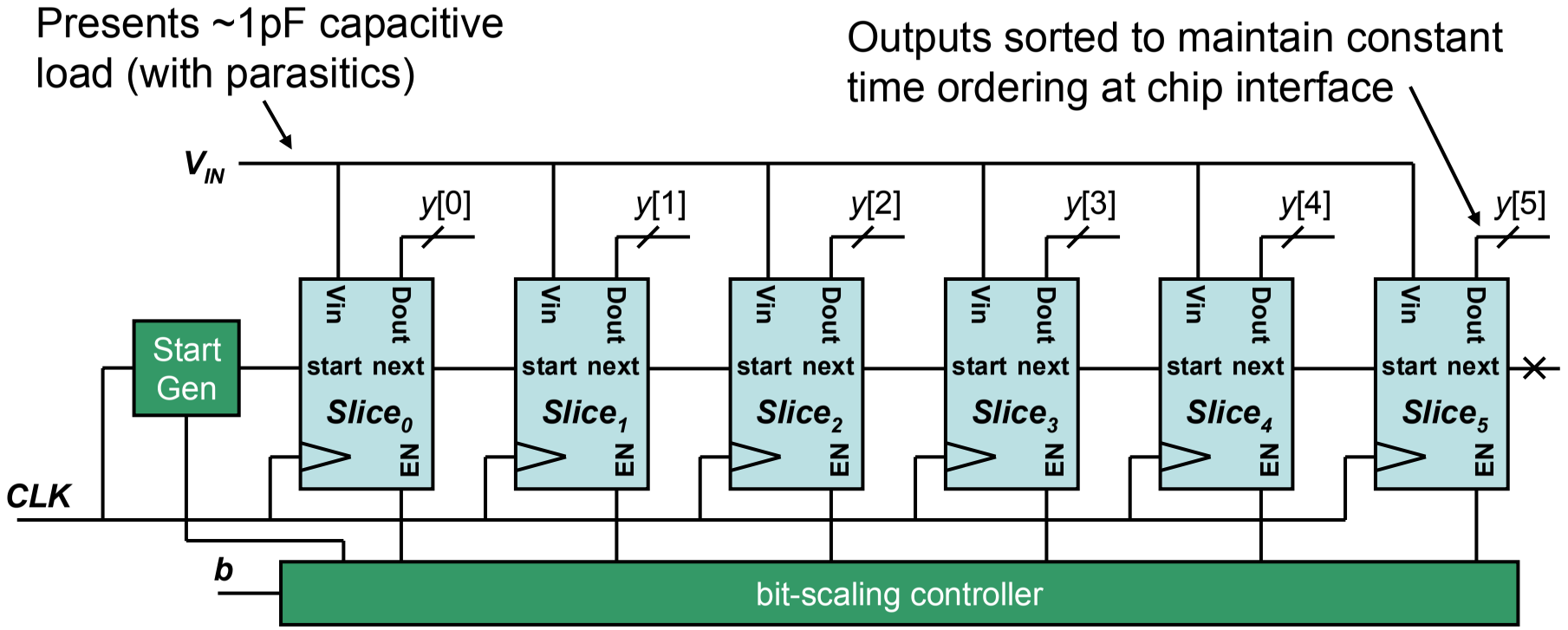
ADC Architecture Selection

- Flash most common but require 2^b-1 comparisons per sample
- [Draxelmayr, ISSCC 2004] 6b, 600MS/s time-interleaved successive approximation register (SAR)
- SAR characteristics:
  - b comparisons
  - Comparators have same speed/accuracy requirements as flash
  - 6 periods to resolve output
  - Digital and capacitor array switching overhead



SAR energy dominated by digital logic at low resolutions and comparators at medium resolution

Time-Interleaved SAR ADC



- Single 500MHz clock from on-chip VCO or external source
- 6 periods per conversion at nominal resolution
- Start signals shared between I and Q ADCs for synchronization

Bit Scaling

- S = sample
- BC = bit-cycle
- Off = Gate ***START*** and ***CLK*** signals, power down preamplifiers
- Scalable down to 1 bit

5 bits

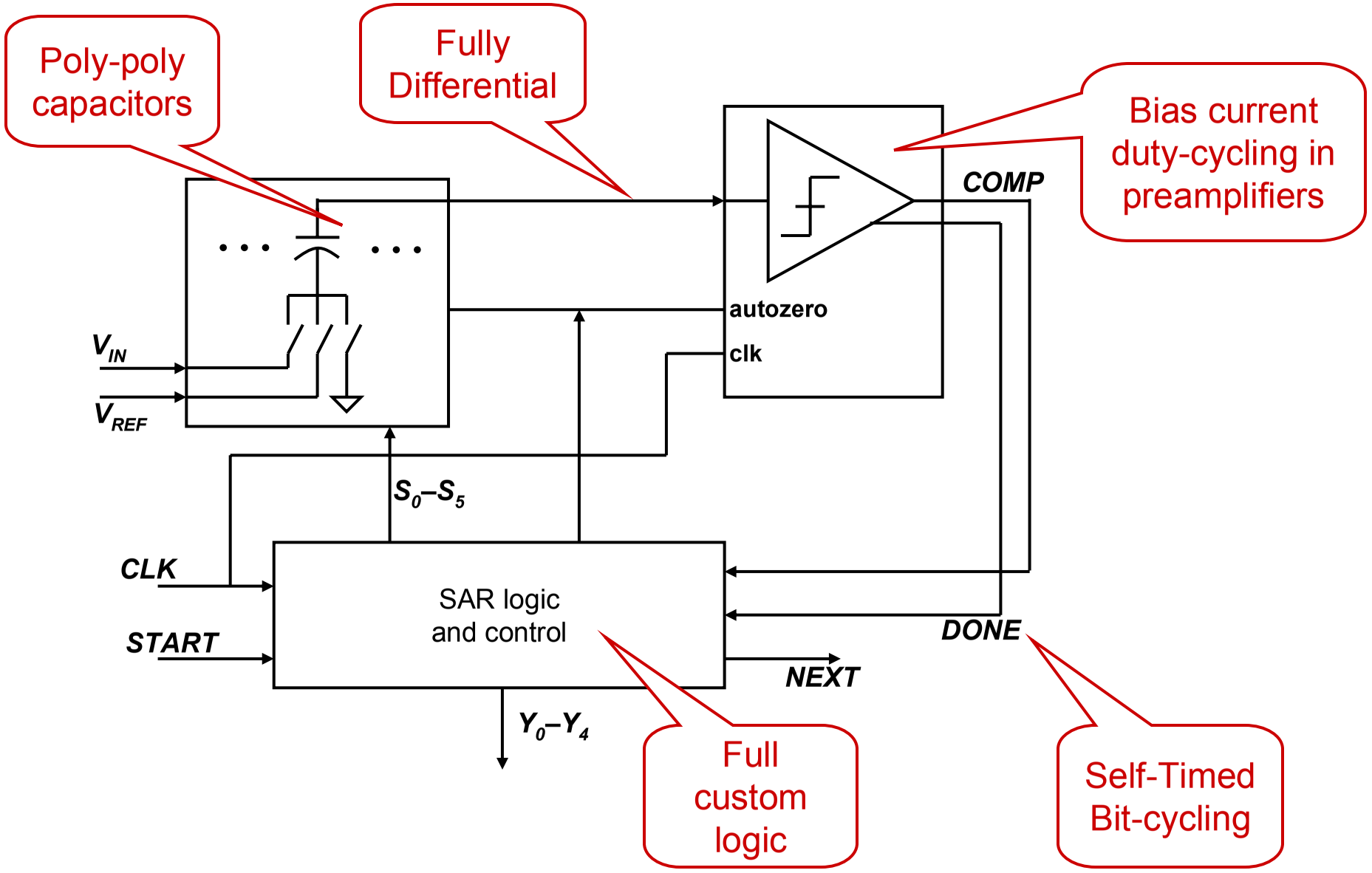
Time Per.	SL_0	SL_1	SL_2	SL_3	SL_4	SL_5
1	S	BC 5	BC 4	BC 3	BC 2	BC 1
2	BC 1	S	BC 5	BC 4	BC 3	BC 2
3	BC 2	BC 1	S	BC 5	BC 4	BC 3
4	BC 3	BC 2	BC 1	S	BC 5	BC 4
5	BC 4	BC 3	BC 2	BC 1	S	BC 5
6	BC 5	BC 4	BC 3	BC 2	BC 1	S

3 bits

Time Per.	SL_0	SL_1	SL_2	SL_3	SL_4	SL_5
1	S	BC 3	BC 2	BC 1	Off	Off
2	BC 1	S	BC 3	BC 2	Off	Off
3	BC 2	BC 1	S	BC 3	Off	Off
4	BC 3	BC 2	BC 1	S	Off	Off

Generating the ***START*** signal for the first slice of each ADC faster automatically resets bit-cycling and latches outputs at the appropriate time.

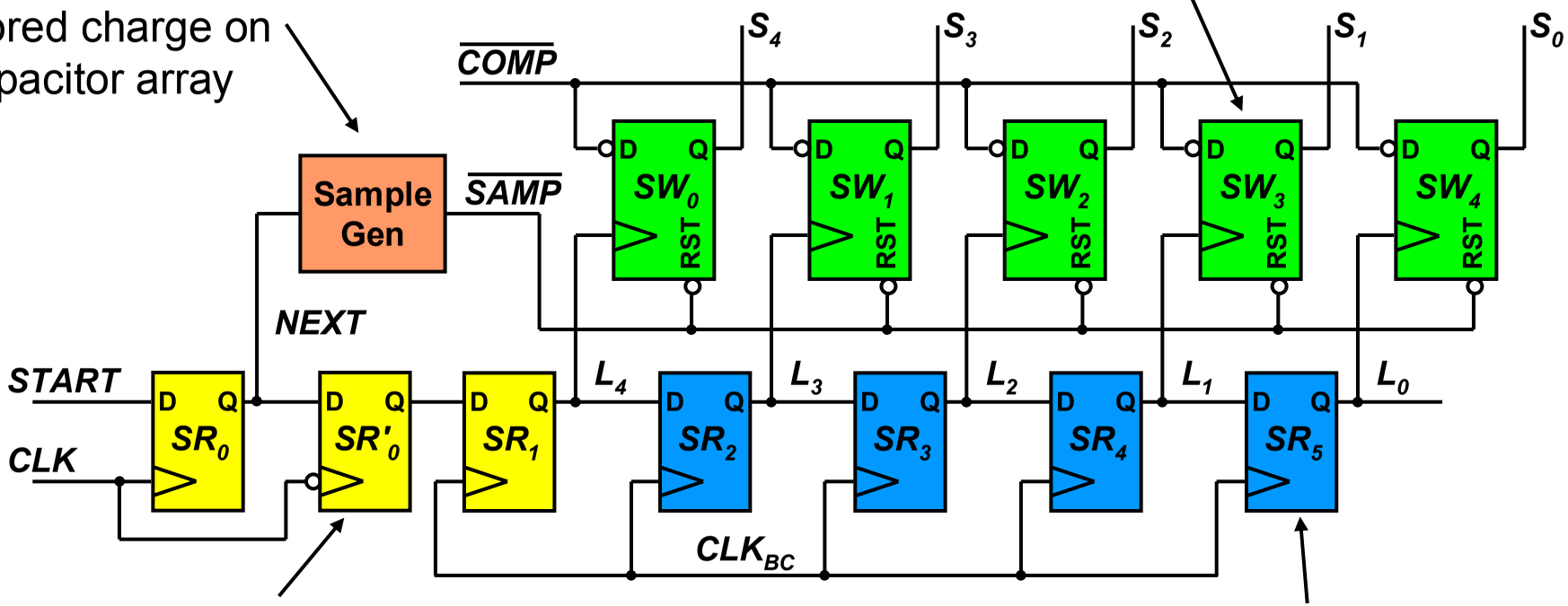
Slice Implementation



SAR Logic and Control

Generates sample and autozeroing signals to minimize corruption of stored charge on capacitor array

Switch drive register is single gate implementing complex logic function to drive capacitor array (S_0-S_4)

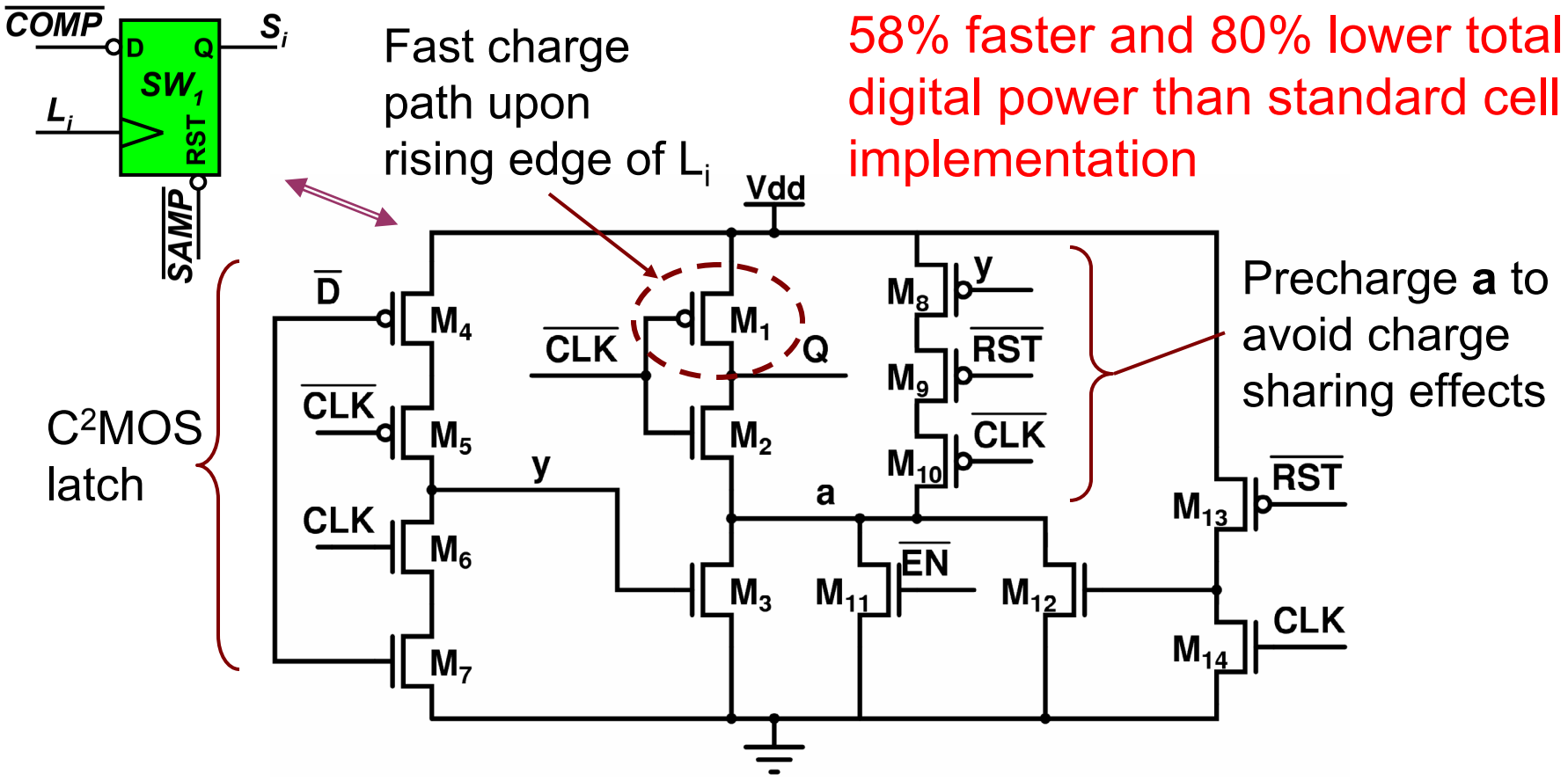


Standard C²MOS registers with enable

C²MOS registers with enable and synchronous reset

Propagation delay is $2 \cdot t_{ck\text{-}q}$ from rising edge of CLK_{BC}

Custom Switch Drive Register

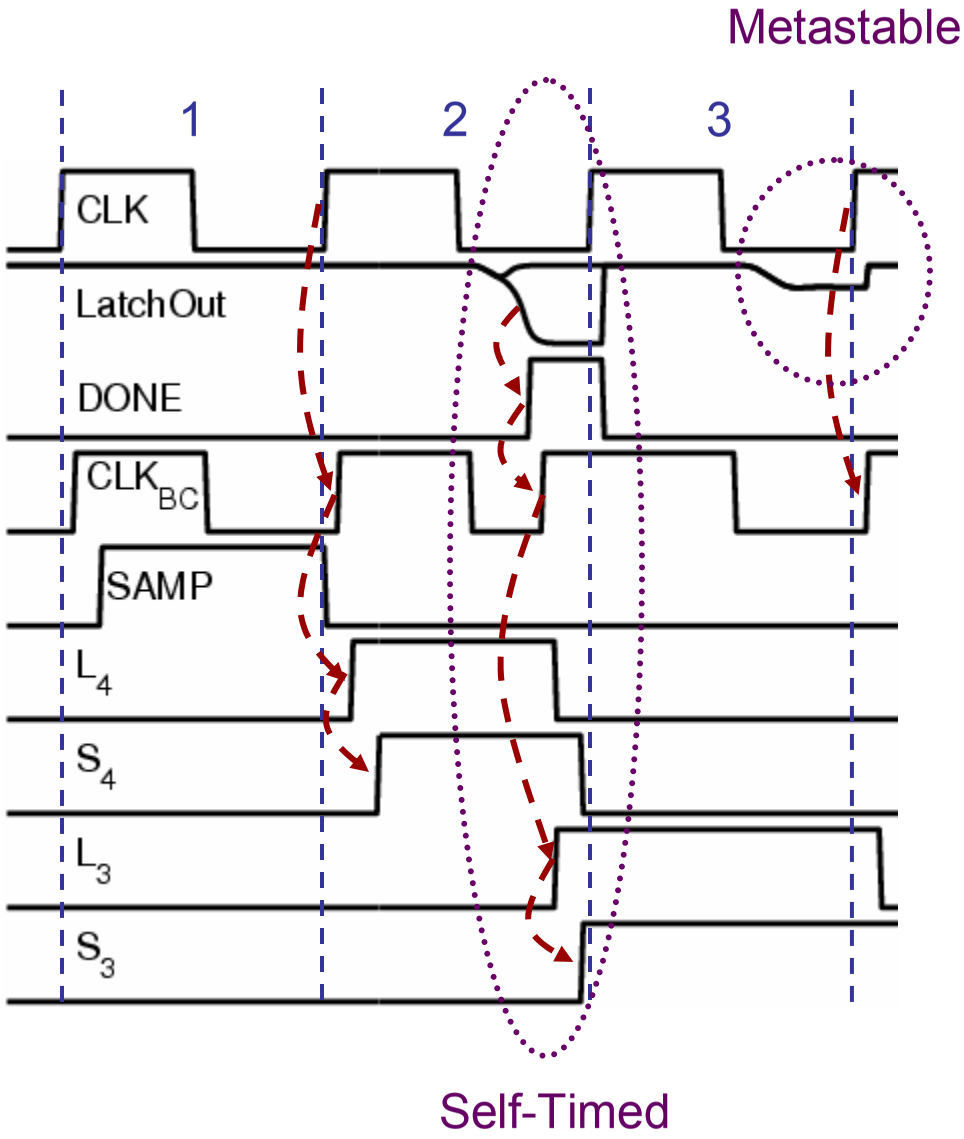


Deterministic nature of SAR algorithm allows simplified gate designs because not all input signal combinations are possible.

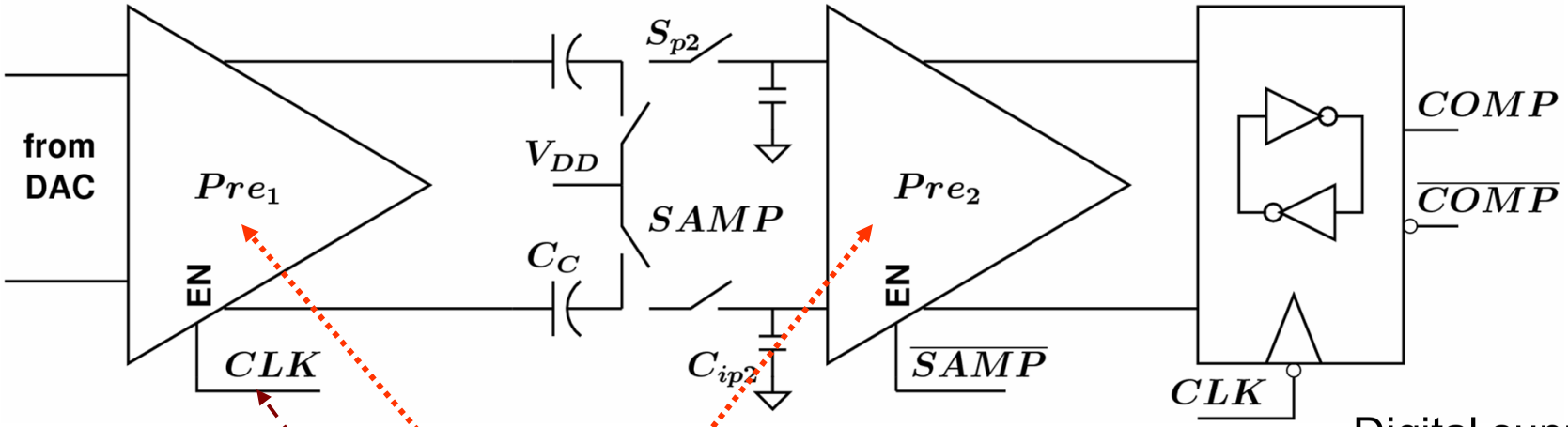
Time-Borrowing

- Digital feedback between each bit-cycle
- Use self-timed bit-cycling [Promitzer, JSSC 2001]
- Extends period for analog settling → reduced bias currents
- Deterministic nature of SAR signals forces a large input (fast settling time) to follow a small one (chance of metastability)

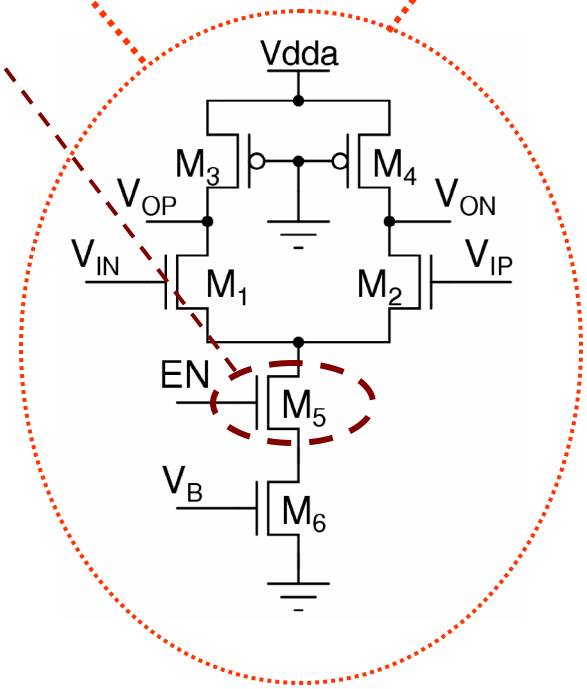
- Joint design of the timing between analog and digital sections.



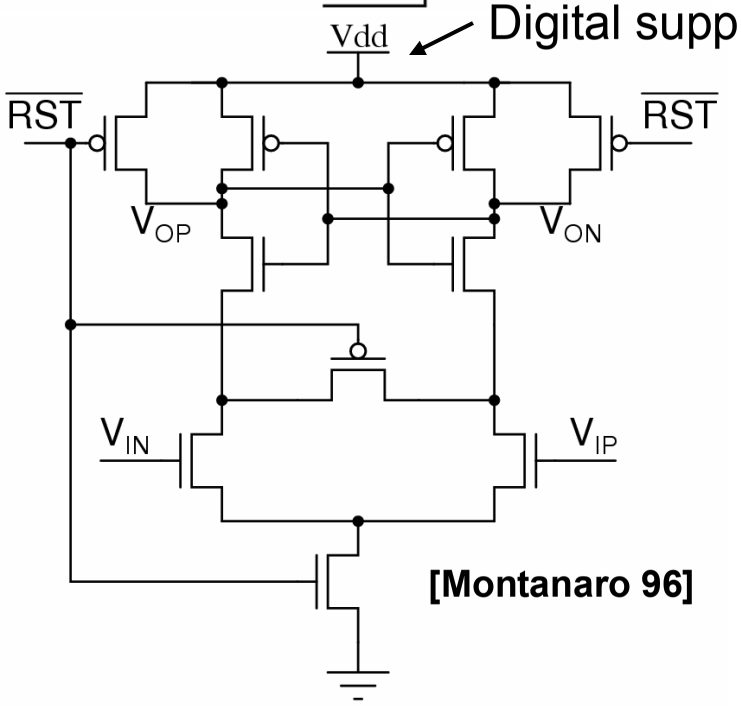
Comparator Design and Schematics



Preamplifiers only on when actively needed



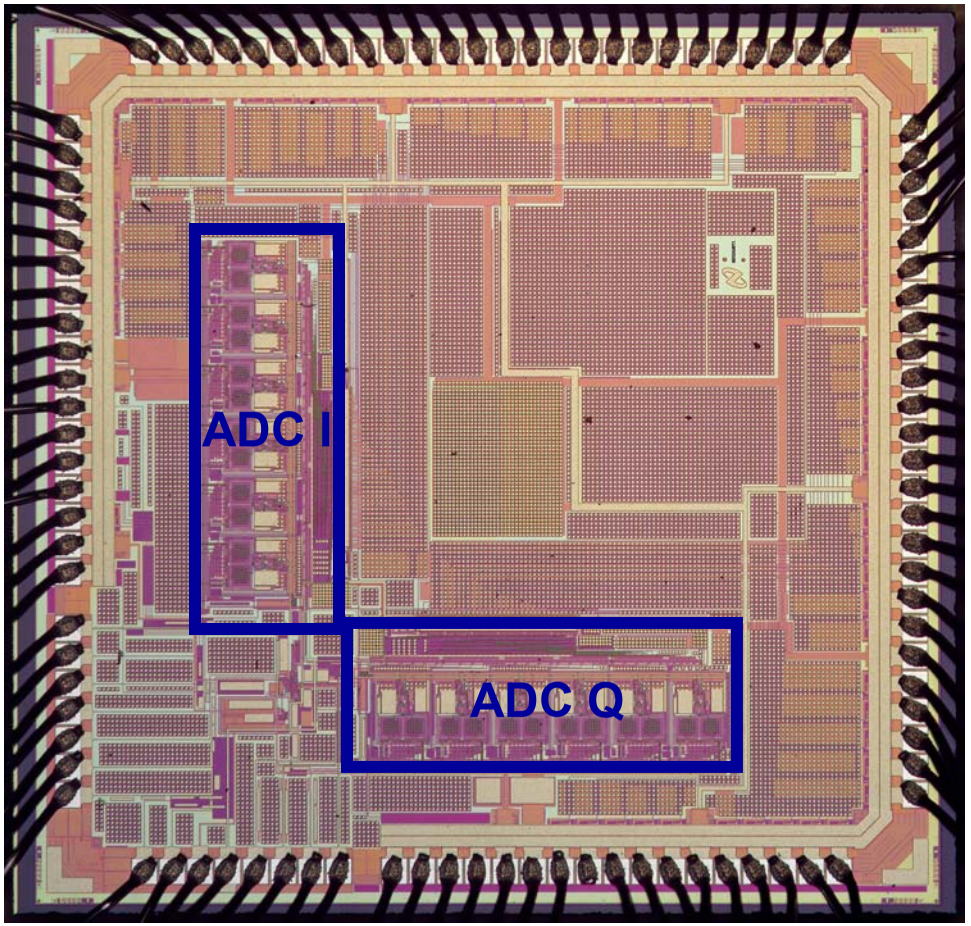
Simple structure allows high speed operation with low voltage (1–1.2V)



[Montanaro 96]

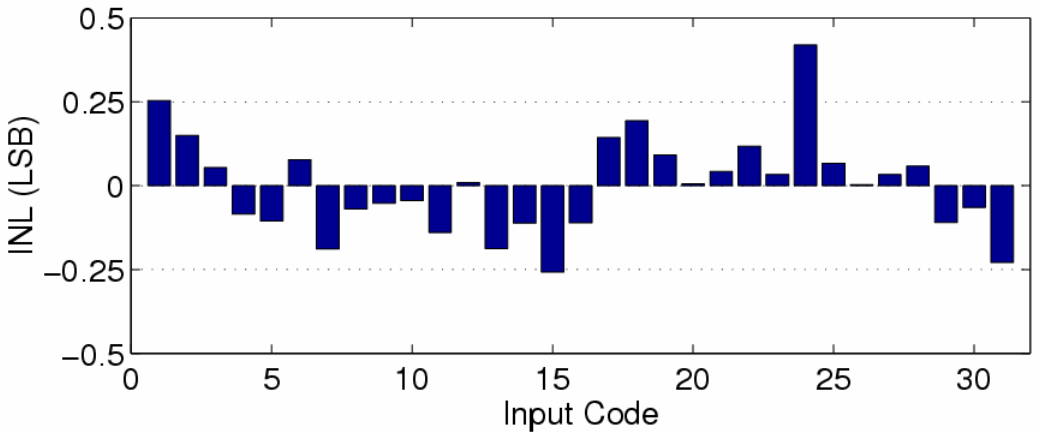
Die Photo

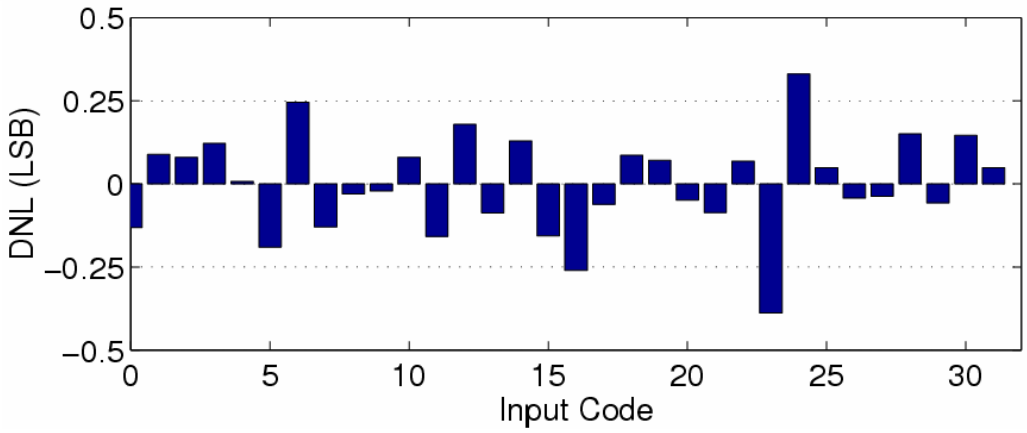
- National Semiconductor 0.18µm CMOS process
- Total area: 2.3mm x 2.4mm
- Active area per ADC: 0.5mm x 1mm
- Chip also includes reference voltage buffer, VCO, and external clock chain.



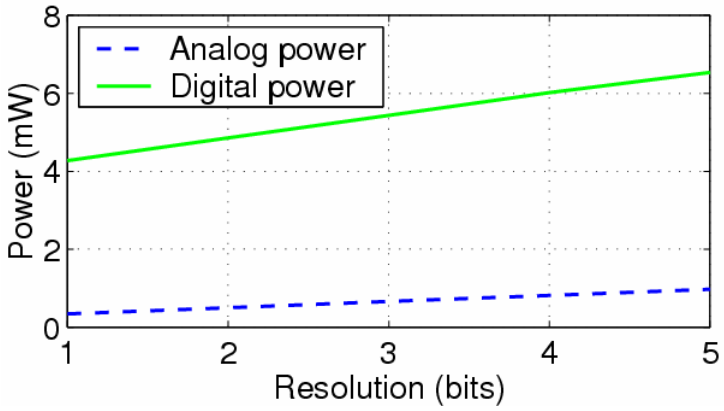
Static Performance

500 MSample/s operation





Typical results



Analog V_{DD}: 1.2V nominal

Digital V_{DD}: 1.8V nominal

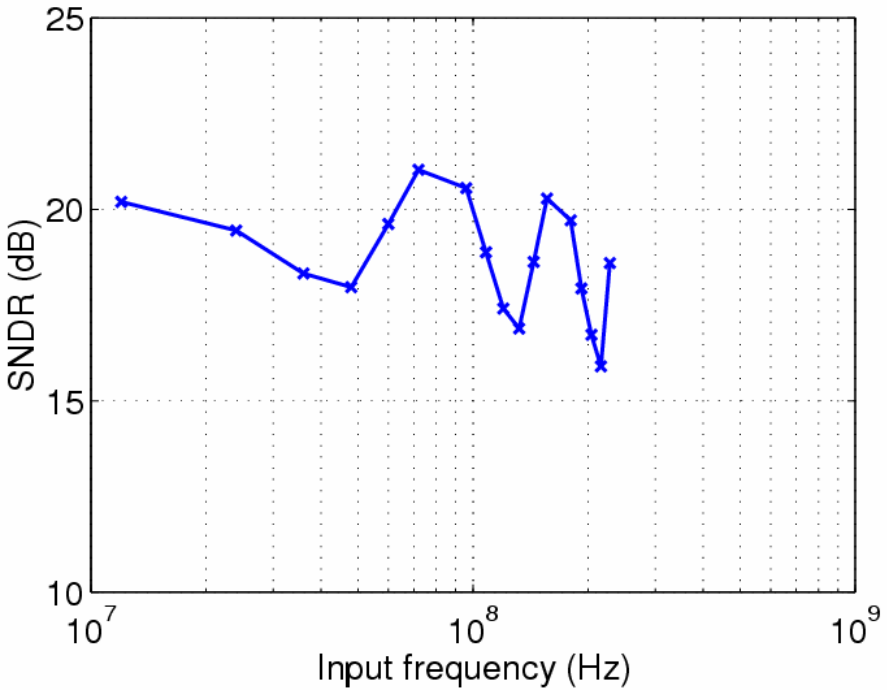
7.8mW max power per ADC, excluding I/O

Full scale input: 200-400mV single-ended

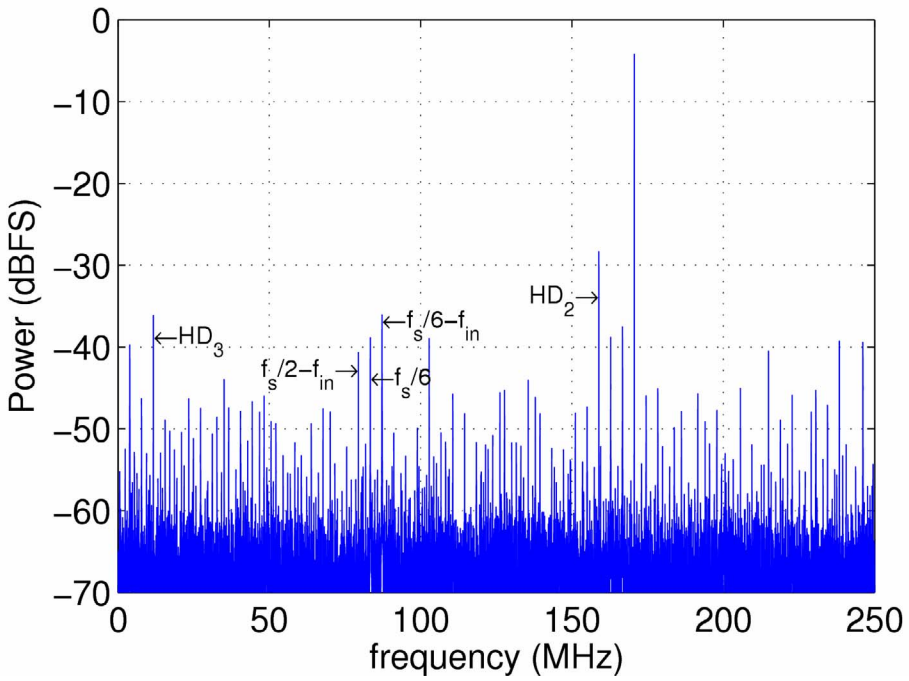
Duty cycling reduces analog power by 15%

Dynamic Performance

Signal-to-noise-plus-distortion ratio

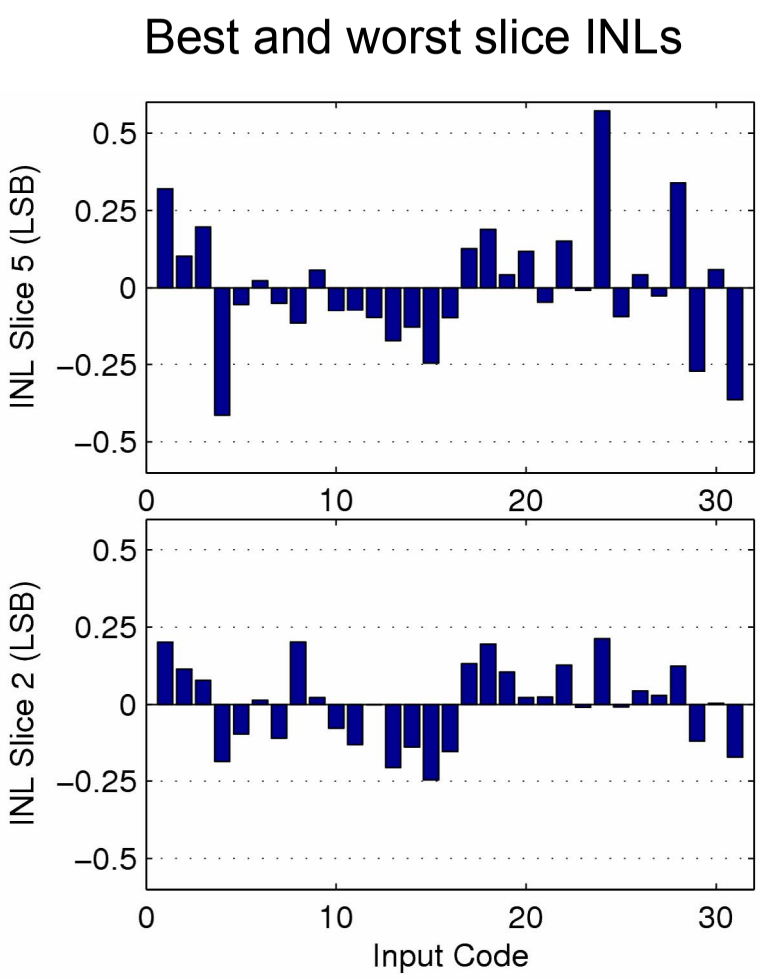


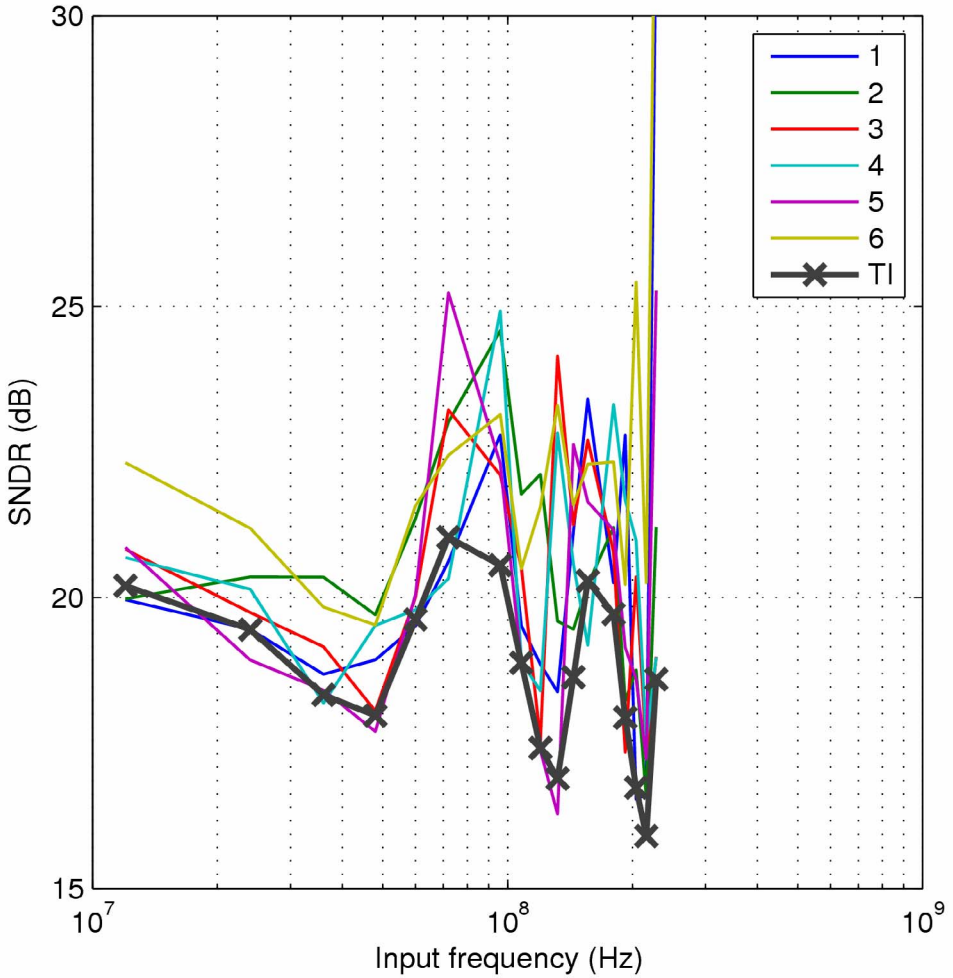
FFT of 170.56MHz input sampled at 500MHz



- Periodic behavior ↔ Insufficient time for sampling
- Dynamic tests use external, low jitter clock
- Offset and timing mismatch between slices not limitation of performance

Time Interleaving Performance





Static performance testing averages uncorrelated errors; dynamic performance is dominated by worst case slice.

Conclusions

- Parallelism enables greater architectural flexibility.
- SAR architecture not limited to only low speed converters.
- Self-timing, a technique well known in digital, can also ease critical path constraints and power in analog.
- Digital power and complexity cannot be ignored in high-speed mixed signal circuits.

Acknowledgments

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