The Mixed Signal Optimum Energy Point: Voltage and Parallelism

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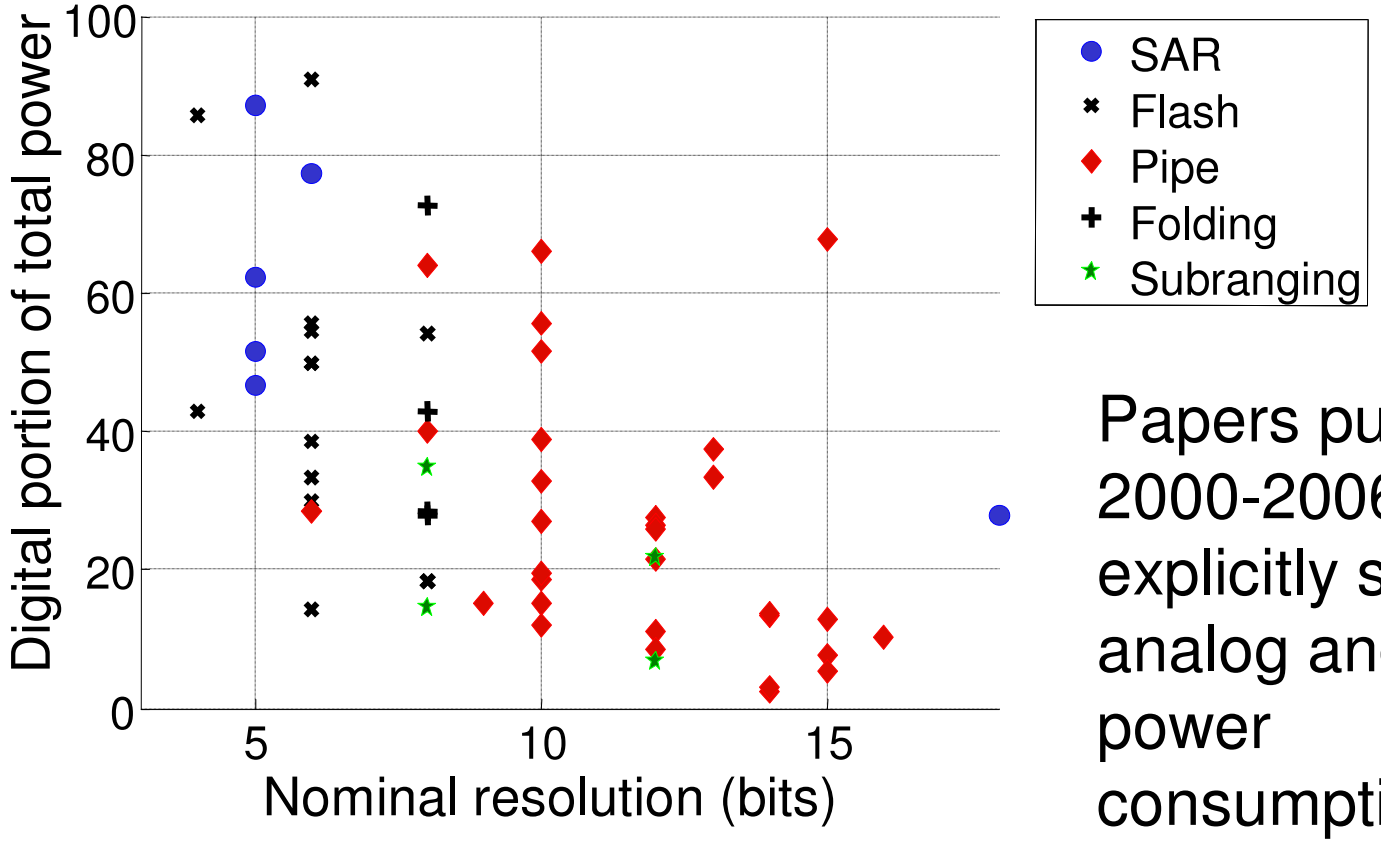
Digital Power in ADCs



Papers published 2000-2006 that explicitly separate analog and digital power consumptions.

Digital cannot be ignored; a comprehensive approach is required to fully optimize ADC performance.

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- Block Descriptions
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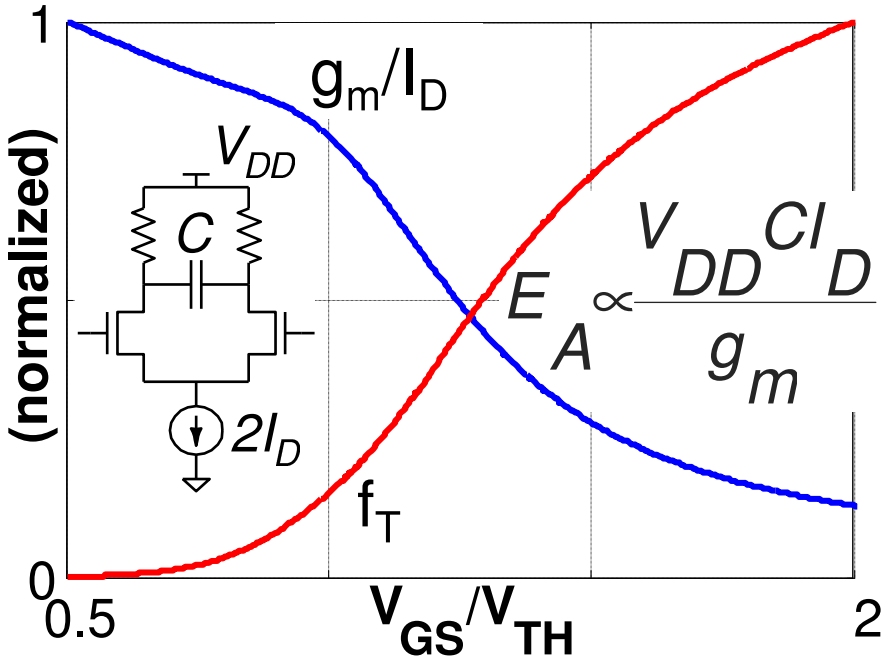
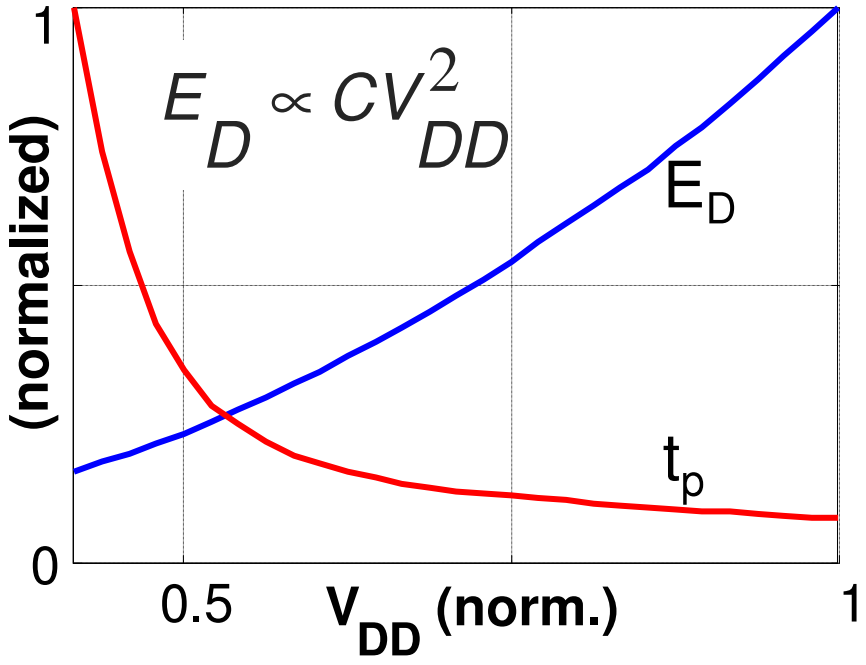
Energy and Parallelism

Slower ADCs are more energy efficient

- Analog circuits biased in sub-threshold
- Reduced digital supply voltages





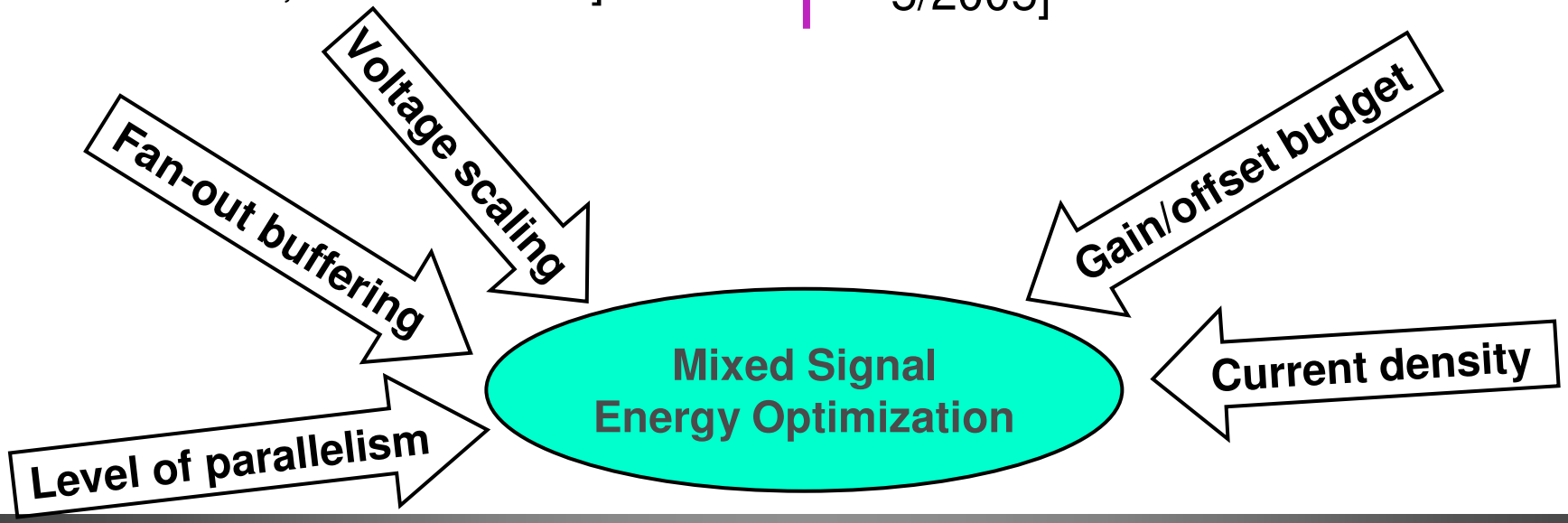
Mixed Signal Energy Optimization

Digital Optimization

- Minimum energy point balances switching and leakage energy. [A. Wang, ISVLSI 2003]
- Sensitivity analysis for sizing, supply voltages, and architectural tradeoffs. [D. Markovic, JSSC 8/2004]

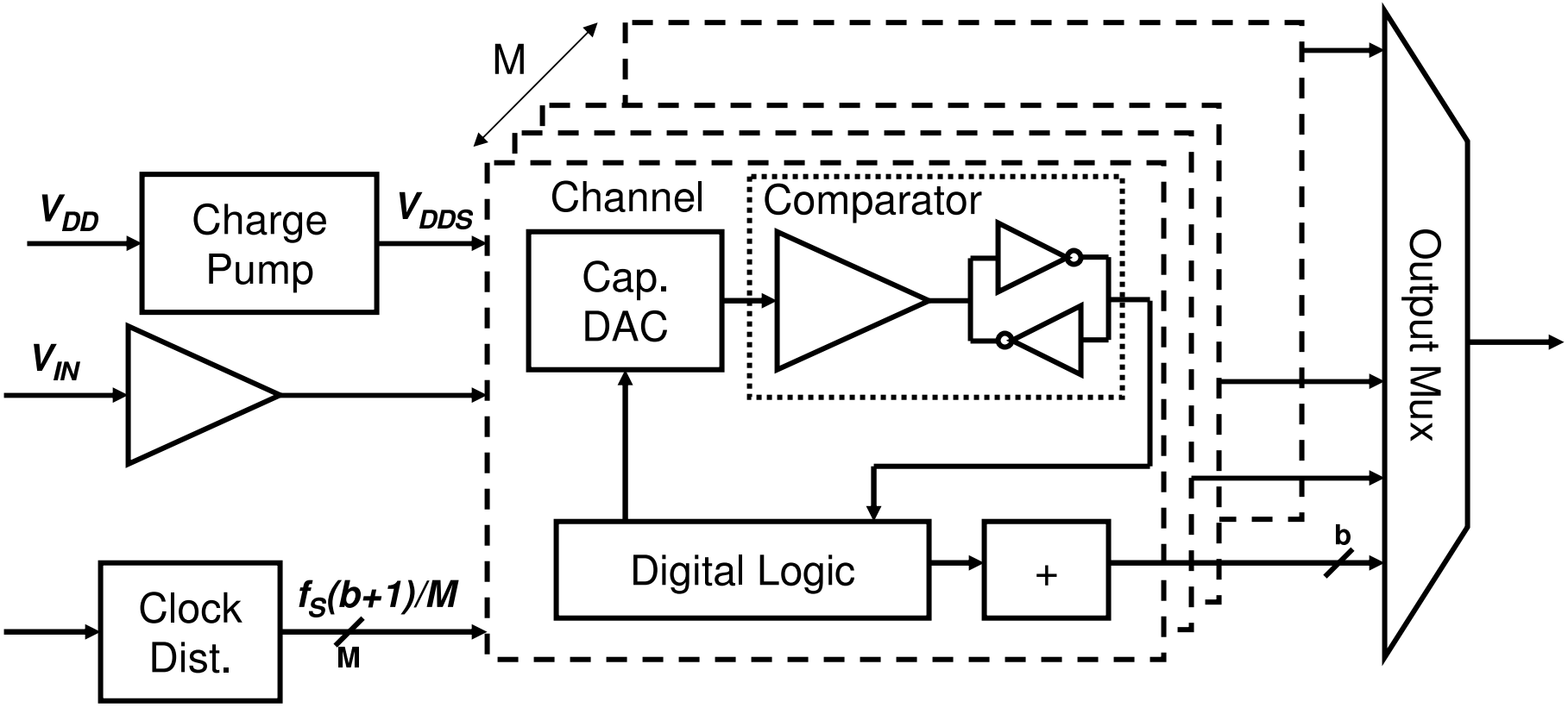
Analog Optimization

- Geometric programming for convex optimization of pipeline ADCs [M. del Mar Hershenson, ICCAD 2002]
- Parallelism moves bias points into weak inversion for energy savings [M. Spaeth, MIT CICS 5/2005]



Case Study: SAR ADC

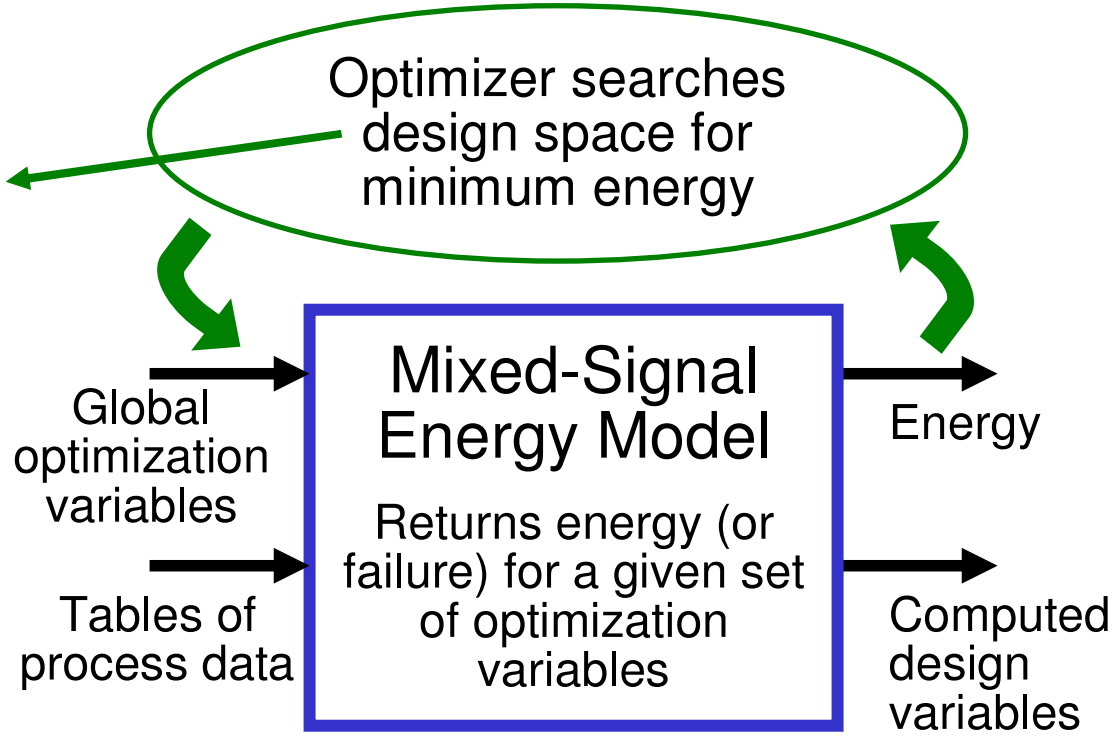
- Parallel successive approximation register (SAR) ADC is the test circuit for this optimization
- SAR ADC has comparable analog/digital complexity
- Careful modeling of channel performance and interleaving overheads is required



Methodology: Top-Level

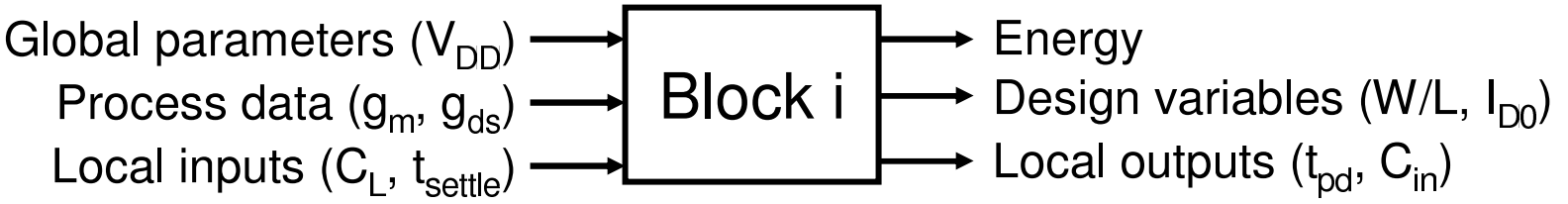
- Main model goals
  - Encapsulate the key interactions and tradeoffs between analog and digital to find true mixed-signal optimum
  - Ease of equation setup and close correspondence with design
  - Process independence and architecture modularity
- As solution speed is not critical, a discrete optimization is used

b	Resolution	5 bits
f_S	Sampling frequency	500 MHz
M	# channels	≥ 1
V_{DD}	Core supply voltage	0.5 to 1.2 V
V_{FS}	Full scale input	0.1 V to V_{DD}
V_{DDS}	Sampling voltage	V_{DD} to 1.2 V



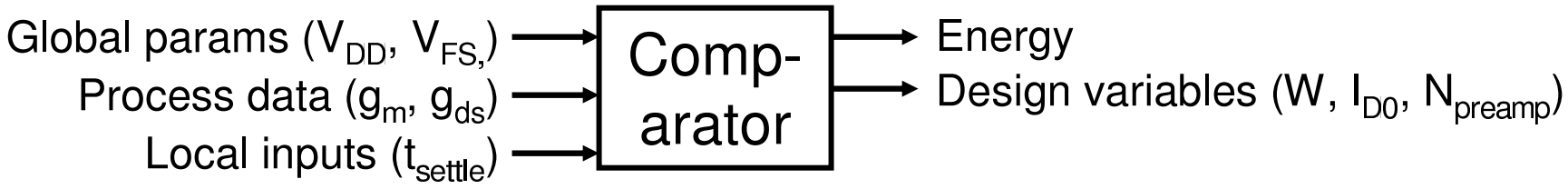
Block Implementation

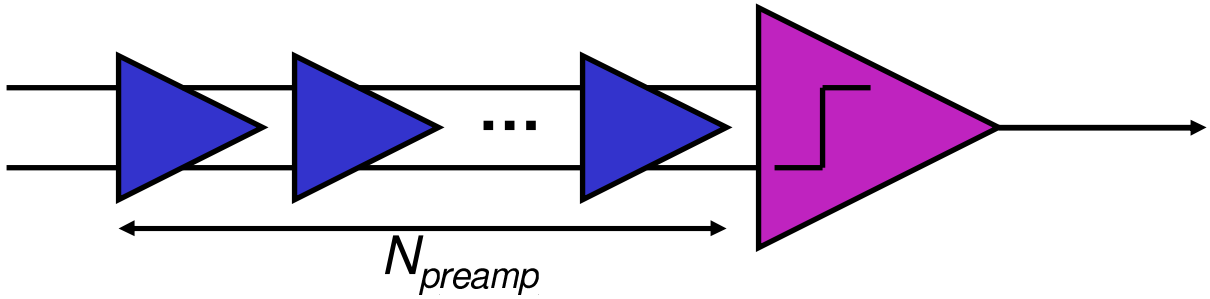
- All blocks within the energy model are implemented as Matlab functions with similar structure

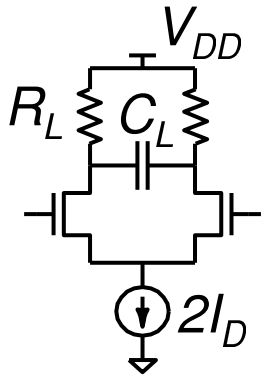


  - Arbitrary calculations can be performed with the block
  - Local inputs and outputs pass dependencies between blocks
- Limited process information is extracted from SPICE simulations and input as tables into the optimization
  - Transistor g_m, g_{ds}, C_{GS}, … as a function of J_D, V_{DS}
  - Digital inverter delay and power as a function of V_{DD}
  - Wiring parasitic estimates

Example: Comparator Block







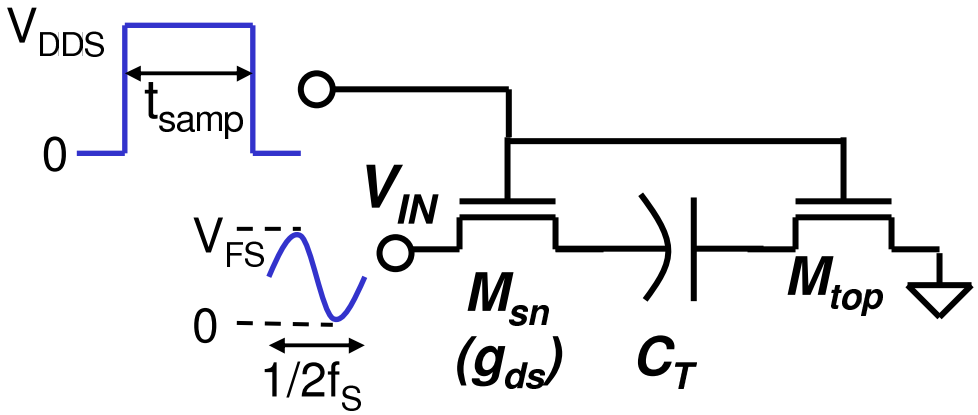
- Autozeroed comparator optimization generalized from the equations in [Ginsburg, JSSC 2/2007]
- Constraints on required input-referred offset, $V_{OS,in}$, and number of time constants for settling, N_τ, are derived from a parallel behavioral model

$$\frac{t_{settle}}{N_\tau} = R_L C_L N_{preamp}$$

$$A_V = \frac{V_{OS,latch}}{V_{OS,in}} = (g_m R_L)^{N_{preamp}}$$

Digital/Analog Interface: Sampling

- Sampling demonstrates low-level circuit interaction between analog and digital
- First, the analog design problem:



Settling constraint

$$t_{sample} > k_{slew}(b+1)\ln(2)\tau_{samp}$$

Tracking constraint

$$\frac{1}{\sqrt{1+(f_S\tau_{samp}/2)^2}} > 1-2^{-(b+1)}$$

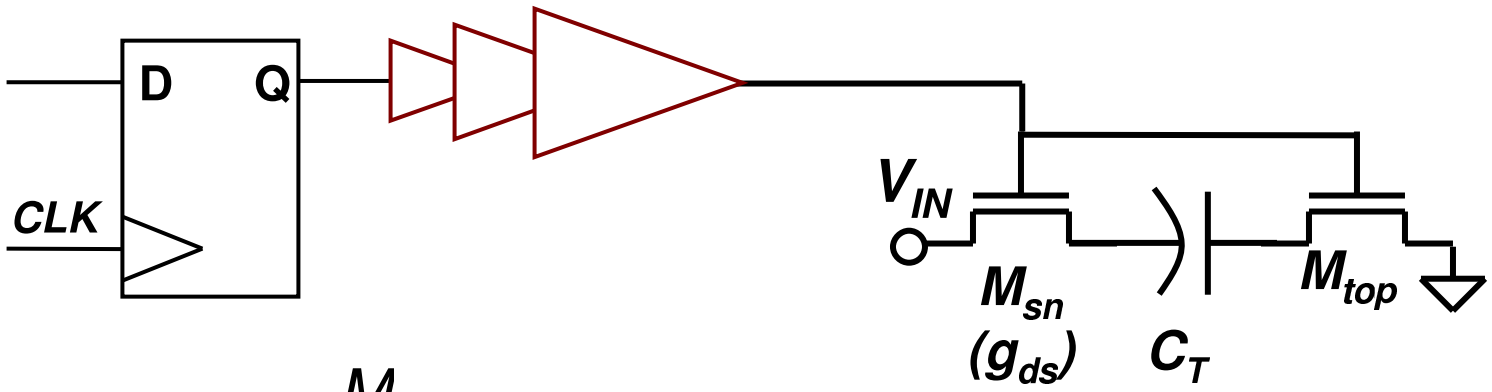
$$\tau_{samp} = C_T / g_{ds}(V_G = V_{DDS}, V_S = V_D = V_{FS})$$

Charge pump assumed to generate $V_{DDS}>V_{DD}$

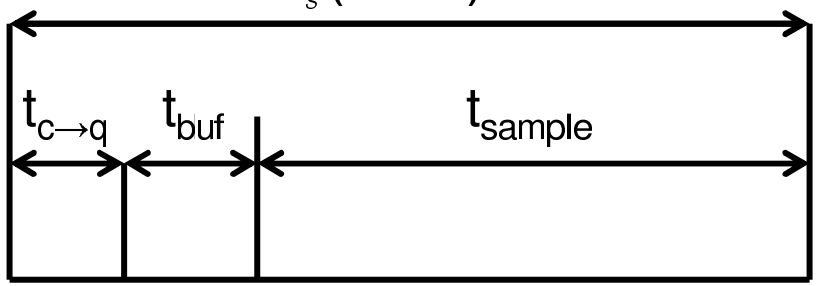
Timing + Energy Closure of Sampling

- Sampling switch tends to be large
- Digital circuits driving analog is turned into a timing-only problem

Buffering automatically inserted in model



$$\frac{M}{f_s(b+1)}$$



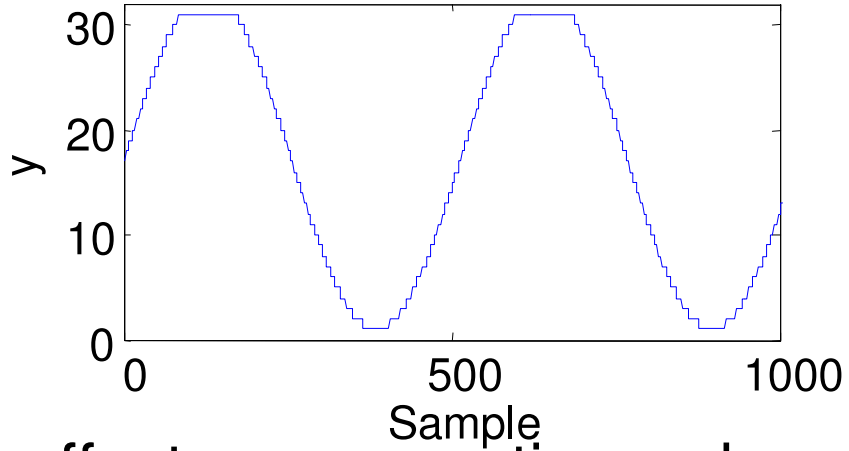
Timing is solved iteratively within the model because buffer insertion may increase sampling switch width through decreased t_{sample}

A/D Tradeoffs: Offset Mitigation

- Effect of offset for interleaved ADC
  - Introduction of periodic offset term in the output:

$$y[n] = Q\left(v_{IN}[n] + v_{OS}[n(\mathrm{mod}\, M)]\right)$$

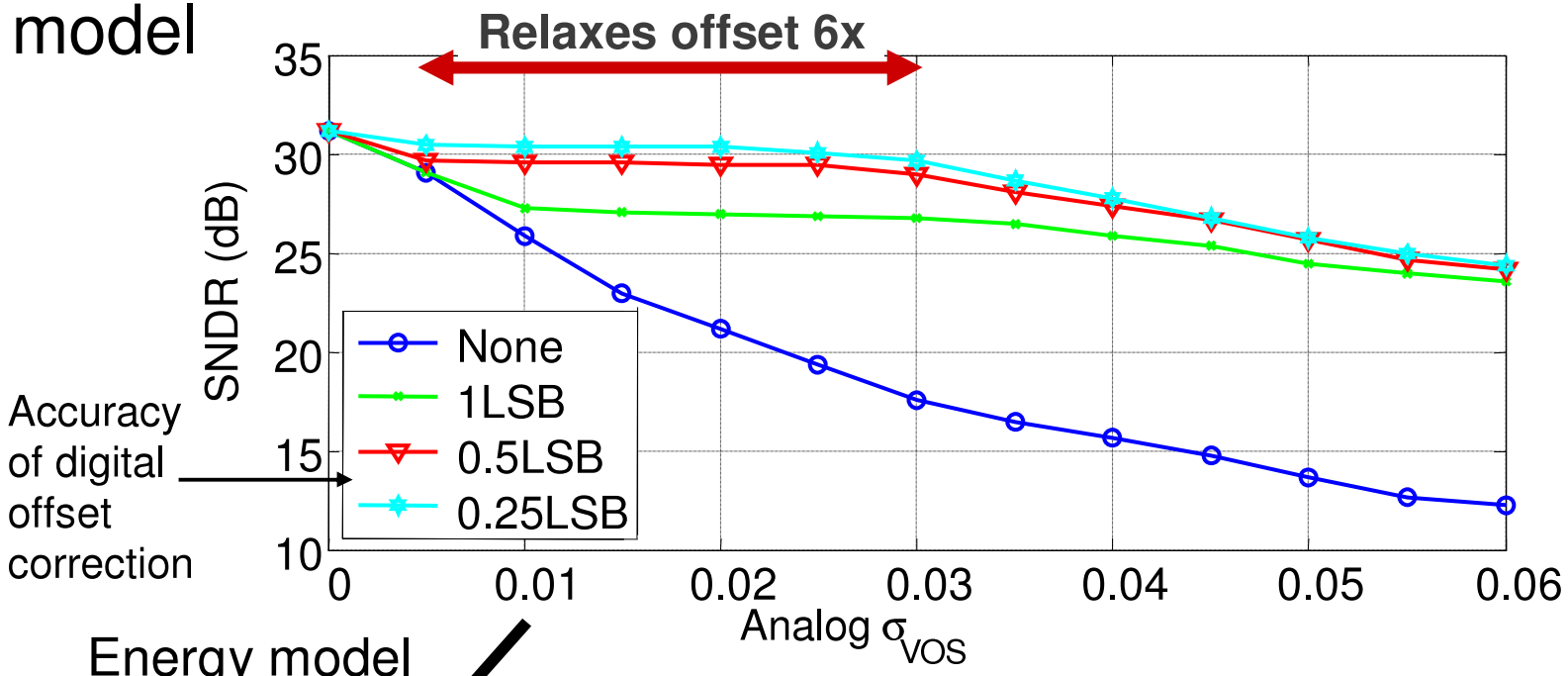
  - Asymmetric clipping of large input signals.



- Analog-only offset compensation reduces periodic term and, as a side effect, makes clipping negligible.
- Mixed-signal approach
  - Use digital offset correction for periodic term.
  - Analog offset requirements for clipping only.

Mixed-Signal Offset Compensation

Architectural tradeoff evaluated with coupled behavioral model



Energy model constraint

$$V_{OS,in} = \begin{cases} \dfrac{2^{-b} V_{FS}}{6} & \text{no digital correction} \\ \dfrac{2^{-b} V_{FS}}{2} & \text{with digital correction} \end{cases}$$

For 1dB SNDR penalty, use one stage preamplifier + digital offset correction.

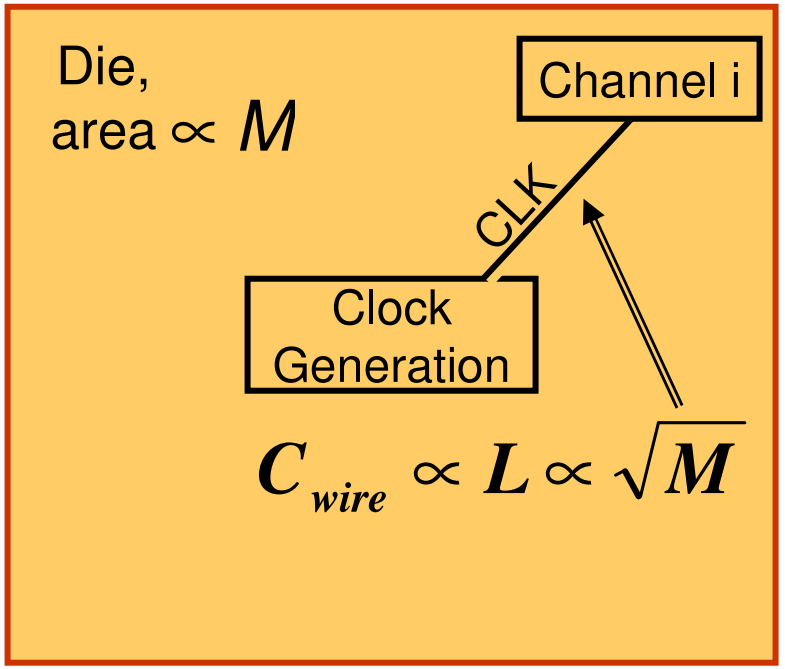
30% overall energy savings.

Parallelism Overheads

- Interleaving is not free; clock distribution across the large die can be a major power impact
- Assumptions
  - Clock path balanced to every channel
  - Each channel receives minimum frequency, $f_S(b+1)/M$, clock

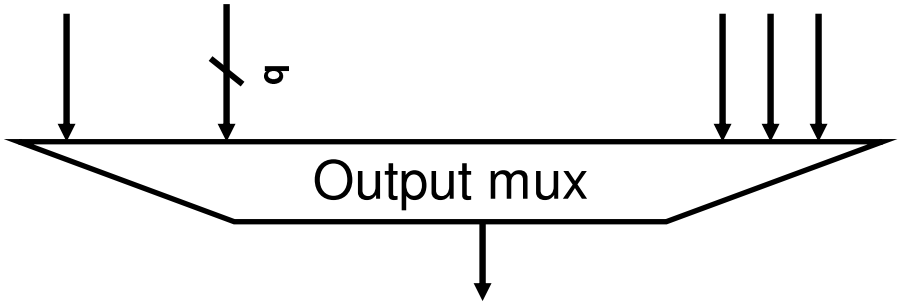
$$E_{CLK} \propto C_0 M^{1/2} V_{DD}^2 (b+1)$$

- If every channel receives the full-speed sampling clock, $E_{CLK} \propto M^{3/2}$



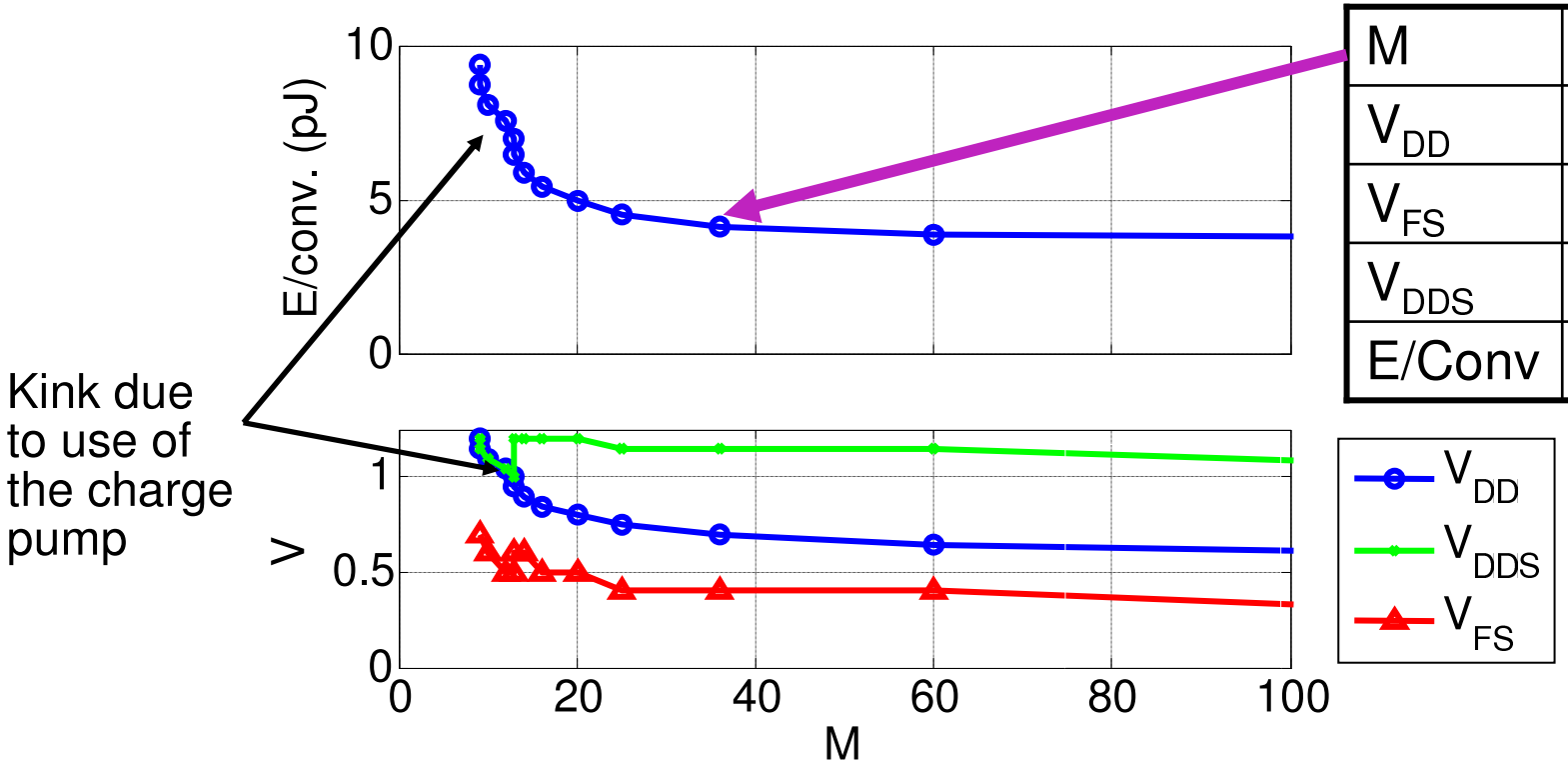
- Other main overhead: multiplexer to re-sort the outputs

$$E_{MUX} \propto b \log M$$



Results

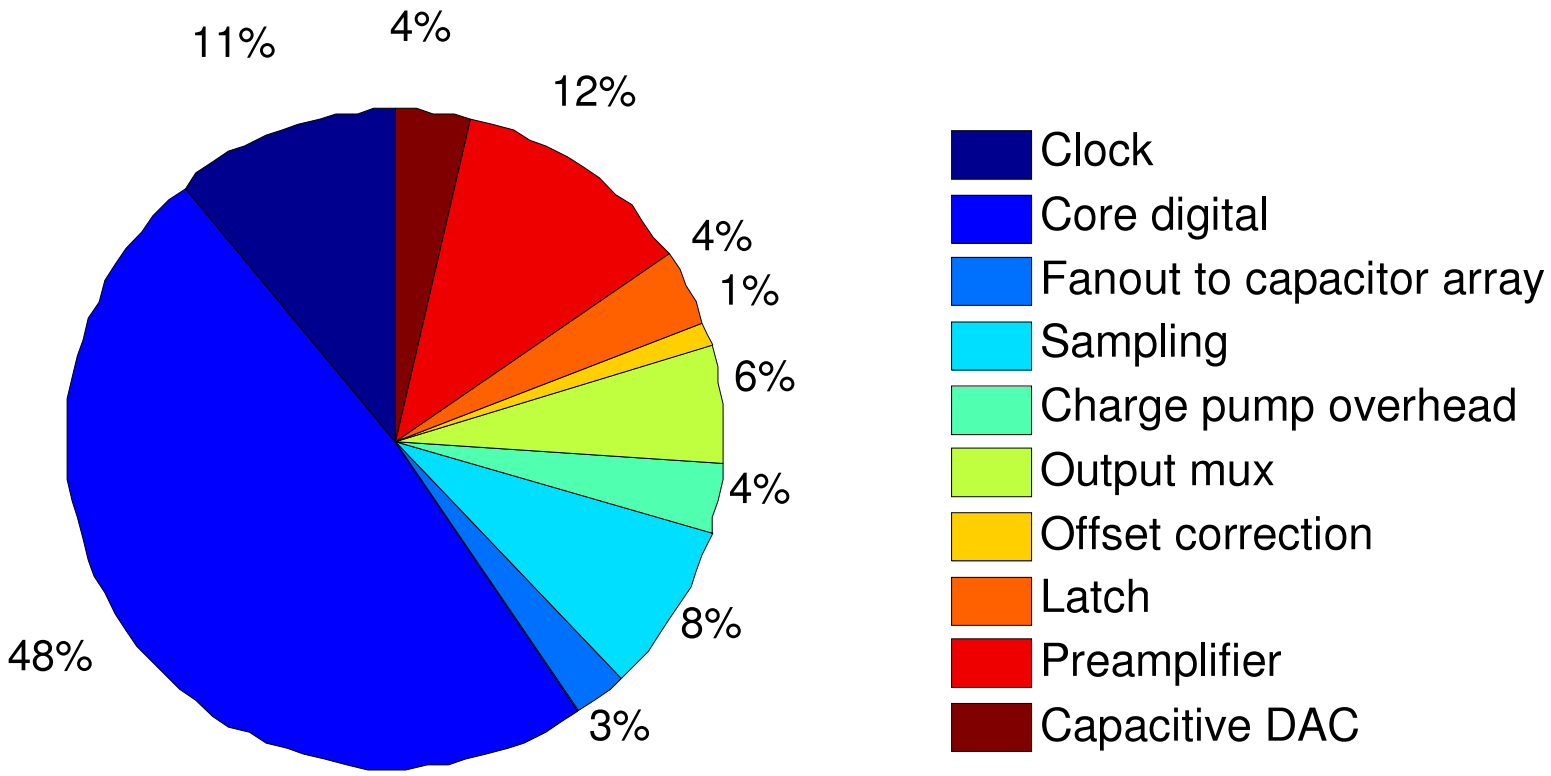
- Solution found in <30 minutes on a 1.8GHz Linux workstation
- The optimization returns initial design parameters for analog transistor sizes, bias currents, digital output buffers, etc.



M	36
V_{DD}	0.7 V
V_{FS}	0.4 V
V_{DDS}	1.15 V
E/Conv	4.15 pJ

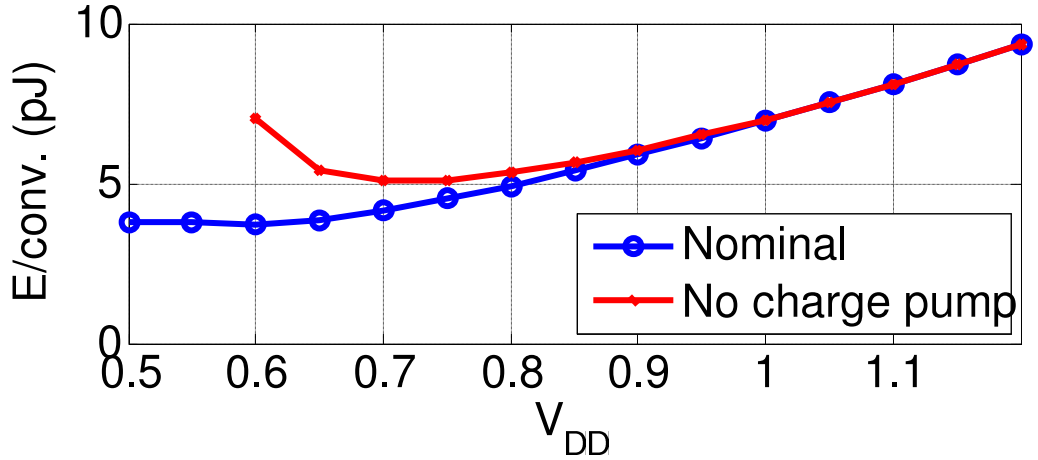
Energy Breakdown

At 36 channel operating point



Architectural Change: Charge Pump?

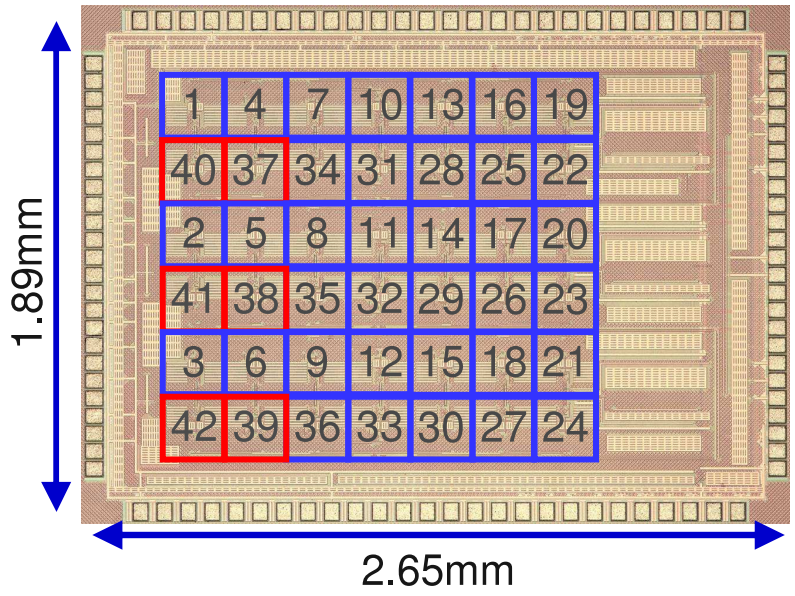
- Flexibility of the model can be demonstrated by evaluating the removal of the charge pump
- The only change is that during the optimization V_{DDS} is set to V_{DD} instead of being independently varied



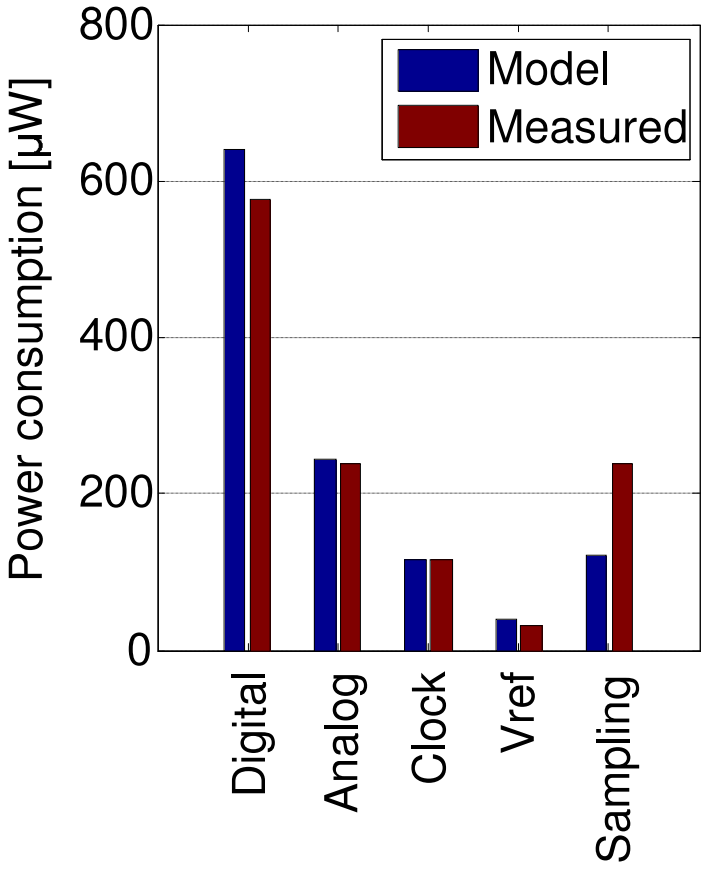
- Even with overhead of a non-ideal charge pump (η_{CP}=70%), driving the digital logic to a lower voltage gives 22% lower energy

Comparison to Silicon

- Test chip fabricated in a 65nm CMOS process [Ginsburg, ISSCC 2008]



Measured power breakdown closely matches model



Conclusions

- Digital power consumption and performance impact is non-trivial in mixed-signal circuits and systems
- ADC energy efficiency can be enhanced by adopting the “digital” techniques of low voltage operation and parallelism
- A mixed-signal discrete energy optimization has been demonstrated that can bridge the analog/digital divide for both local circuit interactions (e.g., timing constraints and fanout) and architectural tradeoffs

Acknowledgments: DARPA, NDSEG Fellowship