An Energy-Efficient Charge Recycling Approach for a SAR Converter With Capacitive DAC

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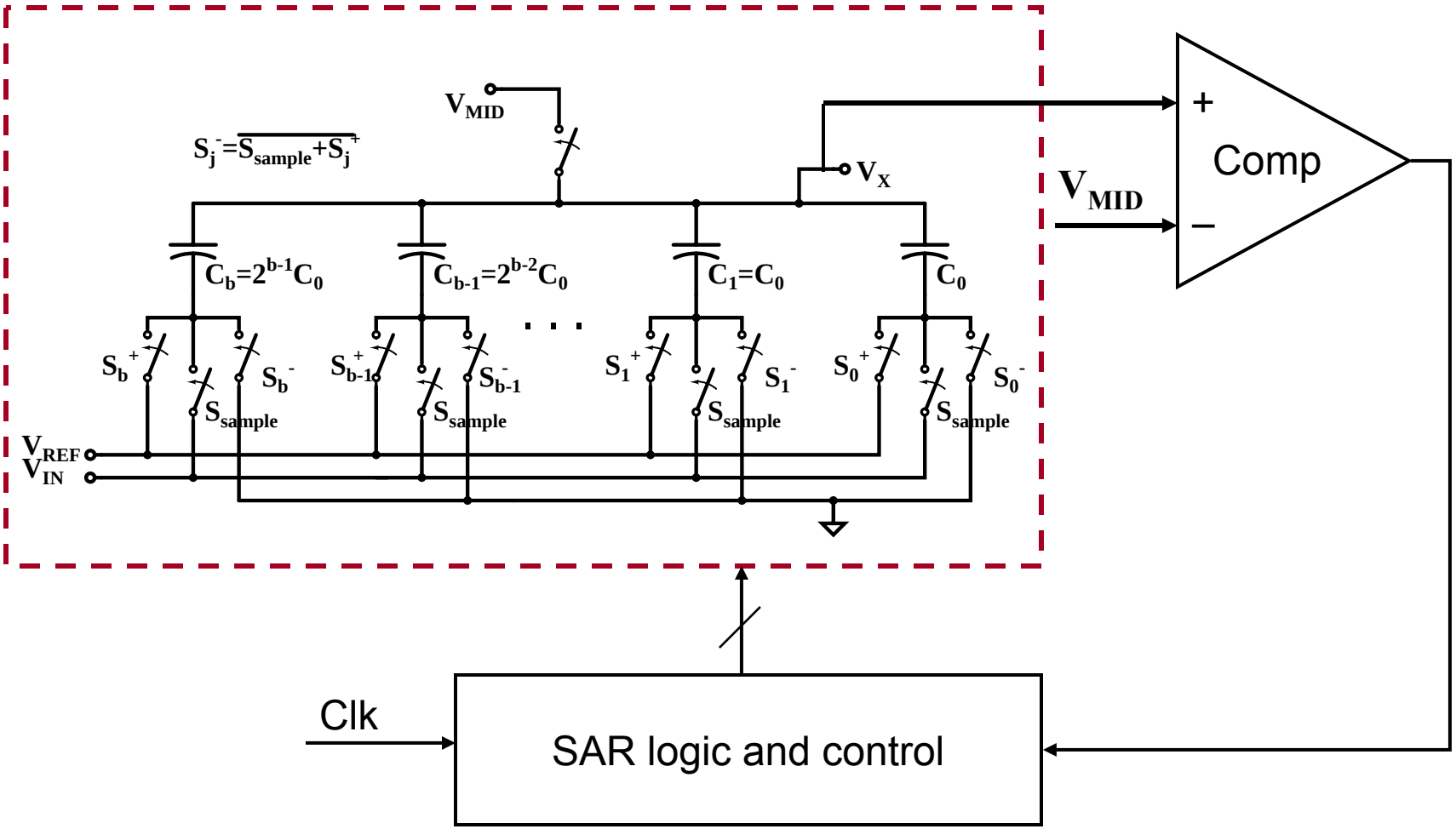
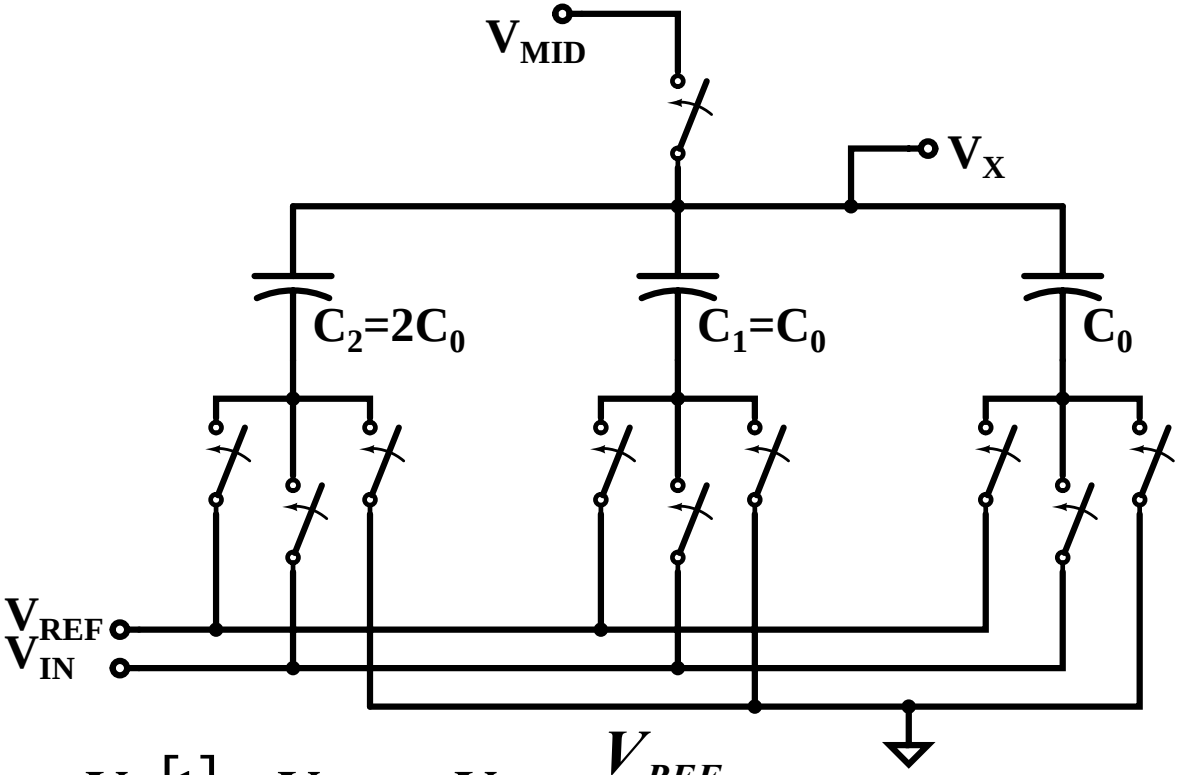
Outline

- SAR Overview
- Capacitor Switching Techniques
  - 1 Step
  - 2 Step
  - Charge Sharing
  - Split Capacitor Array
- Simulation results
- Conclusion

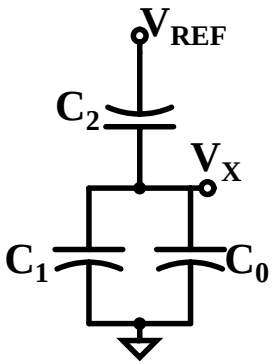
Successive Approximation Register ADC



Conventional Array: 2-bits



Bit-cycle 1

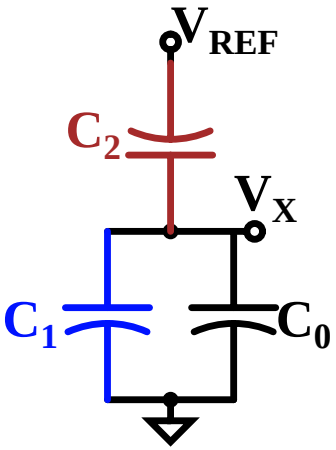


$$V_X[1] = V_{MID} - V_{IN} + \frac{V_{REF}}{2}$$

Energy drawn for first bit-cycle: $C_0 V_{REF}^2$

1-Step: 2nd Bit-cycle

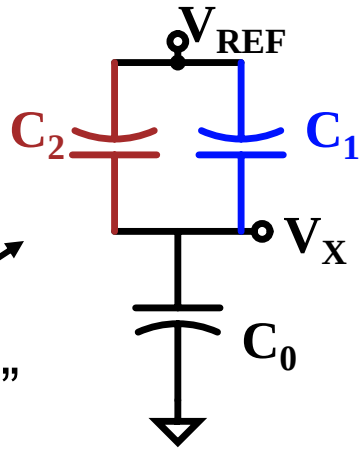
Bit-cycle 1



$V_X[1] < V_{MID}$

$\left(V_{IN} > \frac{V_{REF}}{2}\right)$

"UP"



$$E_{1\to2}^{UP} = \frac{1}{4} C_O V_{REF}^2$$

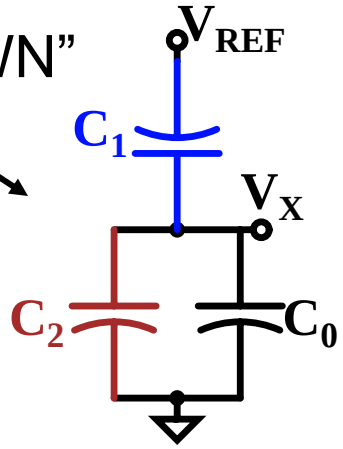
$$E_{TOP} \equiv C_T V_{REF}(-\Delta V_X)$$

$$E_{SW} \equiv C_0 V_{REF}^2$$

"DOWN"

$V_X[1] > V_{MID}$

$\left(V_{IN} < \frac{V_{REF}}{2}\right)$

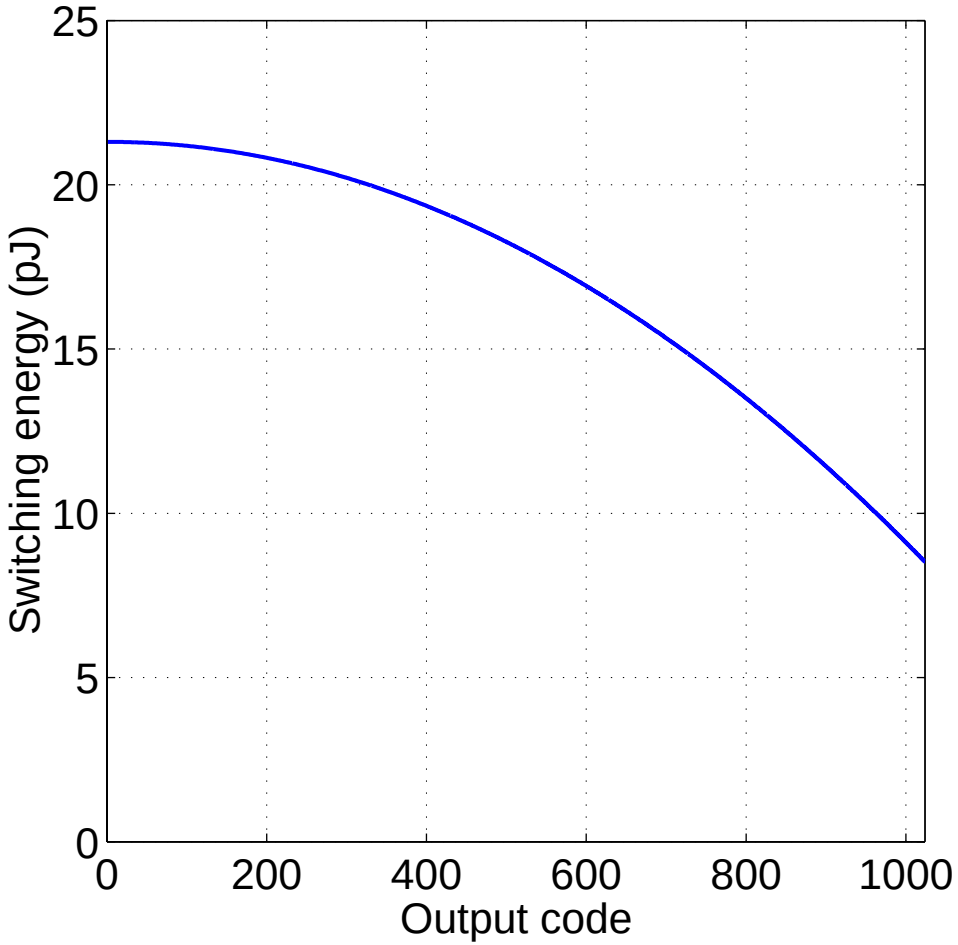


$$E_{1\to2}^{DOWN} = \frac{5}{4} C_O V_{REF}^2$$

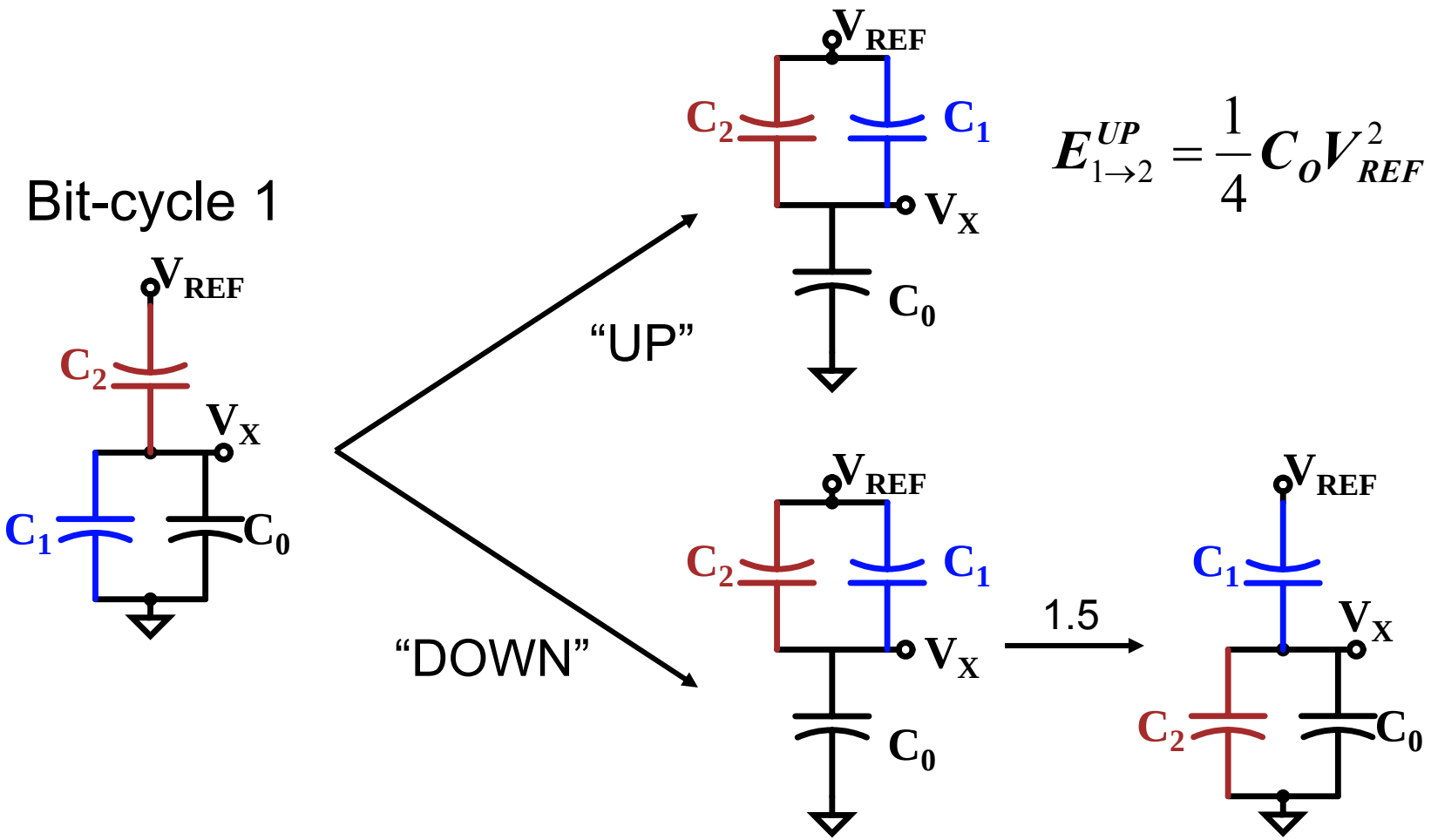
$$= E_{TOP} + E_{SW}$$

1-Step Total Energy

- Lowering V_X requires 5 times more energy than raising it.
- Total energy data dependent
- All of charge on C_2 discharged to ground.



2-Step: 2nd Bit-cycle

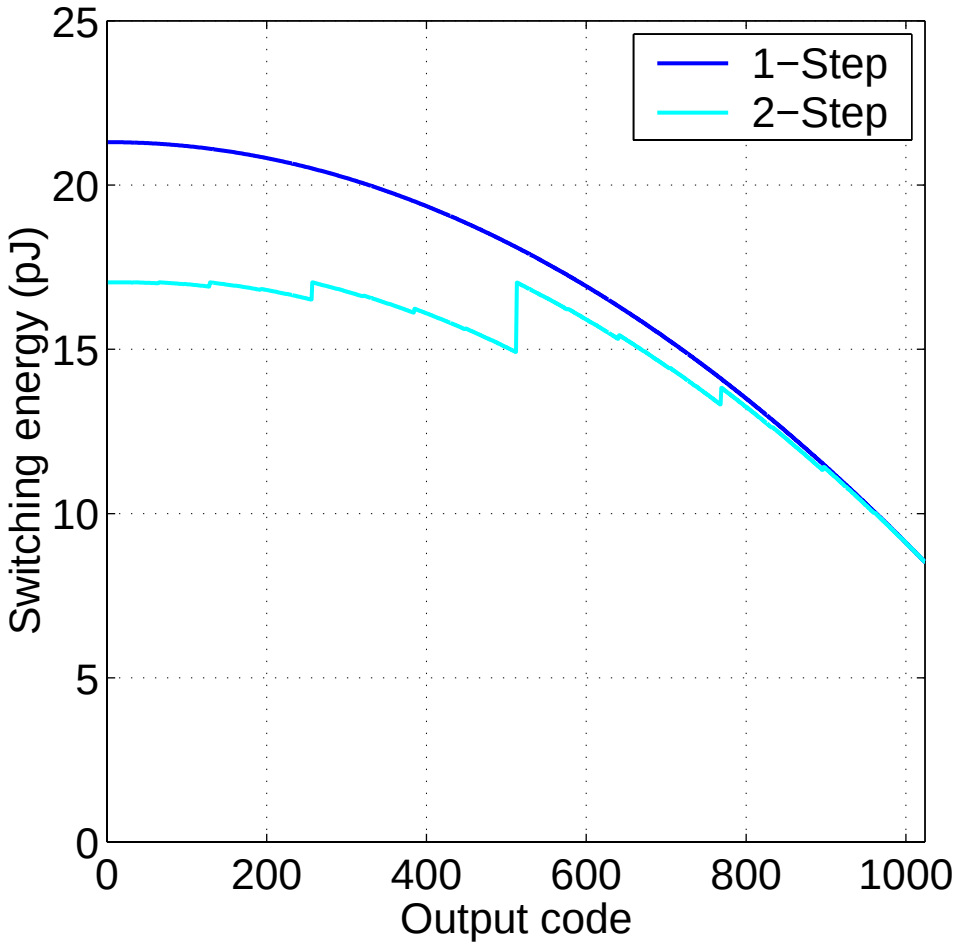


$$E_{1\to2}^{UP} = \frac{1}{4} C_O V_{REF}^2$$

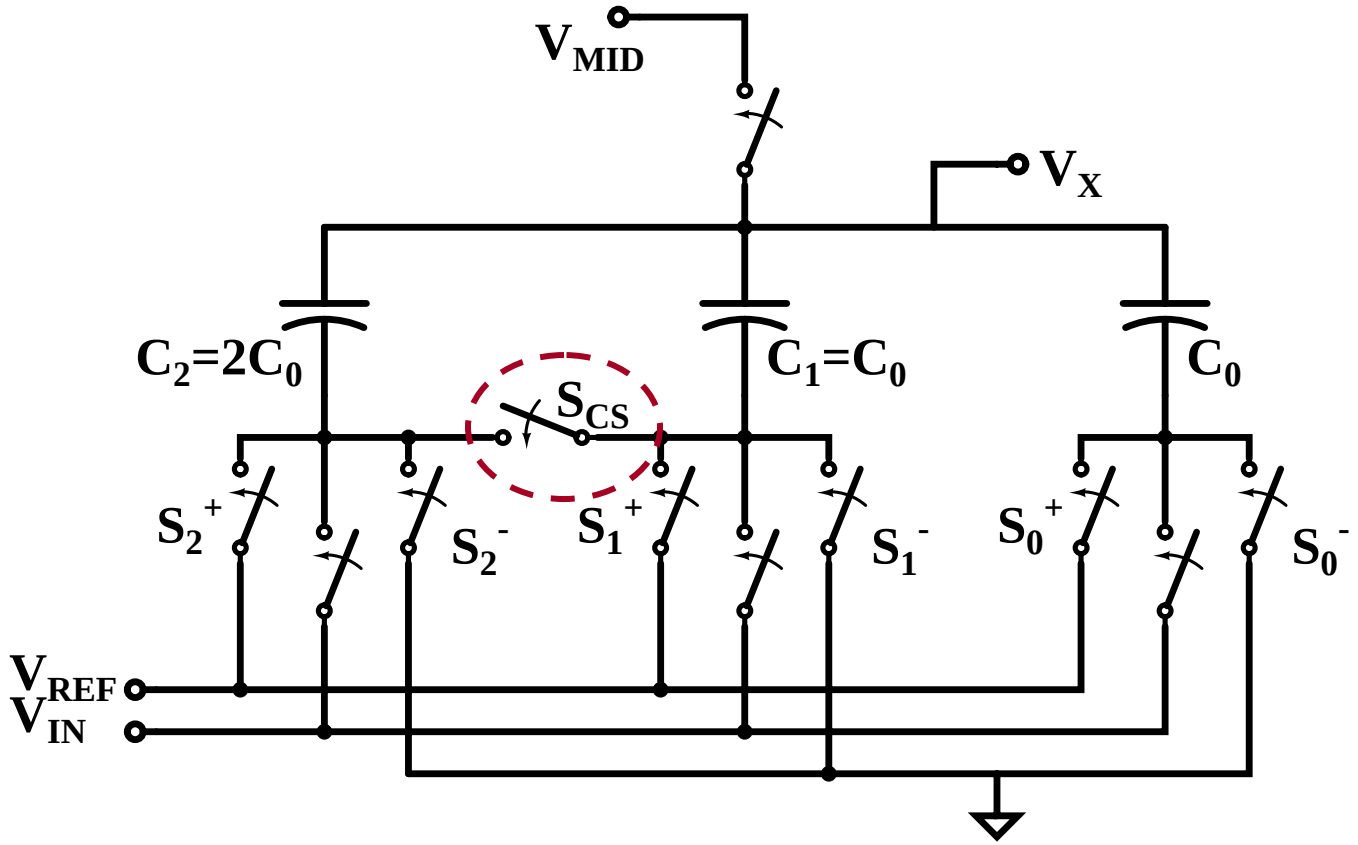
$$E_{1\to2}^{DOWN} = \frac{3}{4} C_O V_{REF}^2 = E_{TOP} + E_{SW} + 2C_0 V_{REF} \Delta V_X$$

2-Step Total Energy

- C_1 partially charged by C_2.
- Can we transfer even more charge?

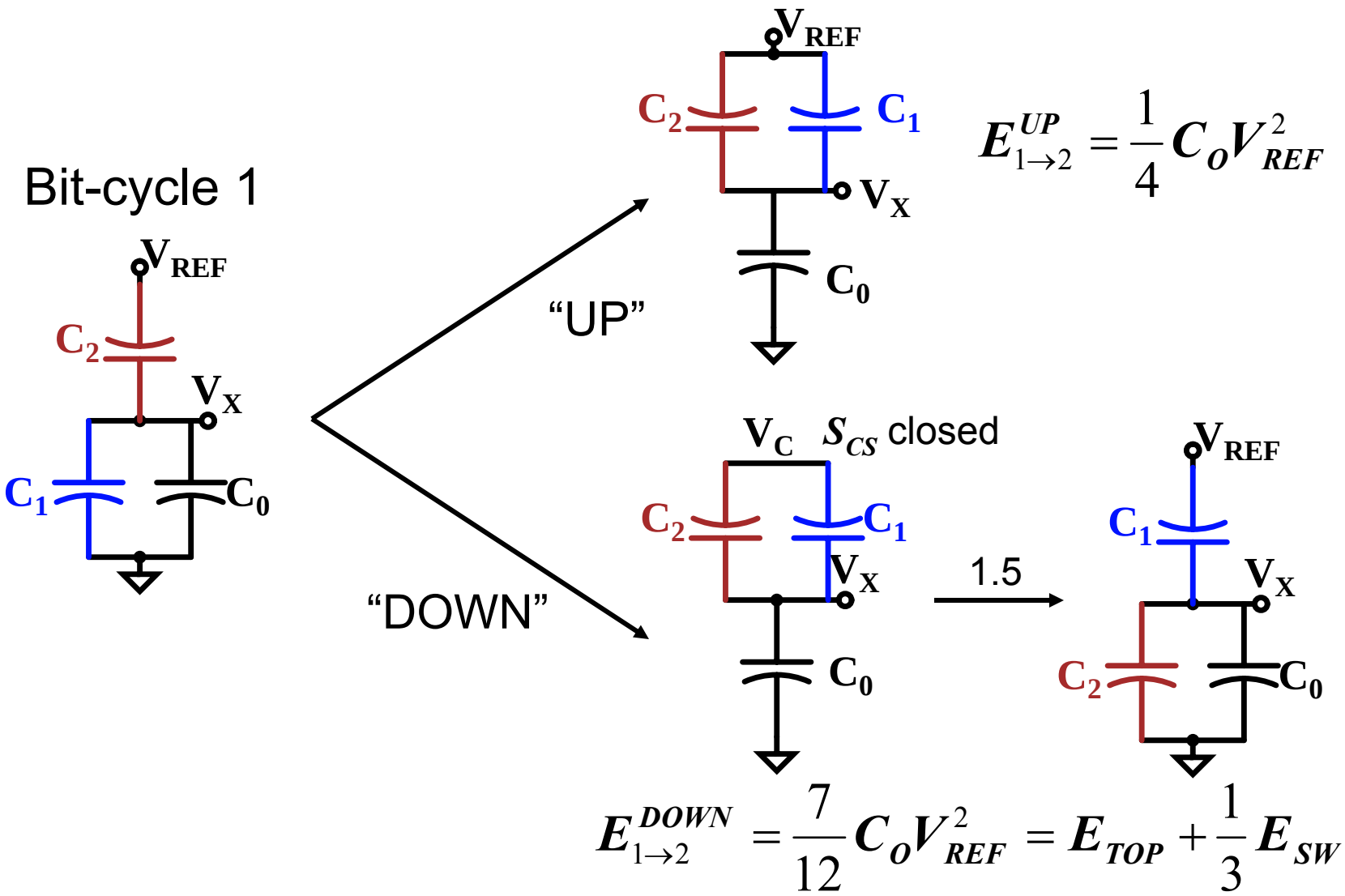


Charge Sharing Capacitor Array

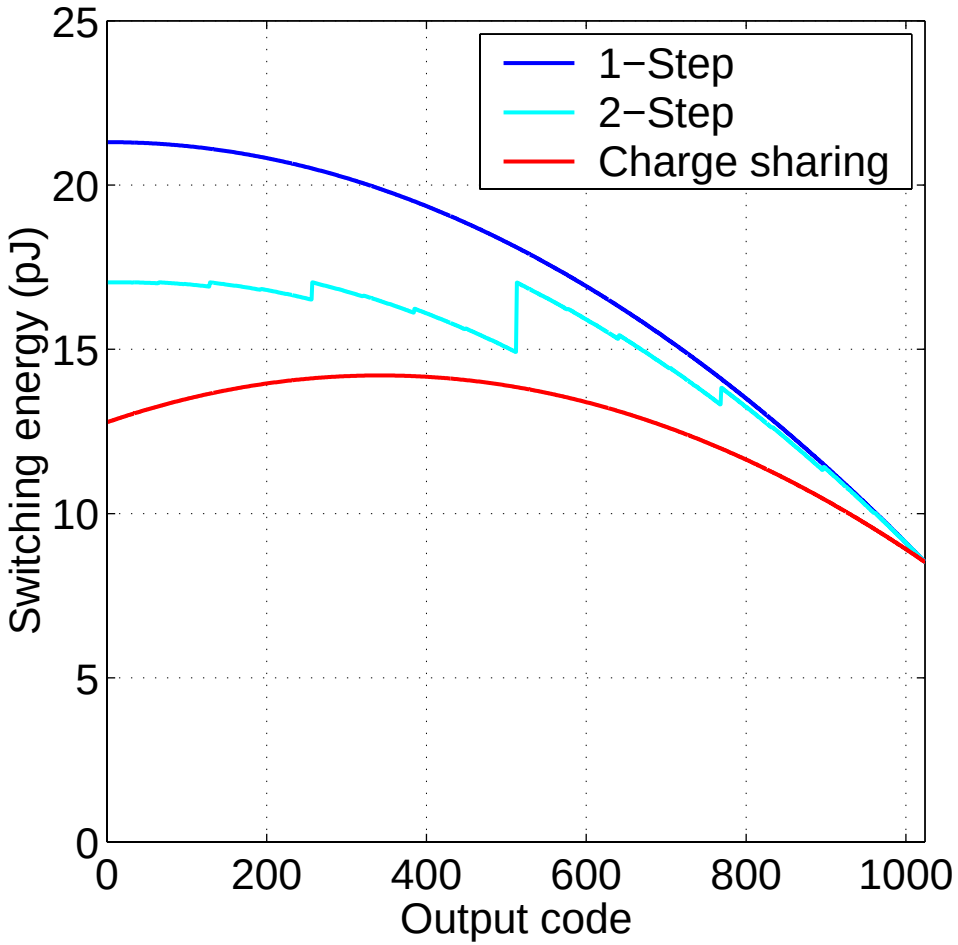


S_{CS} permits greater charge transfer between C_2 and C_1.

Charge Sharing: 2nd Bit-cycle



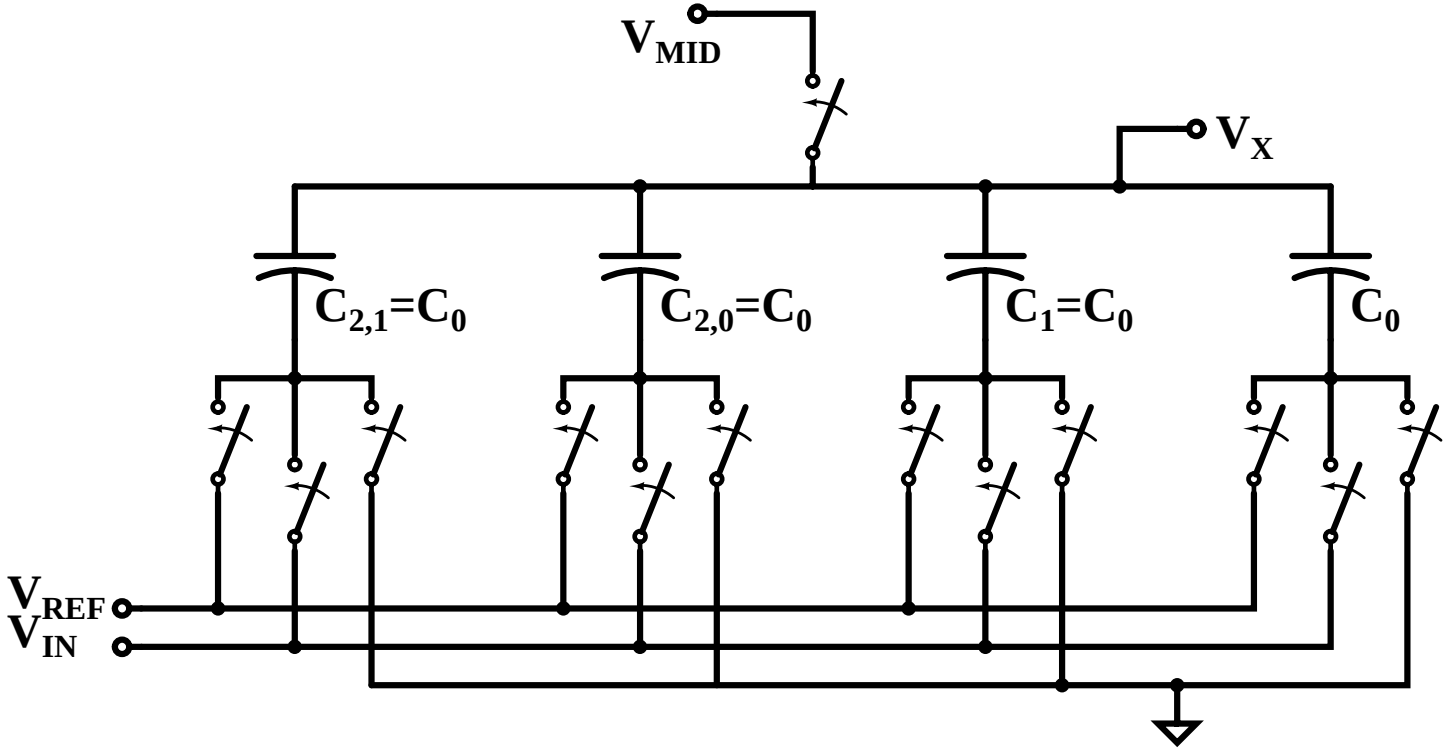
Charge Sharing Total Energy



Why charge up C_1 at all?

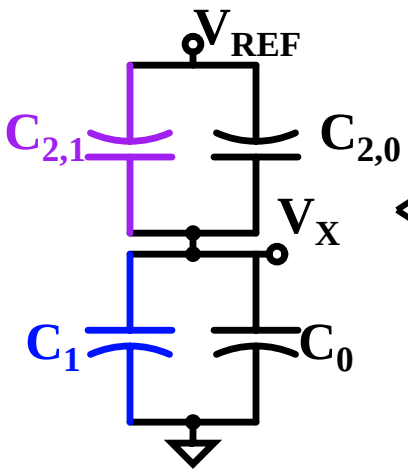
Split Capacitor Array

- Split the MSB capacitor into two separate capacitors (each of size C_0)
- Total capacitance (area) unchanged.

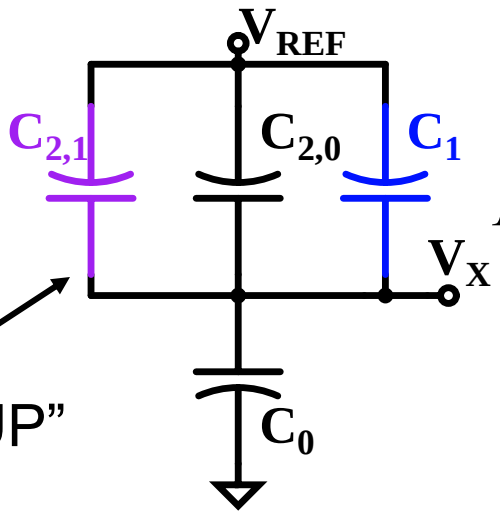


Split Array: 2nd Bit-cycle

Bit-cycle 1



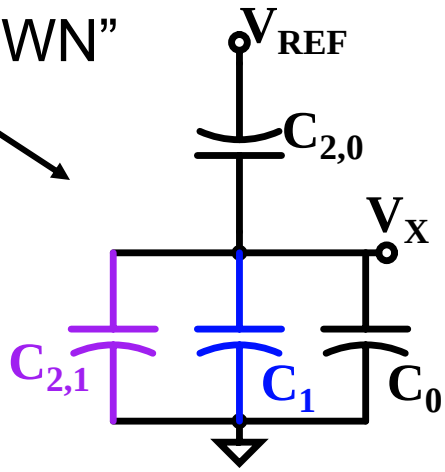
"UP"



$$E_{1\to2}^{UP} = \frac{1}{4} C_O V_{REF}^2$$

Energies match

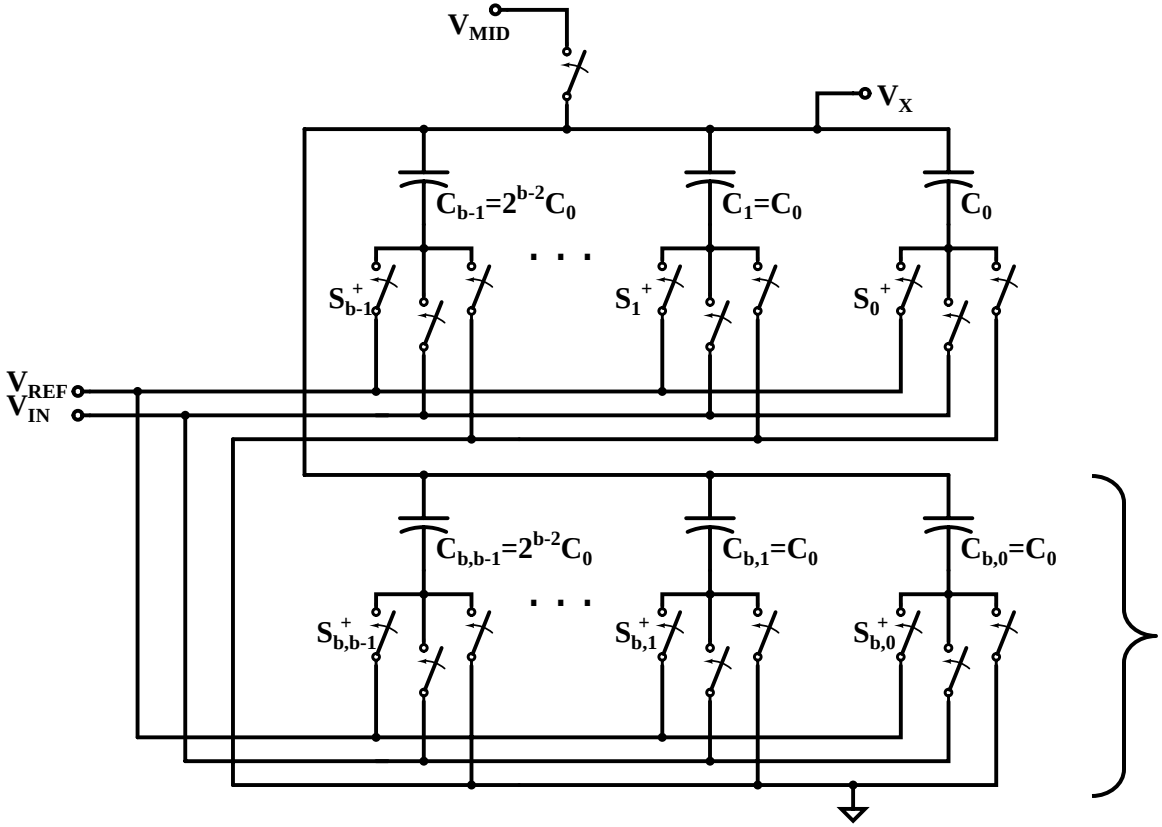
"DOWN"



$$E_{1\to2}^{DOWN} = \frac{1}{4} C_O V_{REF}^2$$

$$= E_{TOP}$$

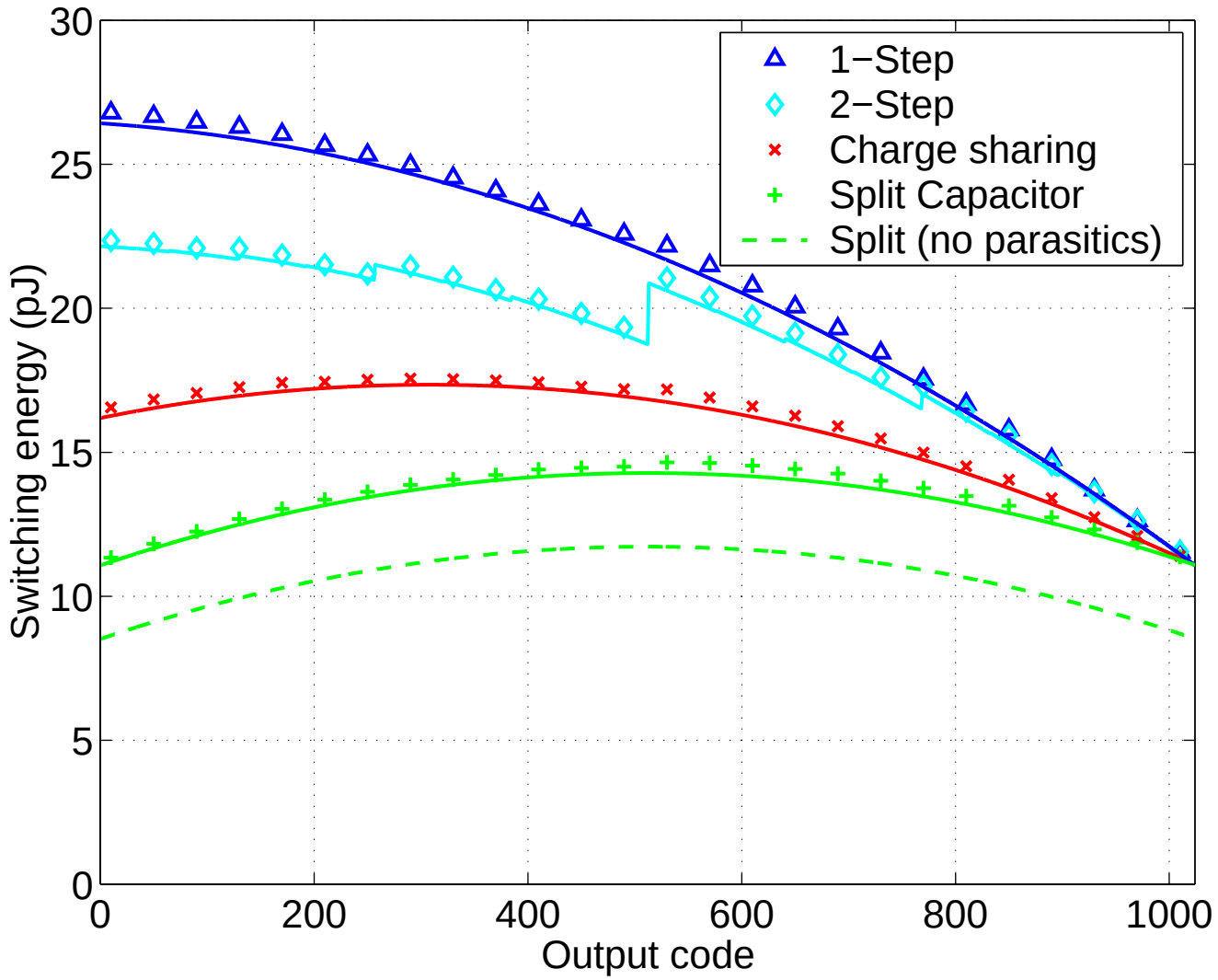
Generalized Split Capacitor Array



MSB capacitor has been split into an identical copy of the rest of the array.

- During first bit-cycle, entire MSB sub-array connected to V_{REF}.
- V_X outputs of array remain unchanged → logical operation correct.

Comparison to Simulations



Performance Summary

Method	# Switches	# Phases	Norm. E
1 step	b + 1	1	1.000
2 step	b + 1	2	0.893
CS	2b	2	0.749
Split	2b	1	0.623

- Energy based on full swing sinusoidal input distribution.

Conclusion

- New split capacitor array reduces switching energy in a DAC of a SAR ADC by 37%
  - No additional clock phases necessary
  - Well suited for large capacitor arrays

- Techniques developed for digital circuits can be used to lower power consumption in analog ones involving switched capacitors.

Acknowledgments

- HP-MIT Alliance
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- NDSEG Fellowship
- Naveen Verma from MIT for the charge sharing approach