An Active GHz Clock Network Using Distributed PLLs

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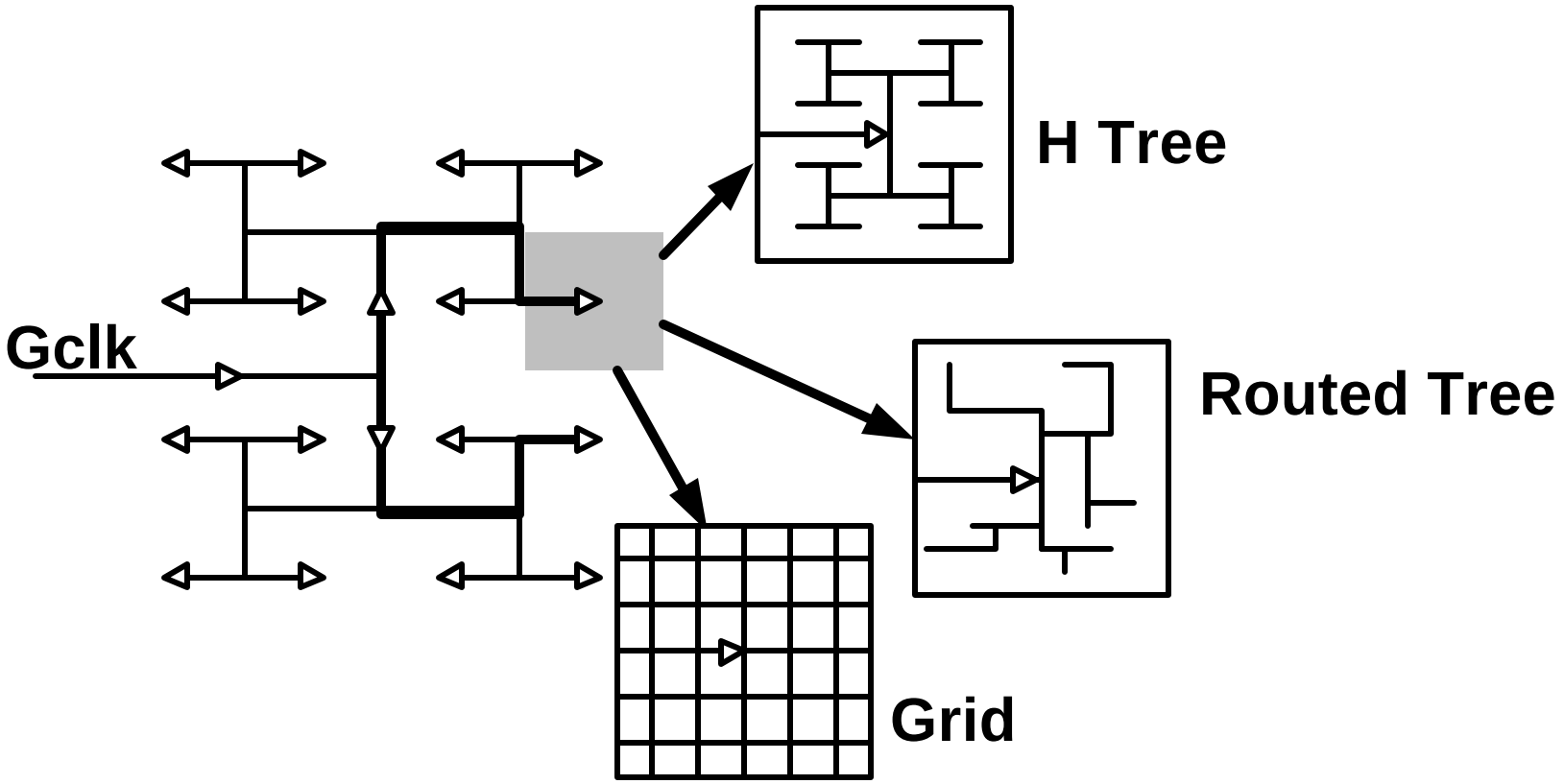
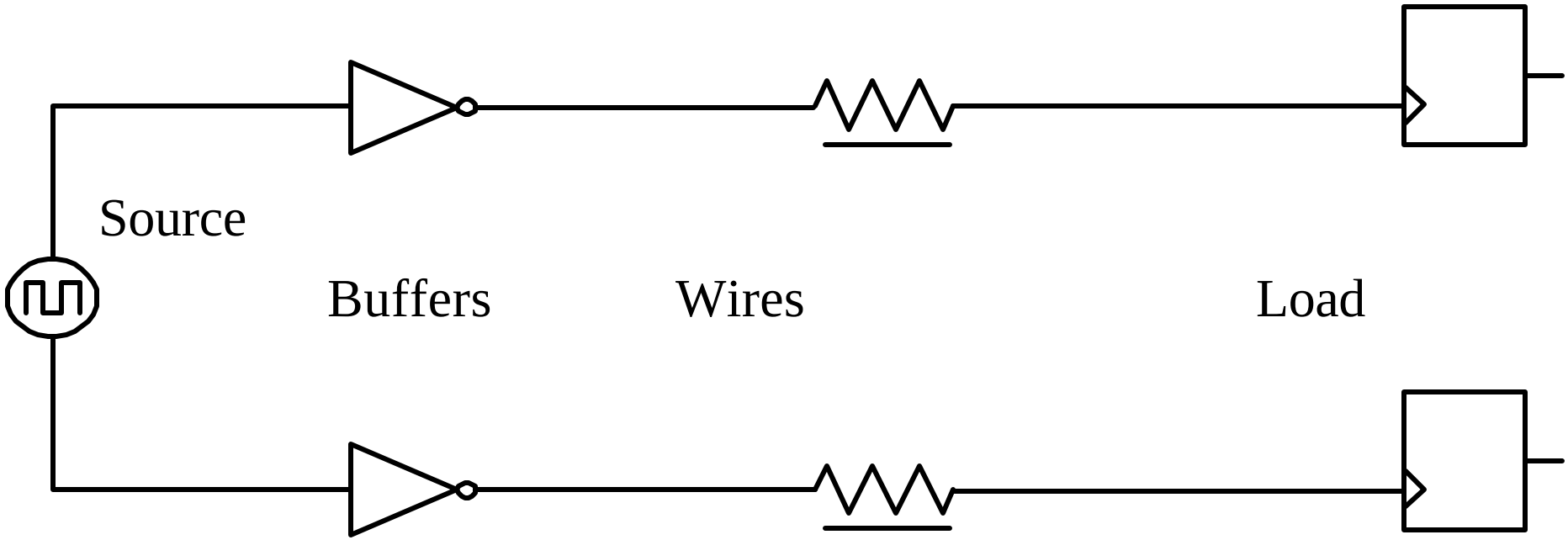
Conventional Clock Distribution



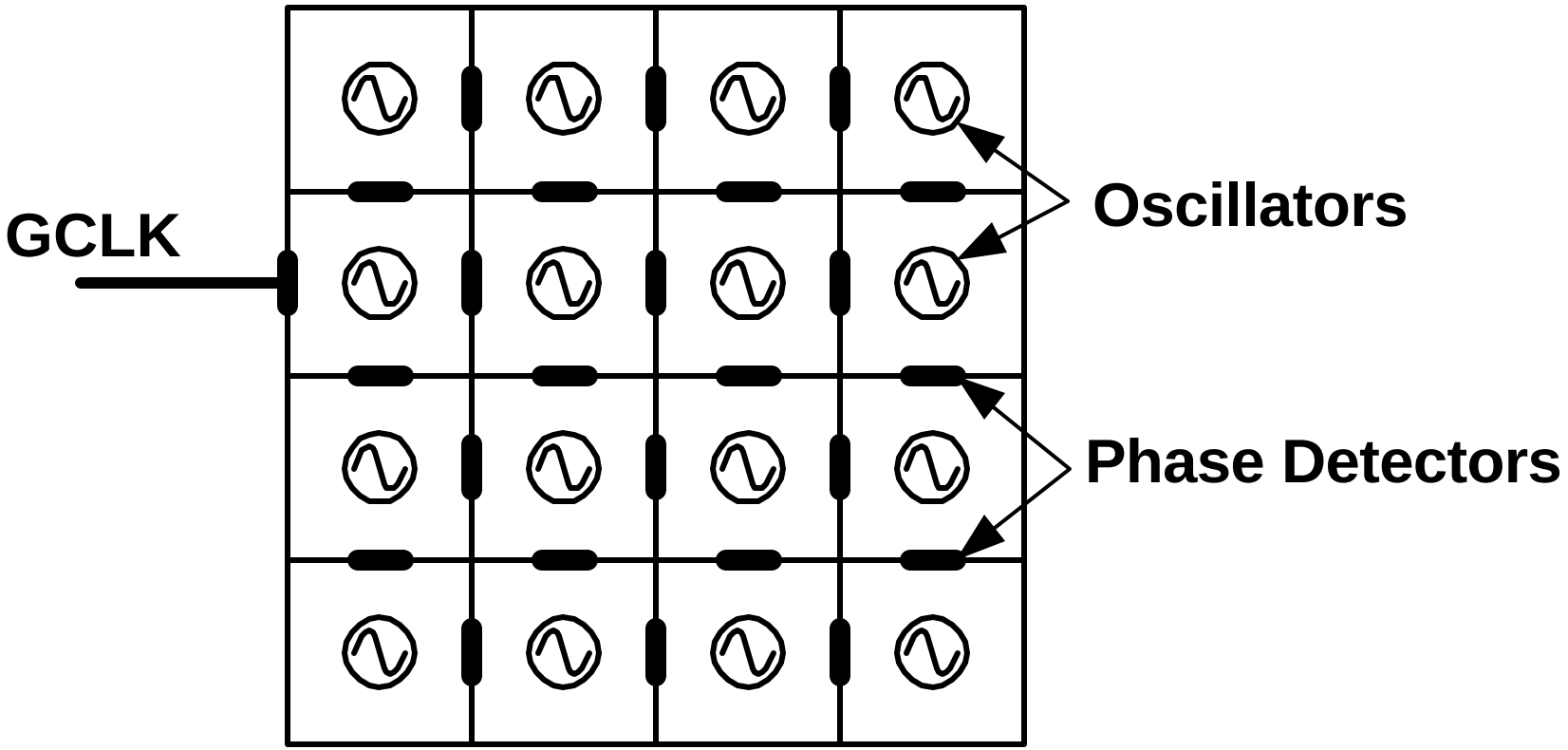
- Central distribution relies on global matching

Sources of Clock Uncertainty



- Systematic: passive compensation
- Random and dynamic: active compensation

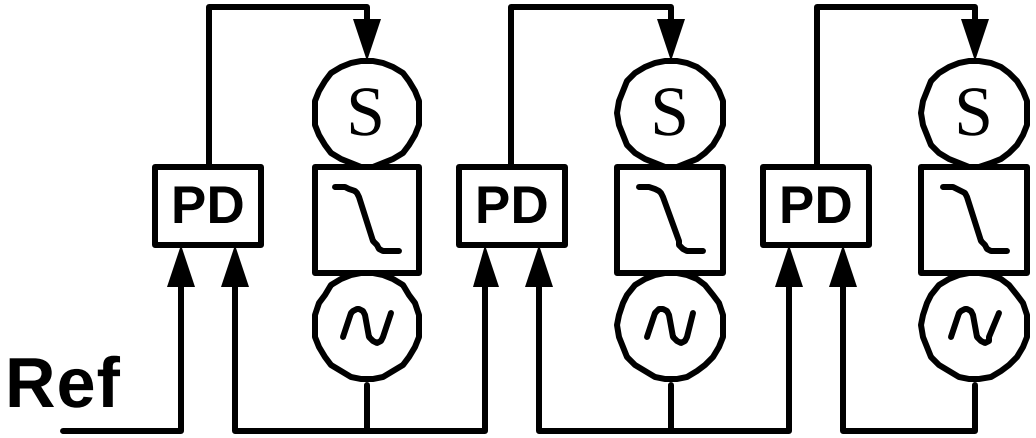
Distributed Clock Generation



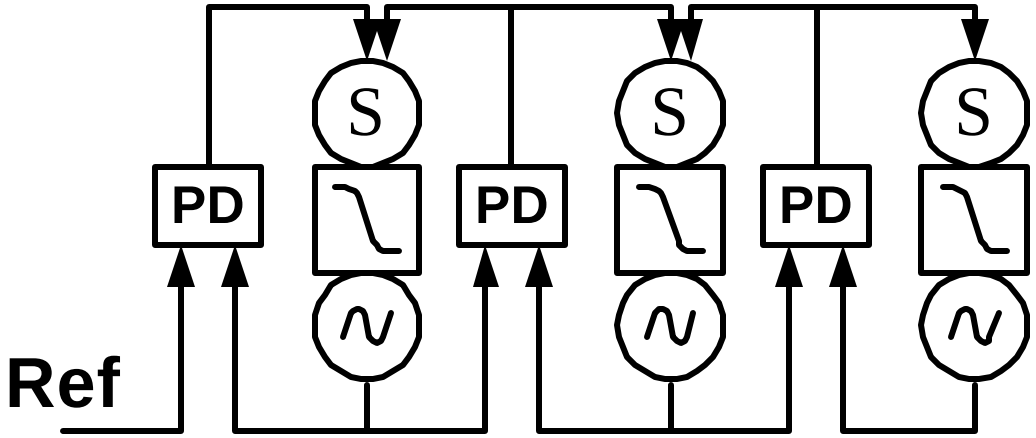
- Synchronized clock generated at multiple points

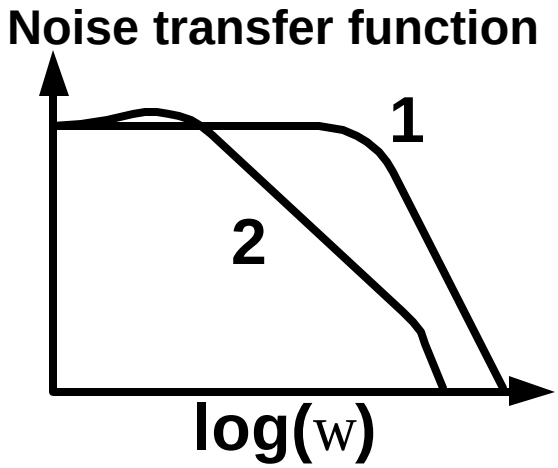
Why Symmetric PLLs?

1

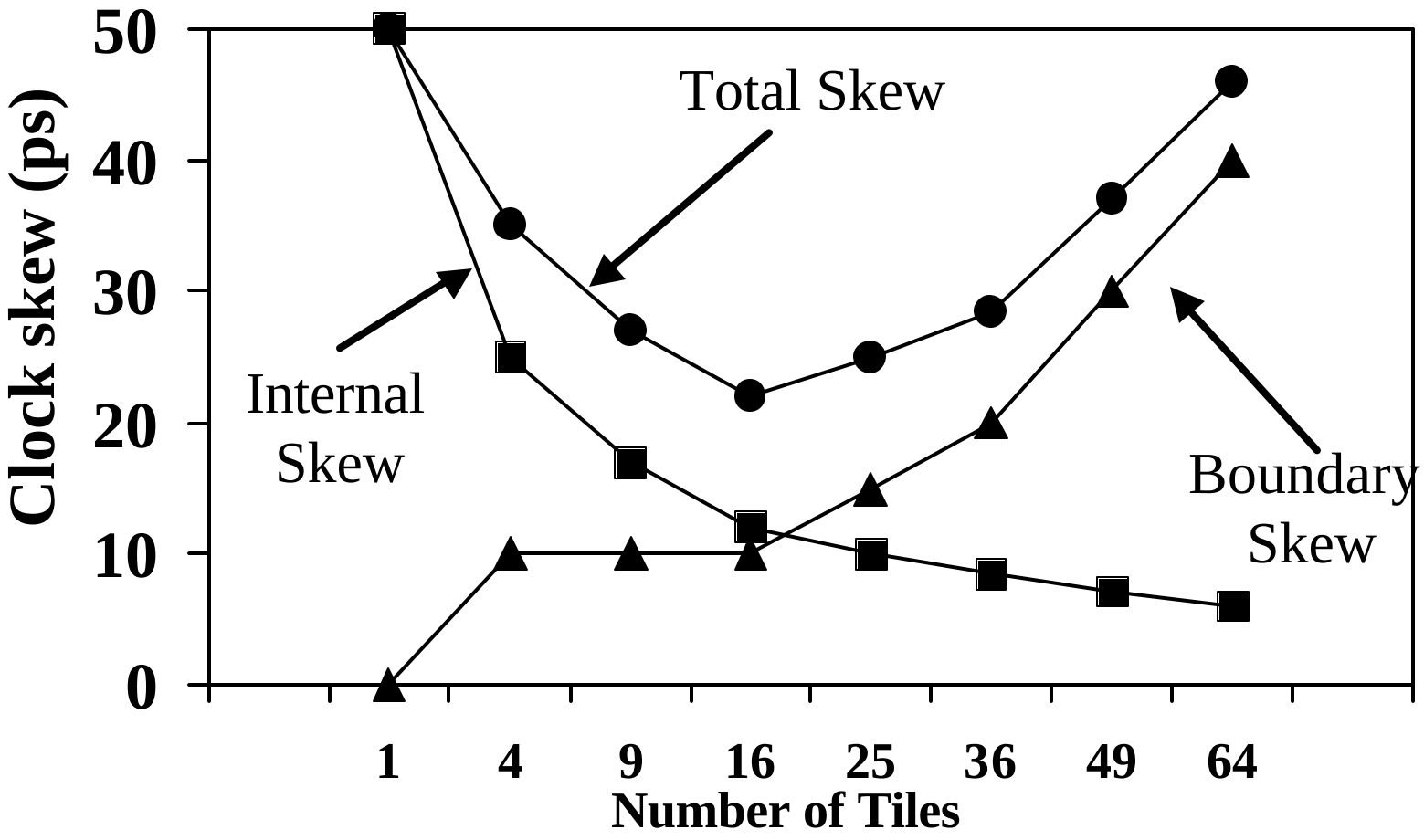


2





How Many Tiles?

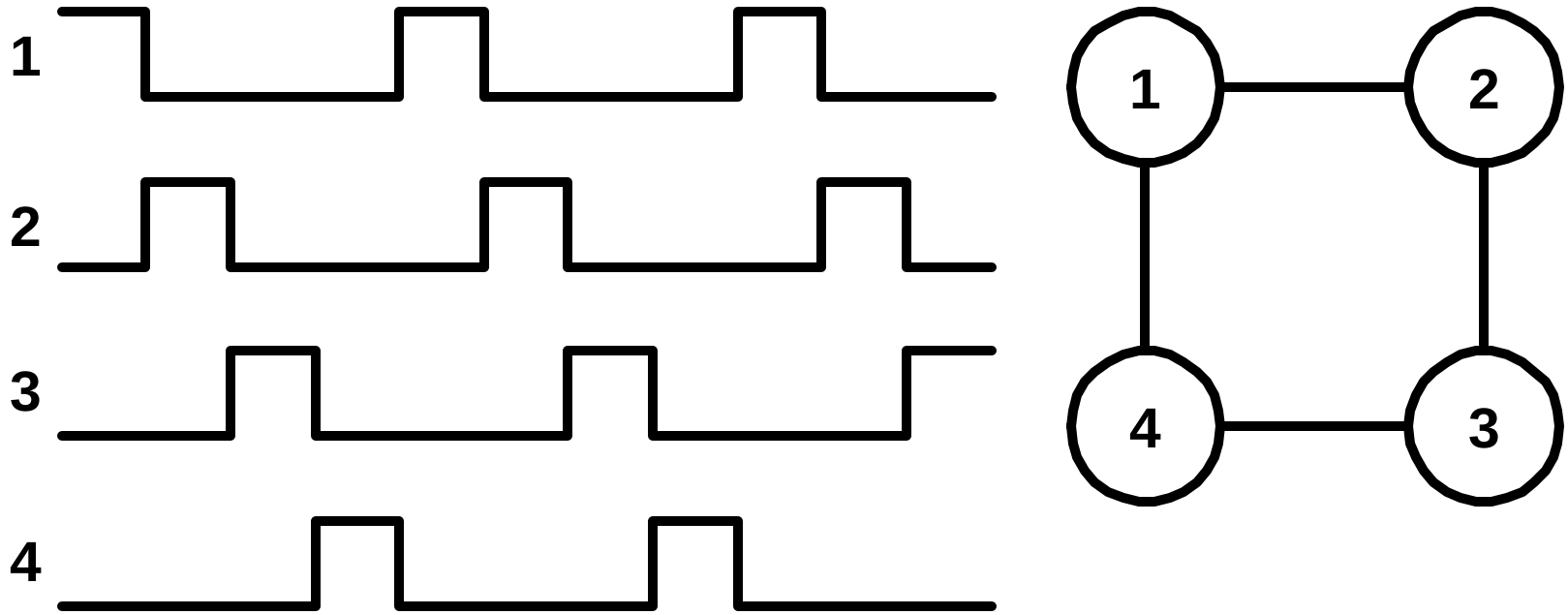


2cm x 2cm

1GHz clock

0.25 μm

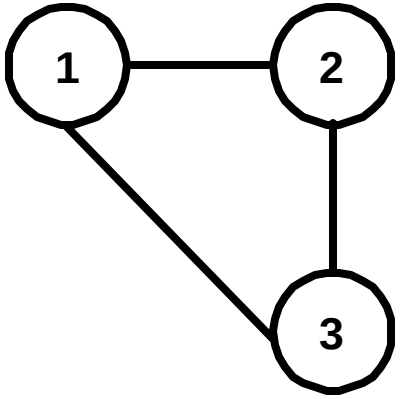
Modelock



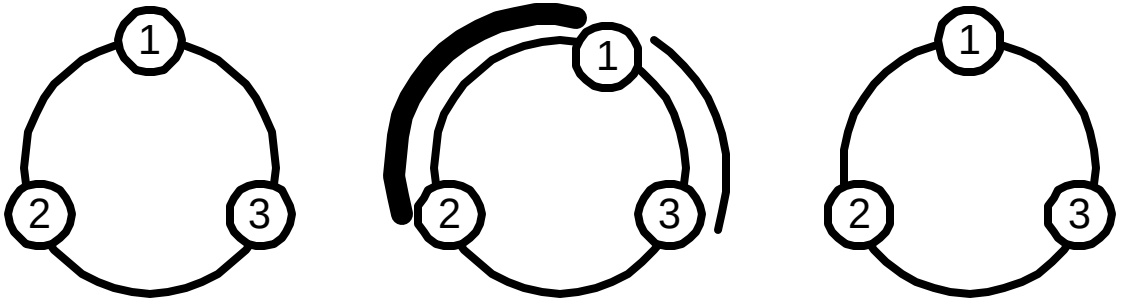
Next Phase = current phase - average phase error

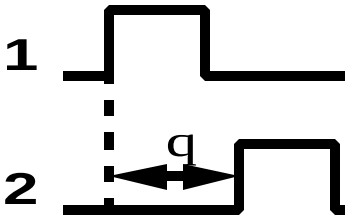
[Pratt 95]

Is Modelock Avoidable?

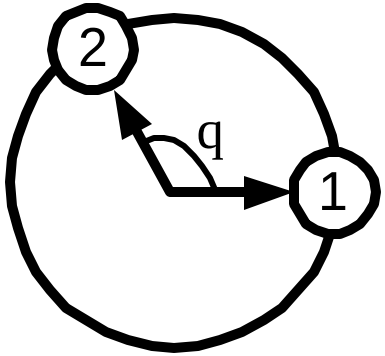


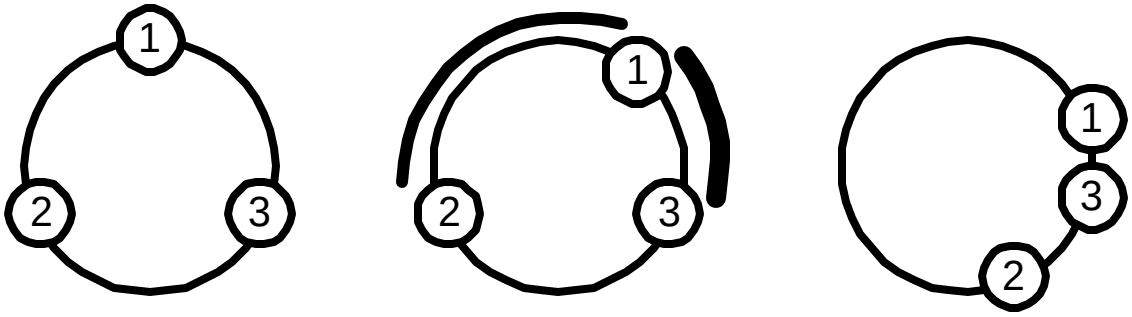
Linear phase detector: mode lock



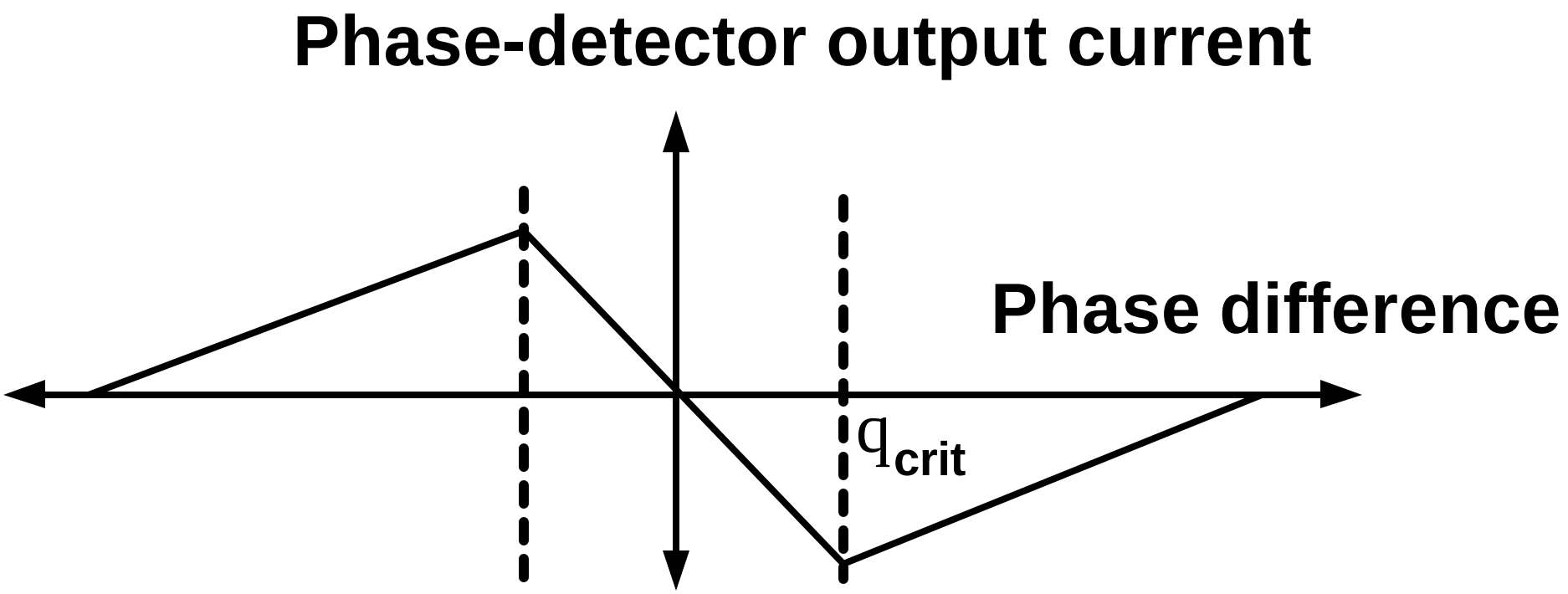


Desired phase detector



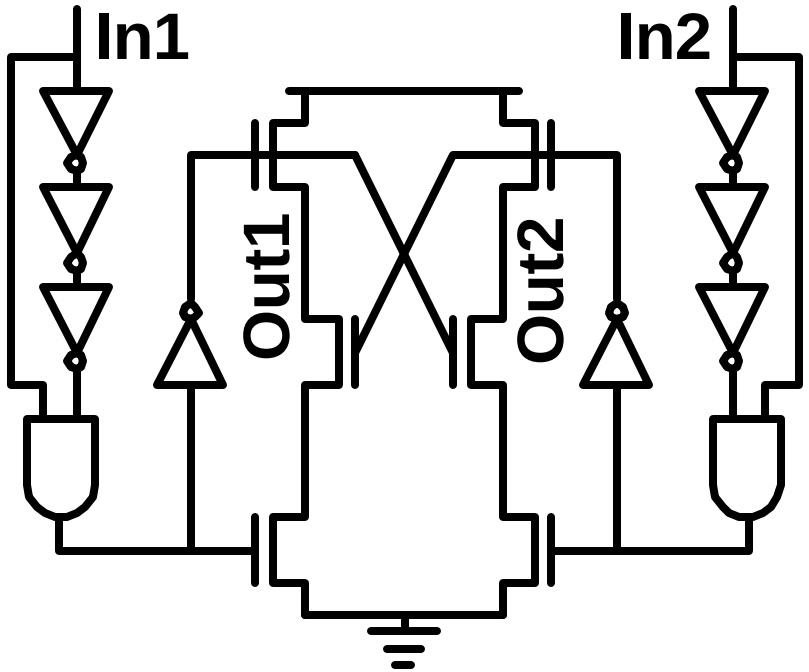


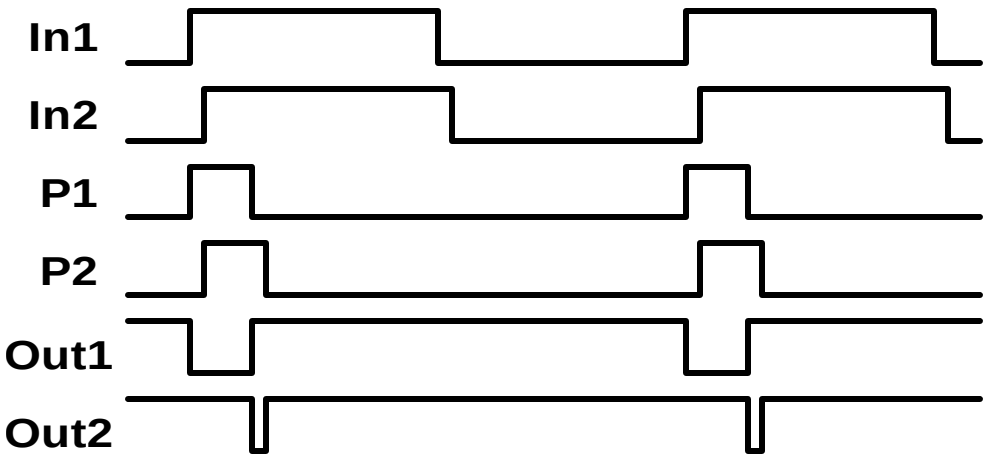
Nonlinear Error Summing

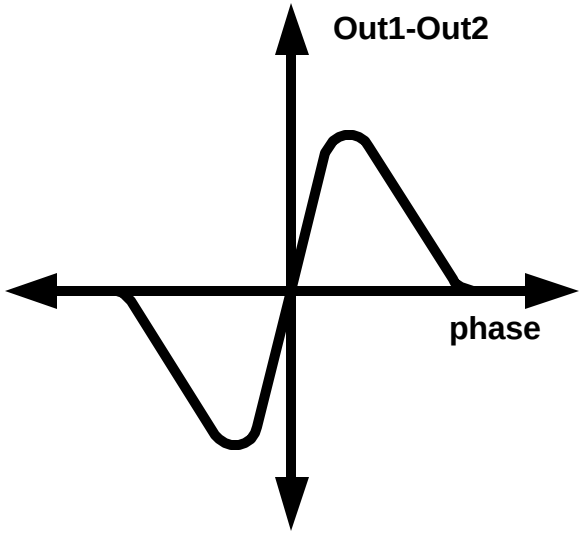


- n from geometry, $\theta_{crit} = 360/n$
- Nonlinearity makes modelocked states unstable

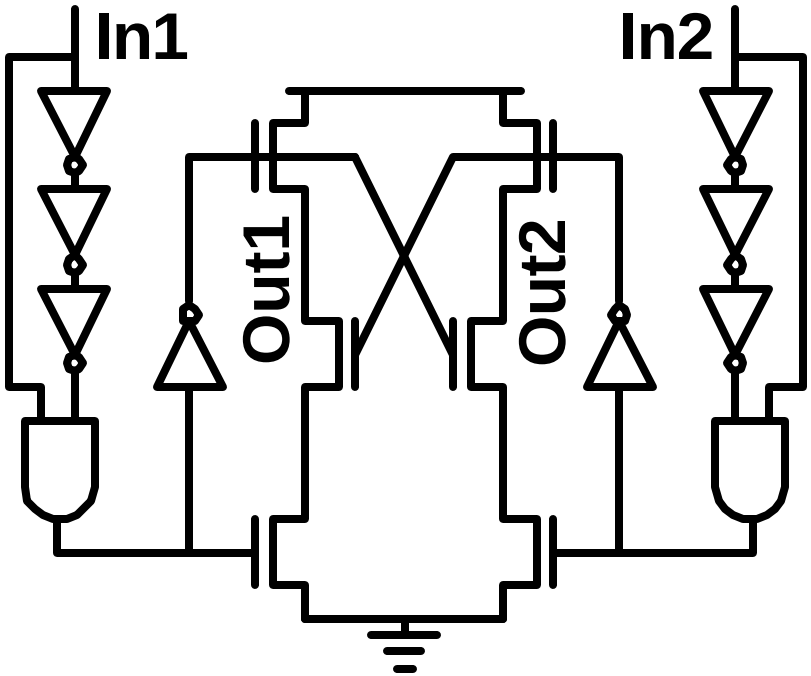
Phase Detector - phase

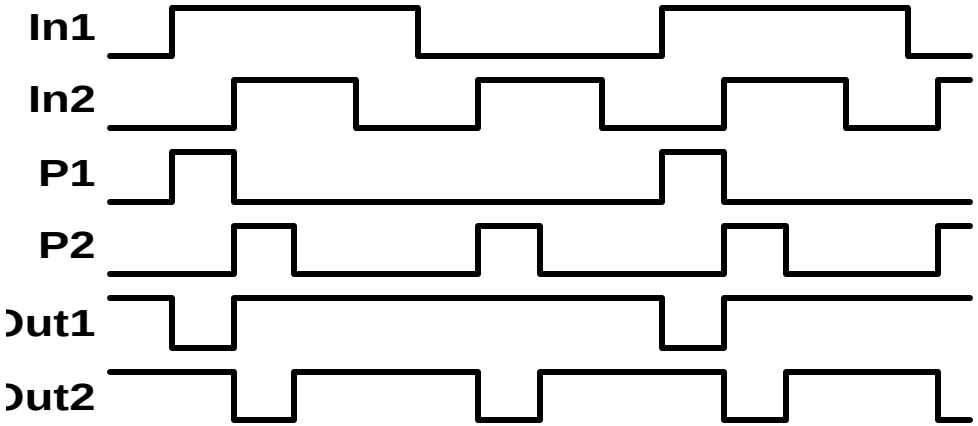


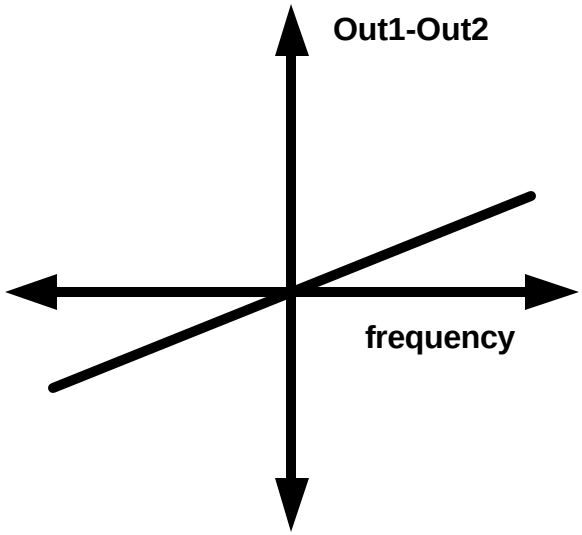




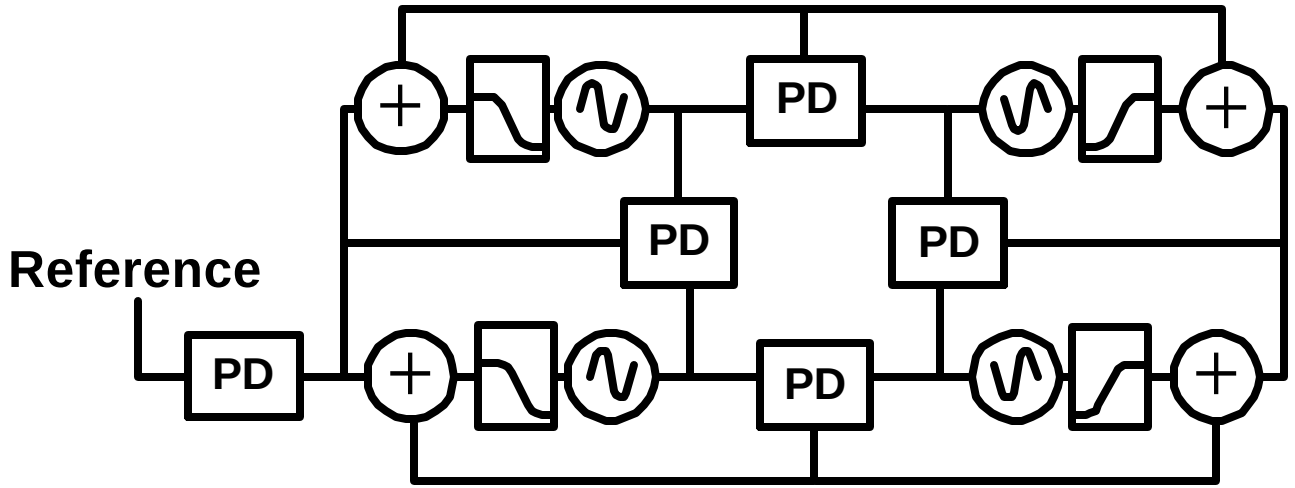
Phase Detector - frequency



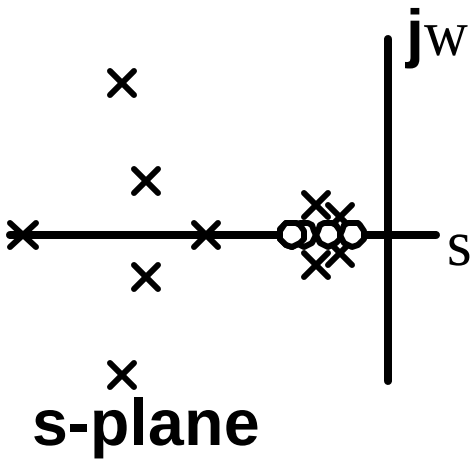


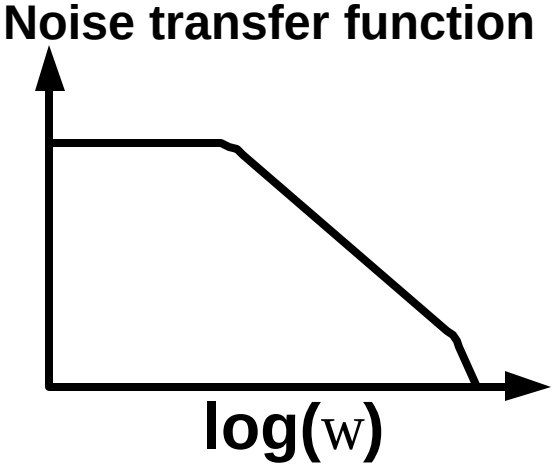


Small-Signal Stability

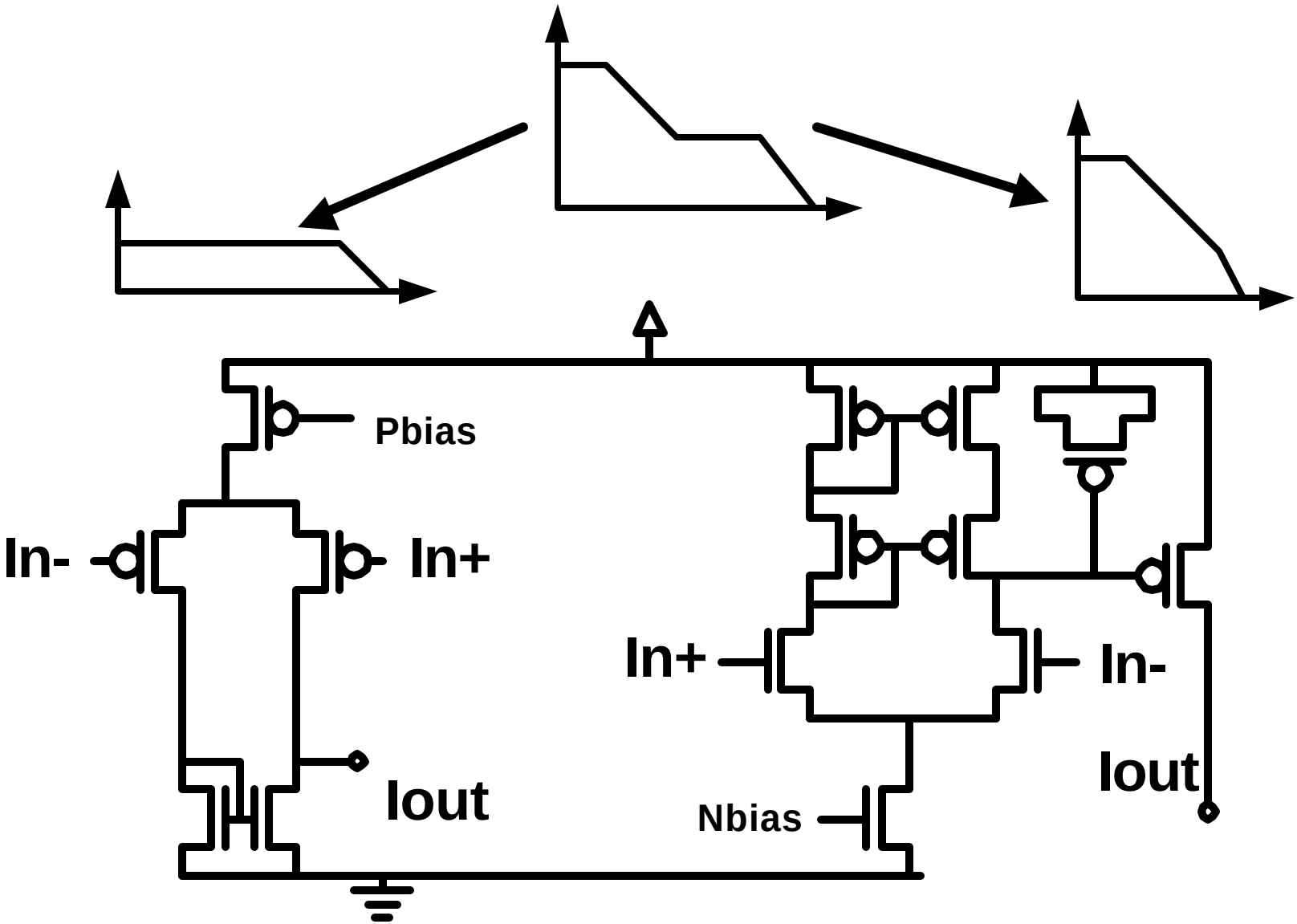


$$F = [s\mathbf{I} - \mathbf{A}_1\mathbf{A}_2\ h(s)]^{-1}\, h(s)\mathbf{A}_1\mathbf{u}$$

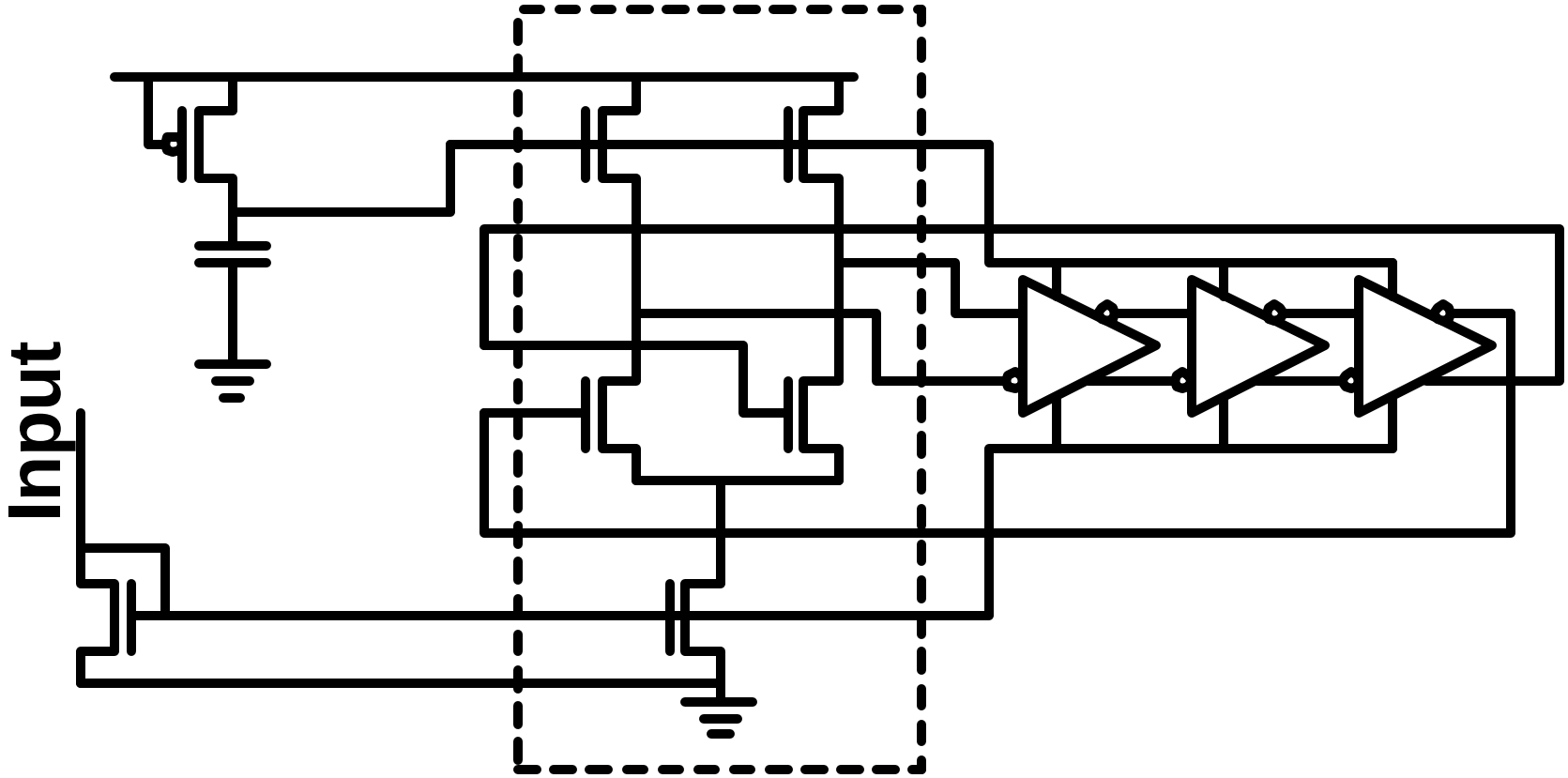




Loop Filter

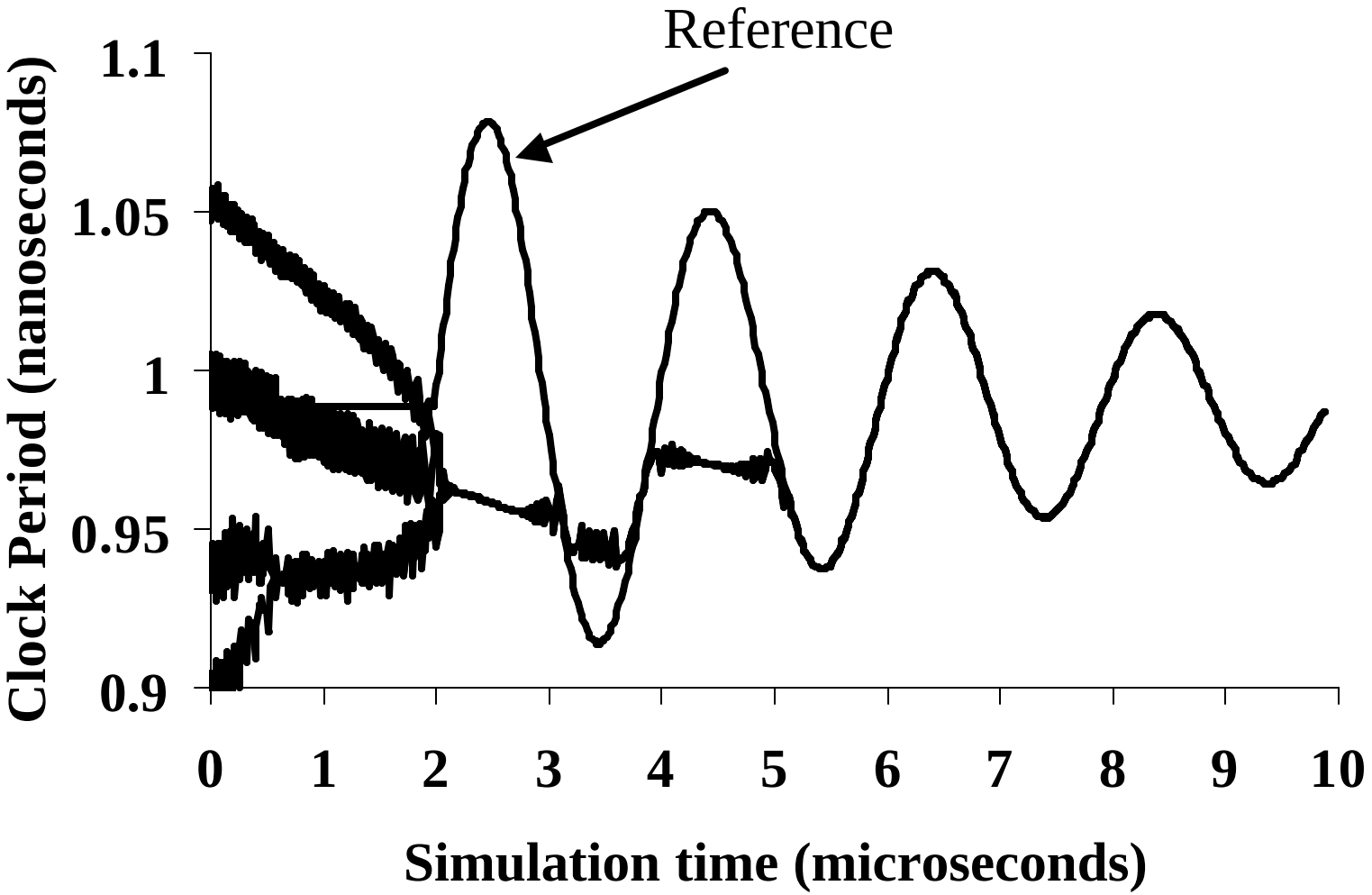


Oscillator

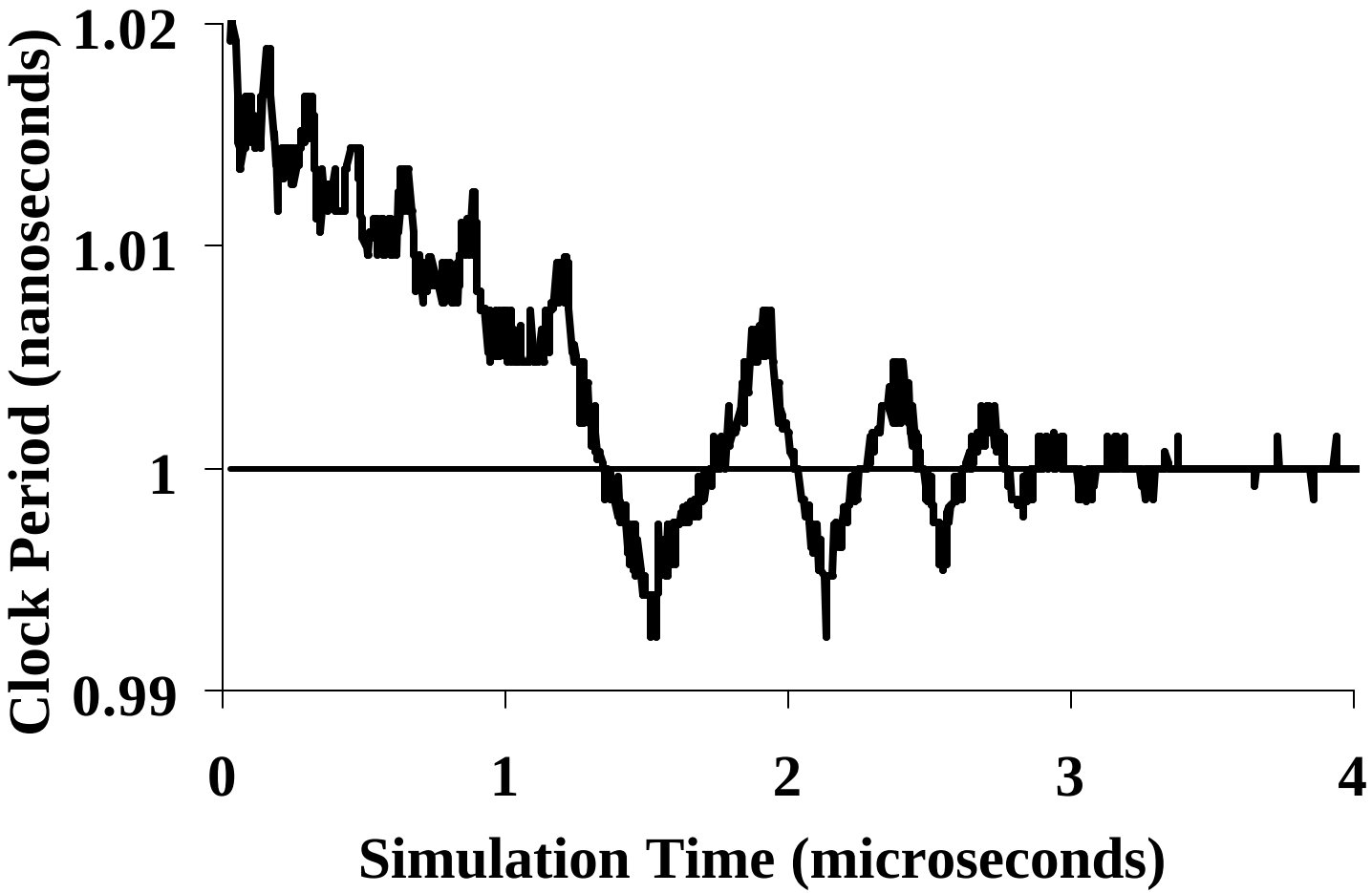


- NMOS-load differential ring oscillator insensitive to supply noise

Large-Signal Acquisition

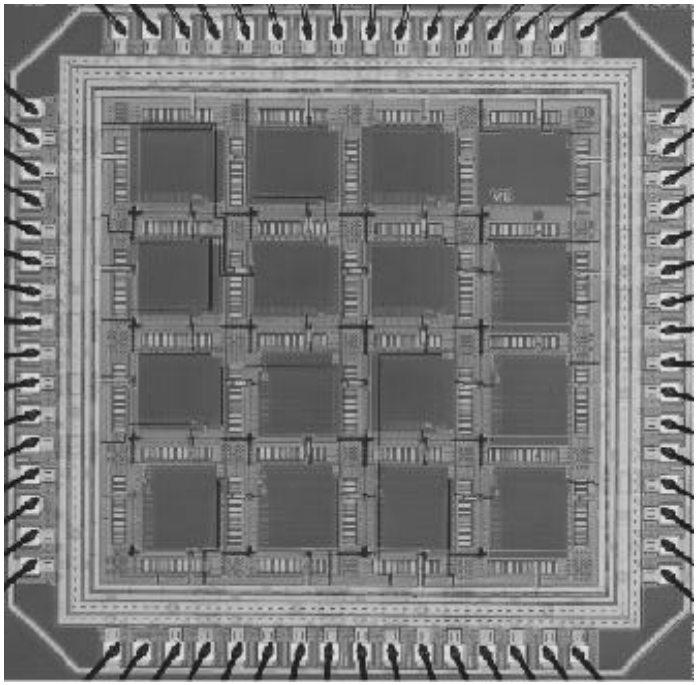


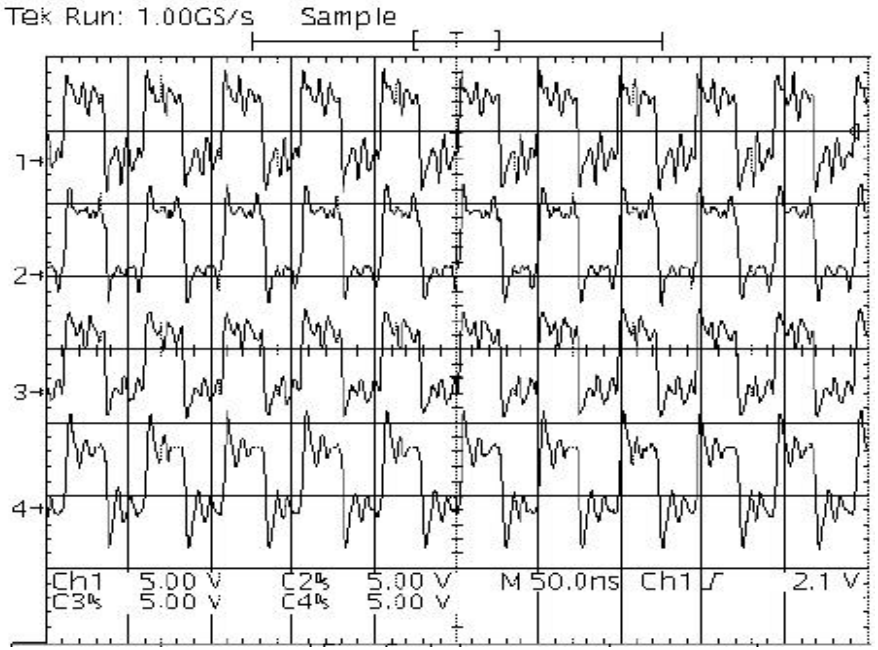
Full System Hspice Simulation



- 16 oscillator network small-signal stable

Results





- 2mm chip. 0.35 µm, single poly triple metal CMOS
- 16 oscillators, each 40µm x 40µm
- 24 phase detectors, each 20µm x 40µm
- Total power: 450mW at 3V, 1.3GHz
- Jitter < 30ps

Conclusions

- Random and time-varying mismatch limit centralized clock distribution
- Distributed generation enables shorter distribution
- Stable multiple-oscillator PLL demonstrated

Acknowledgements

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