Variation-Driven Device Sizing for Minimum Energy Sub-Threshold Circuits

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Outline

- Introduction
- Variation impact on sub-threshold functionality
- Constant-yield device sizing
- Minimum energy operating point with yield constraint
- Delay variability modeling
- Variability comparison

Previous Work

- Digital ICs in sub-threshold
  - C. Kim, H. Soeleman, K. Roy, Trans. VLSI 2003
  - A. Wang, A. Chandrakasan, ISSCC 2004
- Minimum energy point
  - B. Calhoun, A. Chandrakasan, ISLPED 2004
  - B. Zhai, D. Blaauw, D. Sylvester, K. Flautner, DAC 2004
- Variation in sub-threshold: analytical modeling
  - B. Zhai, S. Hanson, D. Blaauw, D. Sylvester, ISLPED 2005
  - J. Chen, L. Clark, Y. Cao, ICCD 2005
- Other approaches to mitigating variation, e.g.
  - Body biasing
  - Optimizing gate drive strengths to meet delay/yield constraints

Current and Variation in Sub-threshold

- **Sub-threshold current model**

$$I_{sub} = I_o e^{\frac{V_{GS} - V_T + \eta V_{DS}}{n V_{th}}} \left(1 - e^{\frac{-V_{DS}}{V_{th}}}\right)$$

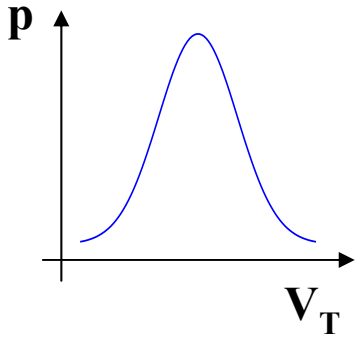
V_T = threshold voltage

η = DIBL coefficient

n = sub - threshold slope factor

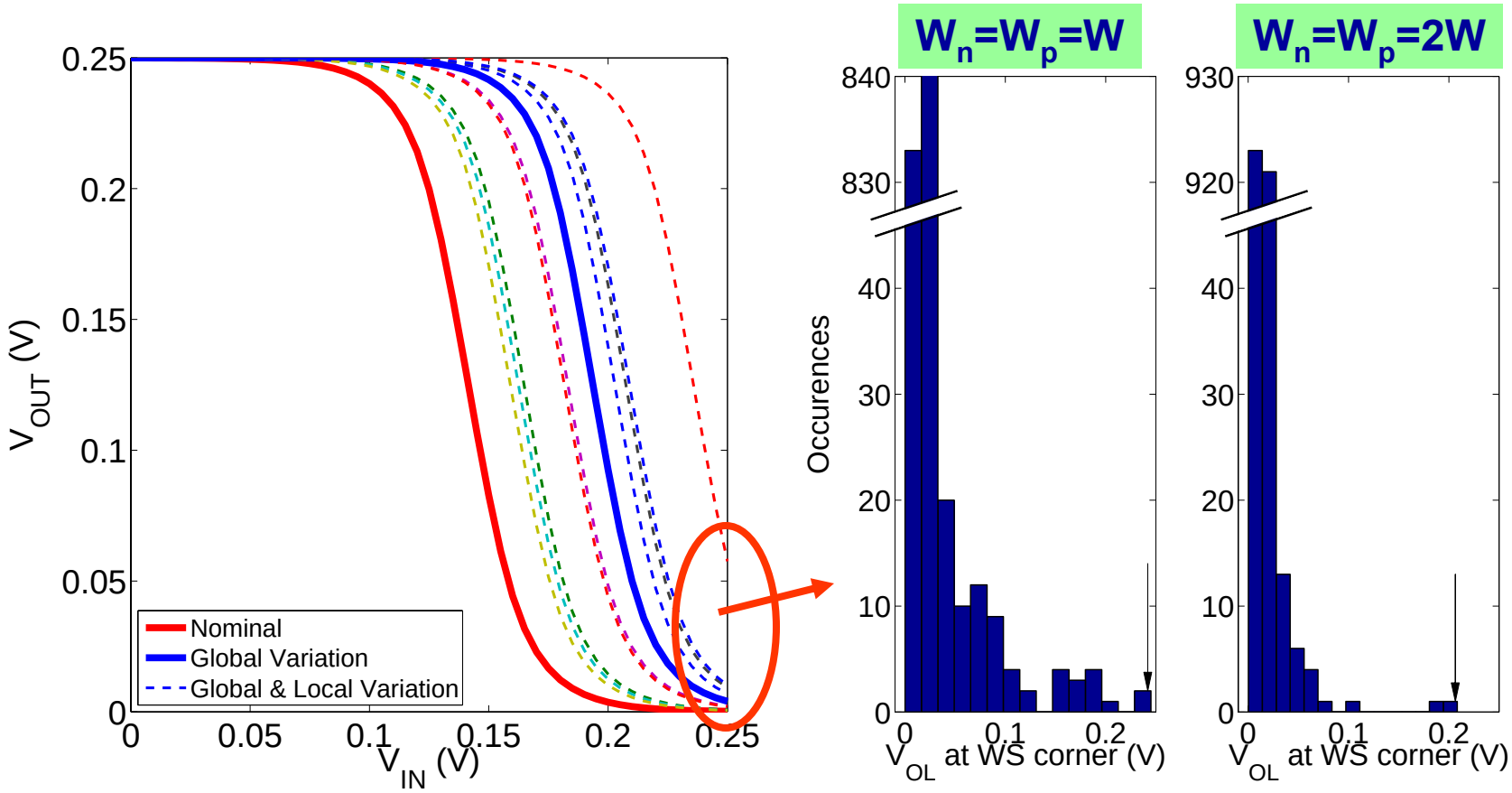
V_{th} = thermal voltage

- **Global (inter-die) variation**
  - **affects all devices on a die equally**
- **Local (intra-die) variation**
  - **affects devices on a die differently**
  - **random variation in L_{eff} and V_T**
  - **model V_T as having Gaussian distribution**



$$\sigma_{V_T} \propto \frac{1}{\sqrt{WL}}$$

Logic Gate Output Swing

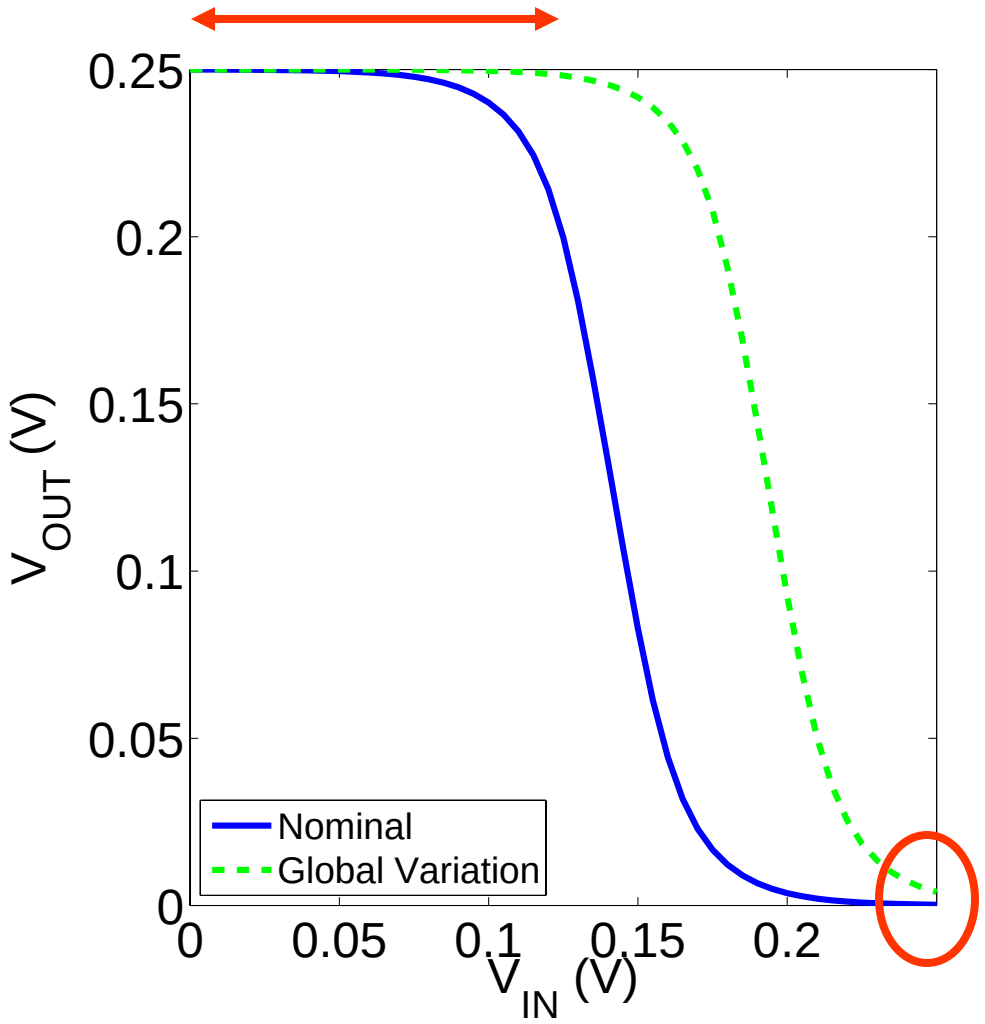


- V_T variation causes distribution of 'high' and 'low' voltage levels of a logic gate

What V_{OL}, V_{OH} levels are acceptable?

Output Swing Metrics

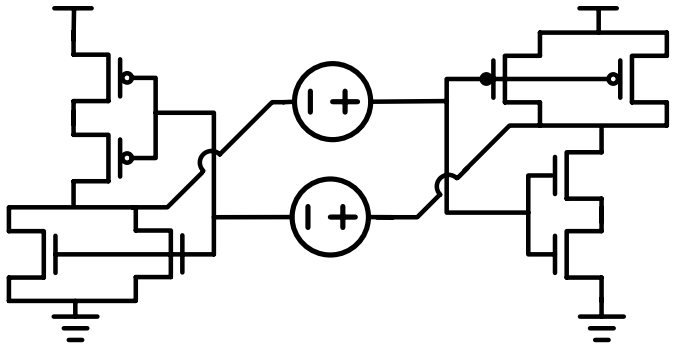
- Common criterion: impose fixed requirement, e.g. V_{OL} < 10% V_{DD}, V_{OH} > 90% V_{DD}
  - Does not scale well across global corners
  - V_{OL}, V_{OH} shift with global corner, but so does V_{IL}, V_{IH}



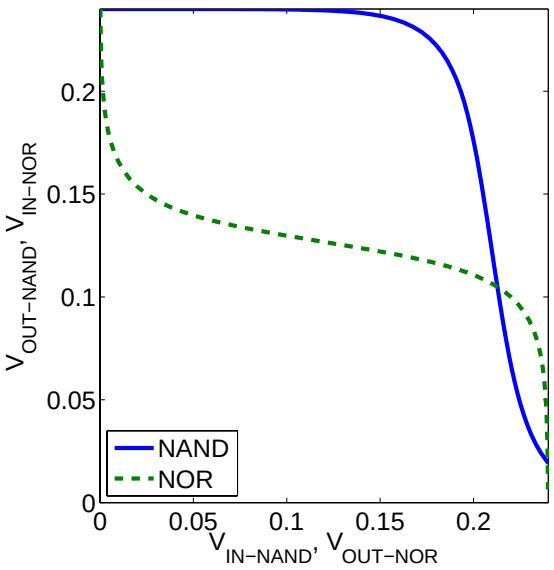
Output Swing Metrics

Proposed: Butterfly plots

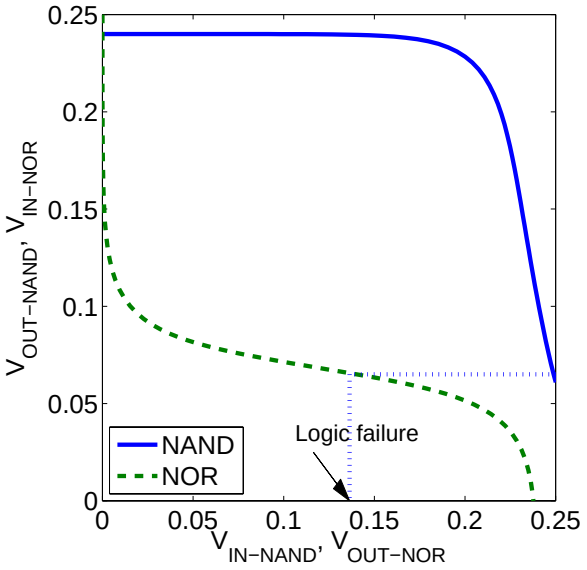
Simulation setup



No logic failure

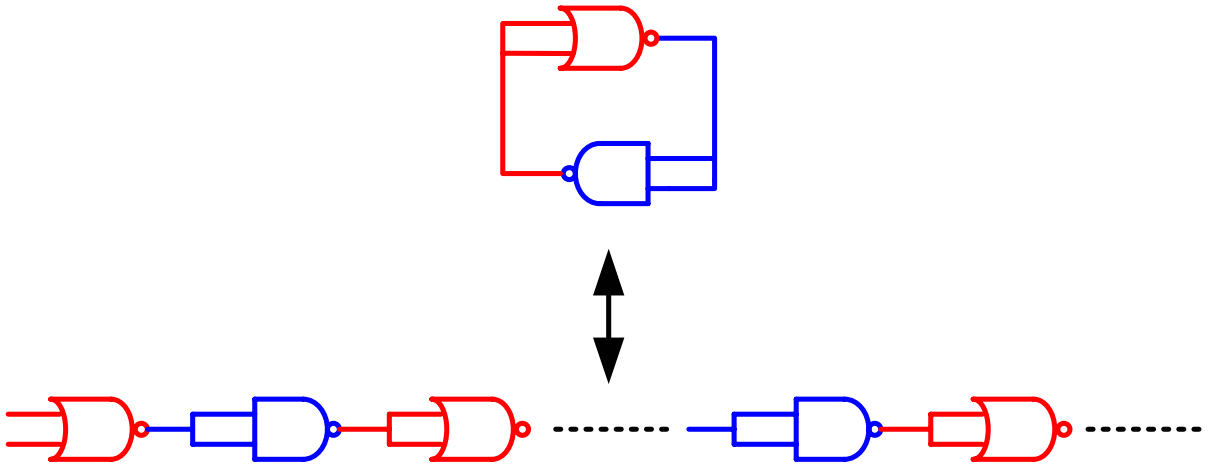


Logic failure



Modeling Limitation

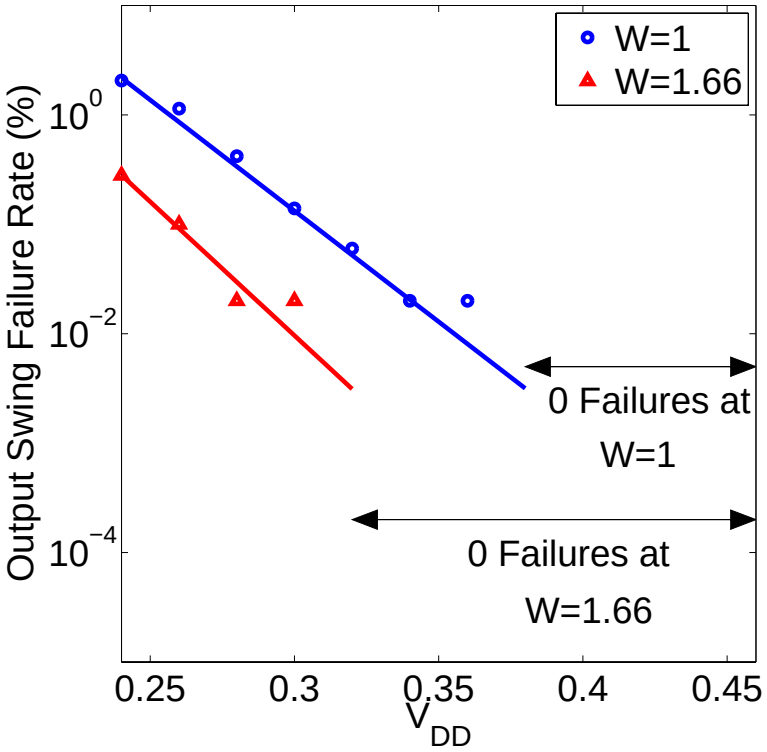
- Noise margin from butterfly plot = maximum noise that can be applied to all gates in an infinitely long chain
  - Lohstroh, Seevinck, de Groot, JSSC 1983

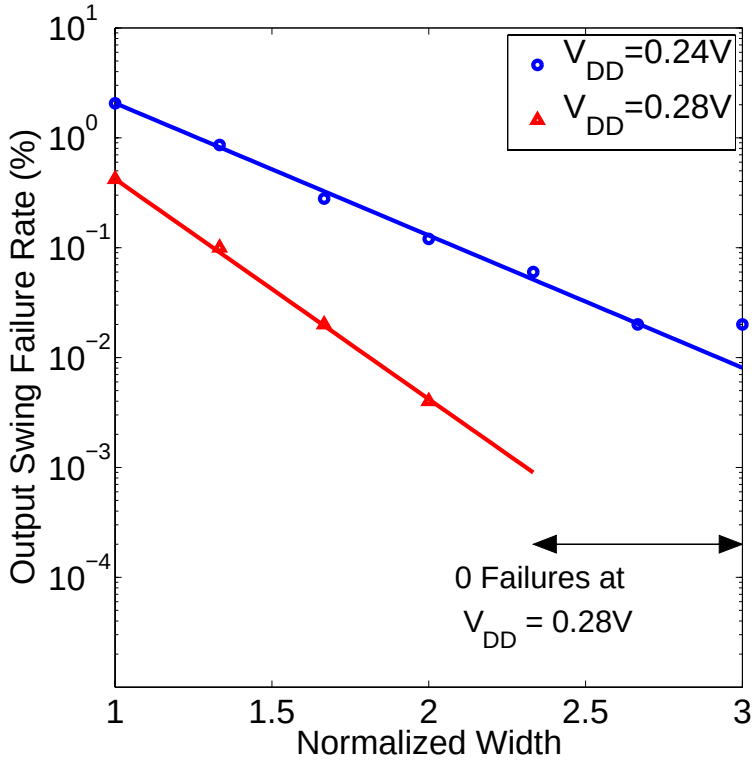


- Does not reflect exact mismatch conditions
- Provides a useful guideline for standard cell design when target circuit is unknown

Output Swing Failure Rate

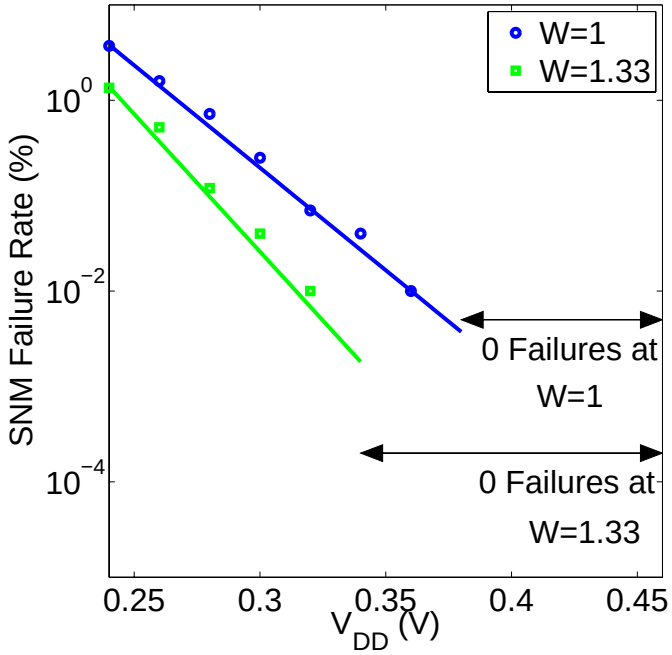
- Put logic gate under test back-to-back with:
  - NAND3 to check V_{OH}
  - NOR3 to check V_{OL}
- Define failure = no enclosed square in butterfly plots
- Failure rate decreases exponentially with device width and V_{DD}

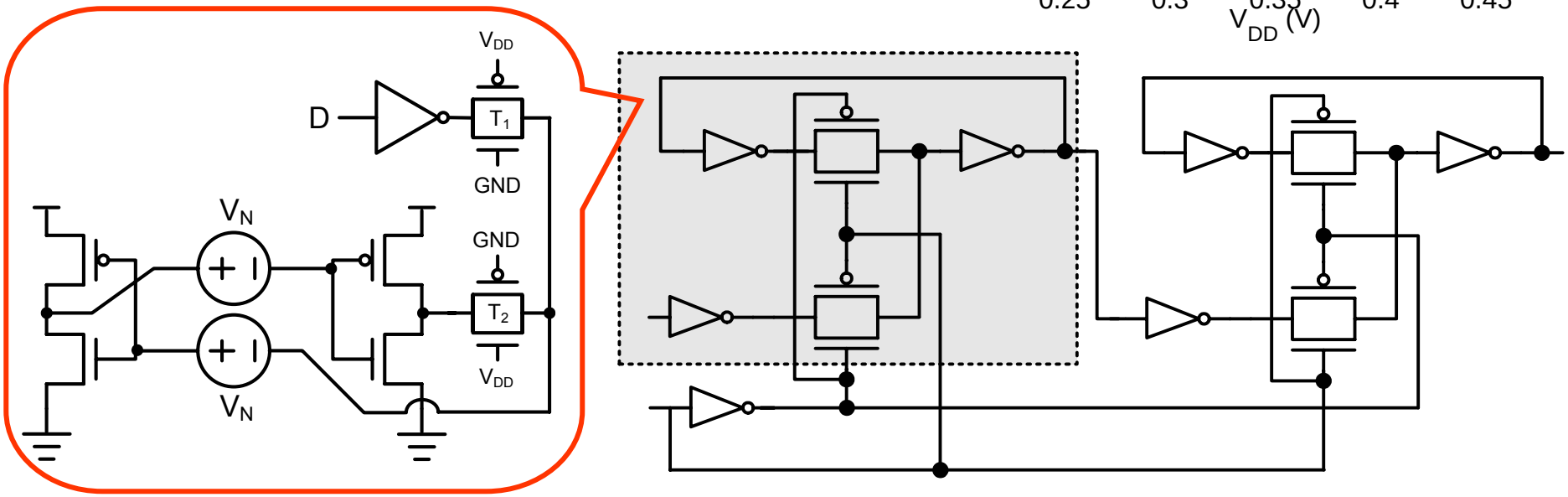




Noise Margin in Registers

- Concept of static noise margin also applicable to data retention in sub-V_T registers
- Failure rate due to negative SNM decreases exponentially with sizing and V_{DD}

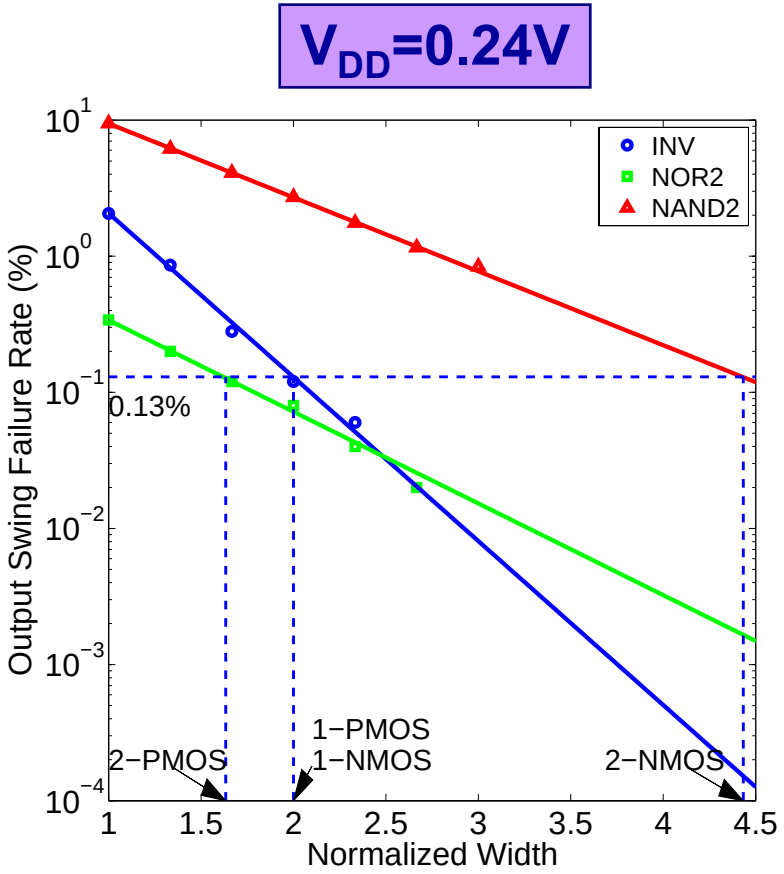




Constant-Yield Device Sizing

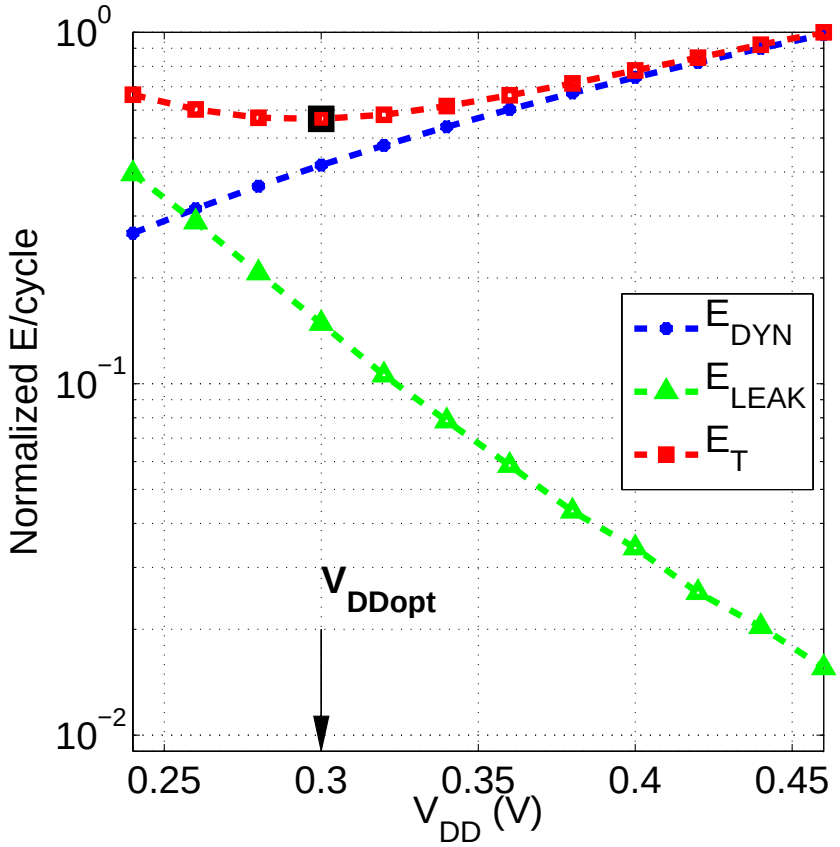
- Find failure rate vs. width plots for different circuit primitives
- Keep device sizes as small as possible, subject to yield constraint

V_{DD}(V)	0.24	0.26	0.28	0.30	0.32	0.34
1-NMOS	2	1.67	1.33	1	1	1
1-PMOS	2	1.67	1.33	1	1	1
2-NMOS	4.43	2.93	2.3	2.27	1.3	1
2-PMOS	1.63	1	1	1	1	1



Minimum Energy Operating Point

- Optimum V_{DD} to minimize energy/operation
- Assumes full functionality at all V_{DD}



$$E_T = E_{DYN} + E_L$$

$$E_{DYN} = C_{eff} V_{DD}^{\ 2}$$

$$E_L = W_{eff} I_{leak} V_{DD} t_d L_{DP}$$

Calhoun & Chandrakasan, "Characterizing and Modeling Minimum Energy Operation for Subthreshold Circuits," ISLPED, 2004

Energy/Variability Trade-off

- Functionality is no longer guaranteed in sub-threshold static CMOS at 65nm
- What if variation causes a circuit to have high failure rates at VDD_{opt}?
  - Need to increase transistor sizes or V_{DD} to mitigate variation
- Incorporate into minimum energy point analysis

Minimum Energy with Yield Constraint

Treat C_{eff}, W_{eff} as functions of V_{DD}

V_{DD}(V)	0.24	0.26	0.28	0.30	0.32	0.34
1-NMOS	2	1.67	1.33	1	1	1
1-PMOS	2	1.67	1.33	1	1	1
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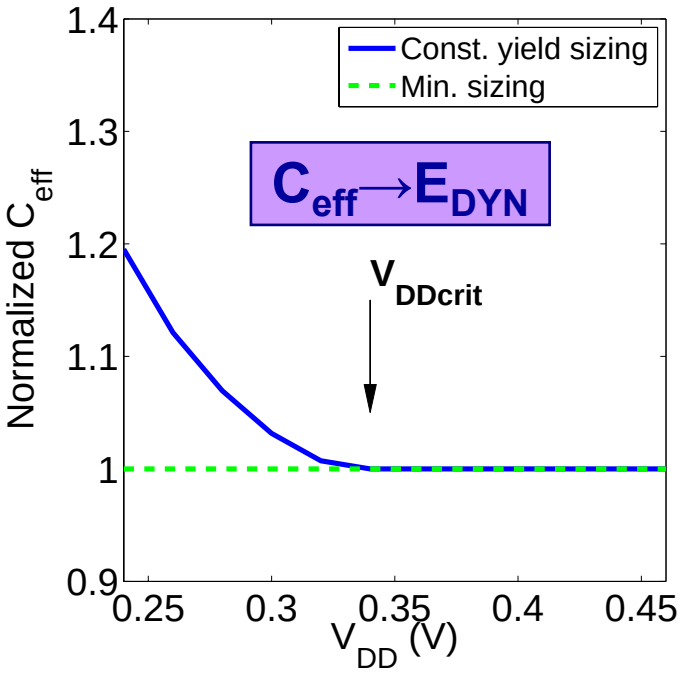
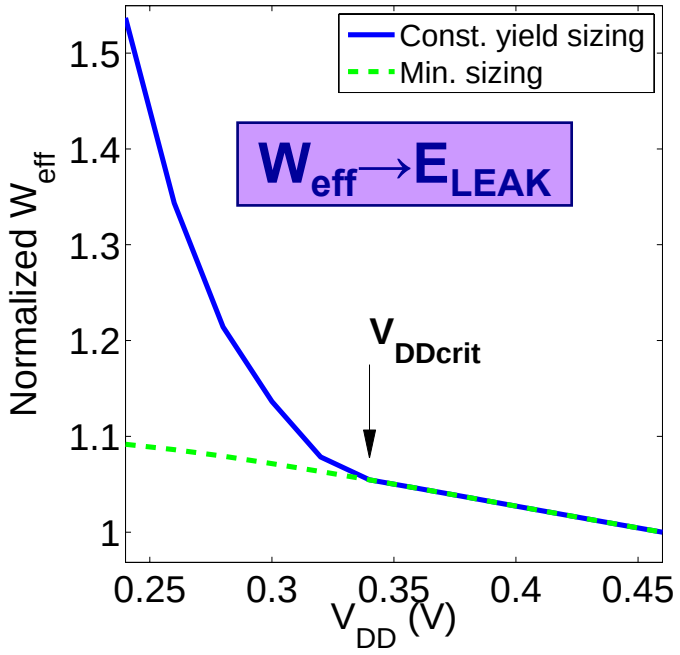
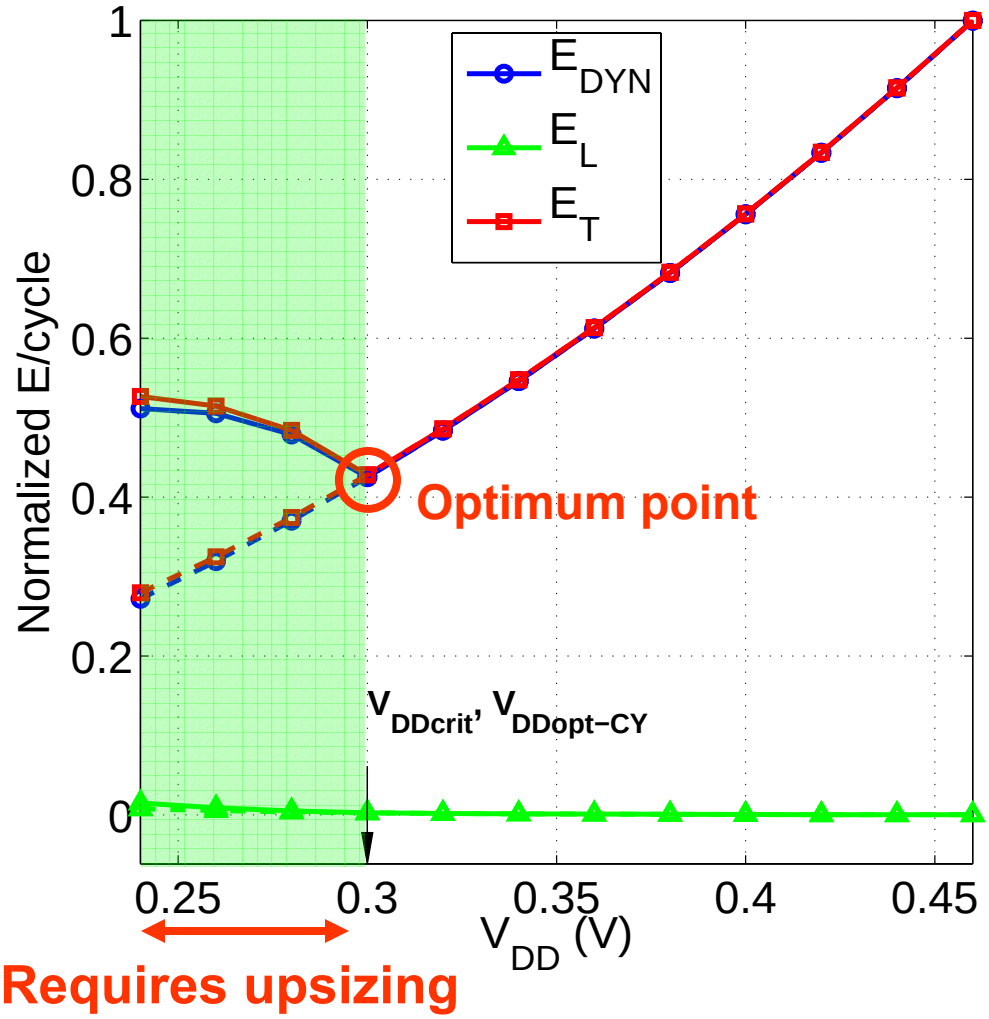




Minimum Energy with Yield Constraint

- Compare energy of inverter chain with minimum size and constant-yield sizing
- To meet yield constraint, must upsize below 0.3V
- Optimum: minimum size circuit at 0.3V

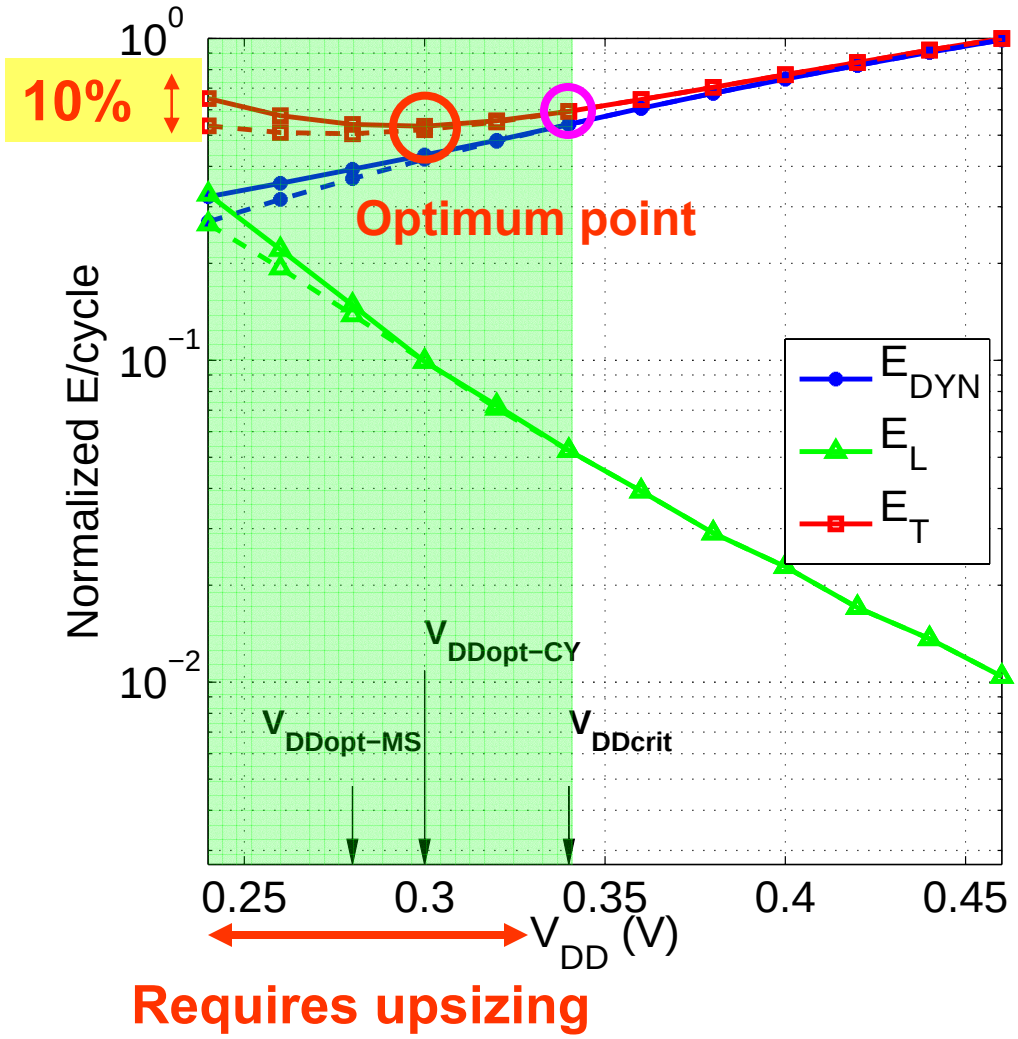
Example 1: 11-stage inverter chain



Minimum Energy with Yield Constraint

Example 2: 32-bit Kogge Stone Adder

- **Case 1: if min. size circuit reaches minimum energy before shaded area**
  - **no upsizing necessary**
- **Case 2: if min. size circuit has minimum point within shaded area**
  - **upsize to achieve minimum energy while satisfying yield constraint**



Delay Variability

- Active current, delay both lognormally distributed
- Measure of variability: coefficient of variation σ/μ
- σ/μ depends on σ_{VT} (local variation) and n (sub-threshold slope factor)

$$t_d = \frac{KC_g V_{DD}}{I_o e^{\frac{V_{GS}-V_T}{nV_{th}}}}$$

$$\frac{\sigma_{t_d}}{\mu_{t_d}} = \sqrt{e^{(\frac{\sigma_{V_T}}{nV_{th}})^2} - 1}$$

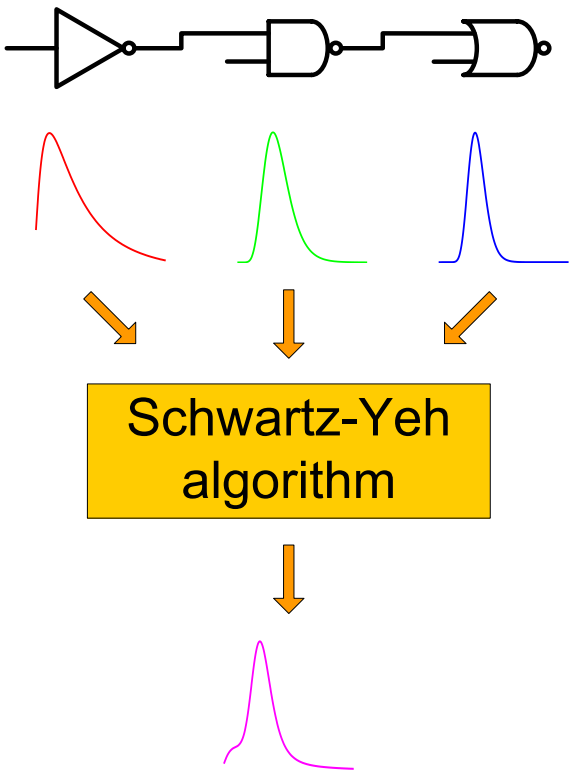
Delay Variability

- Approximate σ/μ as independent of input slew or output capacitance
- Pre-characterize σ/μ of each logic gate under one set of conditions
- Find μ_{actual} of logic gate in critical path
- Relation gives σ_{actual}

$$\frac{\sigma_{actual}}{\mu_{actual}} = \frac{\sigma_{pre-char}}{\mu_{pre-char}}$$

Delay Variability

- σ_{actual}, μ_{actual} characterize delay distribution through each logic gate
- Use Schwartz-Yeh algorithm to sum non-identical delay distributions



Schwartz & Yeh, "On the Distribution Function and Moments of Power Sums with Log-Normal Components," Bell Sys. Tech. Journal, 1982

Modeling Results

Model/Simulation Comparison

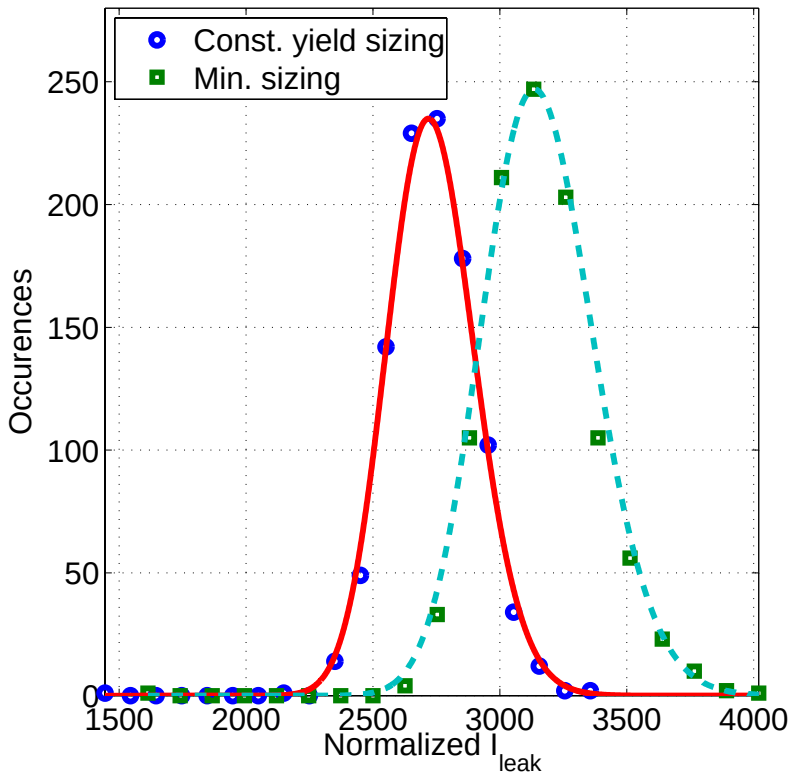
	Model	Monte Carlo	% Difference
μ	36.52	37.13	1.65
σ	7.038	7.262	3.09

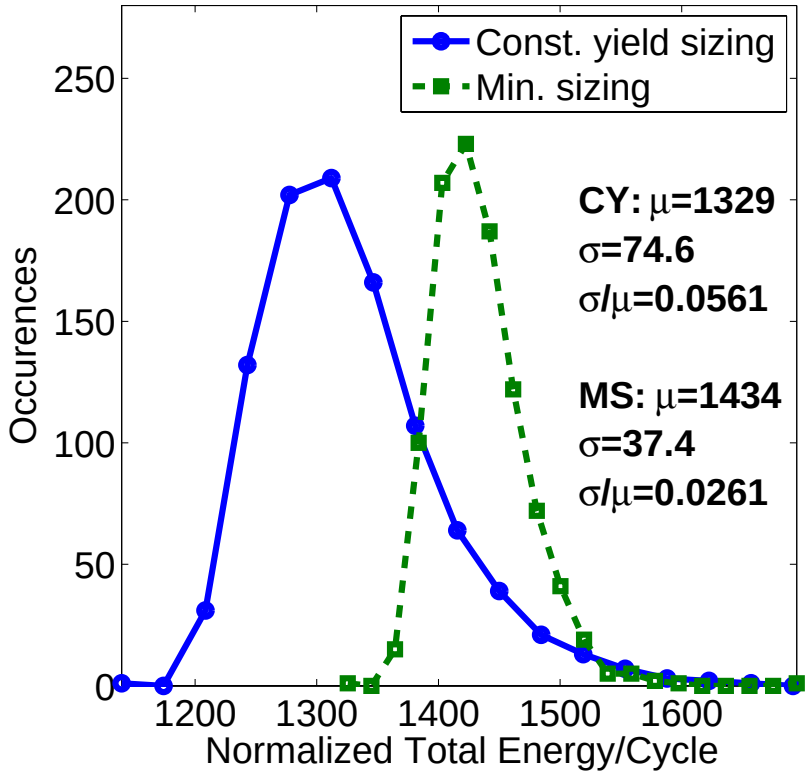
32-bit Kogge Stone Adder Delay (Normalized to FO4 at 0.3V)

	Constant Yield Sizing	Minimum Sizing
μ	90.88	44.92
σ	17.46	8.857
σ/μ	0.1921	0.1972

Energy Variability

- Given the same yield constraint:
  - Upsized adder has smaller mean leakage current and total energy
  - Min. size adder has smaller energy spread





Conclusions

- Local V_T variation: functionality no longer guaranteed in sub-threshold static CMOS
- Sizing methodology for constant functional yield
- Trade-off between energy and variability
- Given a yield constraint, upsizing can provide energy savings without compromising delay variability

- Analysis used to design an 8-tap, 16-bit FIR filter in 65nm
- Fabricated chip is verified to function at V_{DD} = 0.3V