A 65nm Sub-V_t Microcontroller with Integrated SRAM and Switched-Capacitor DC-DC Converter

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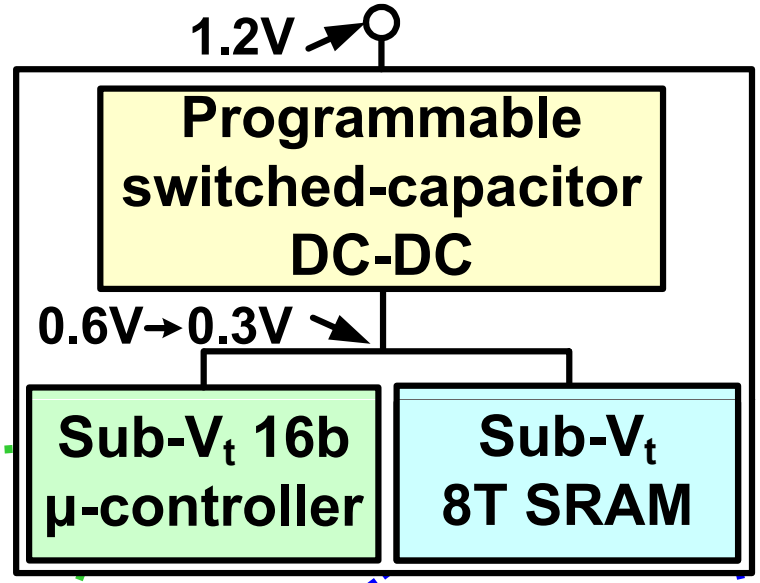
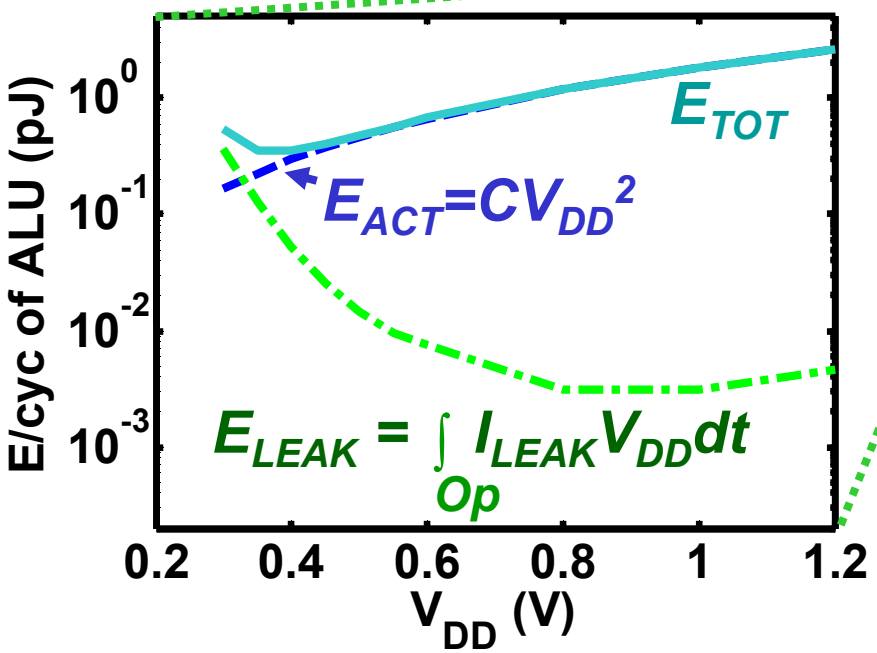
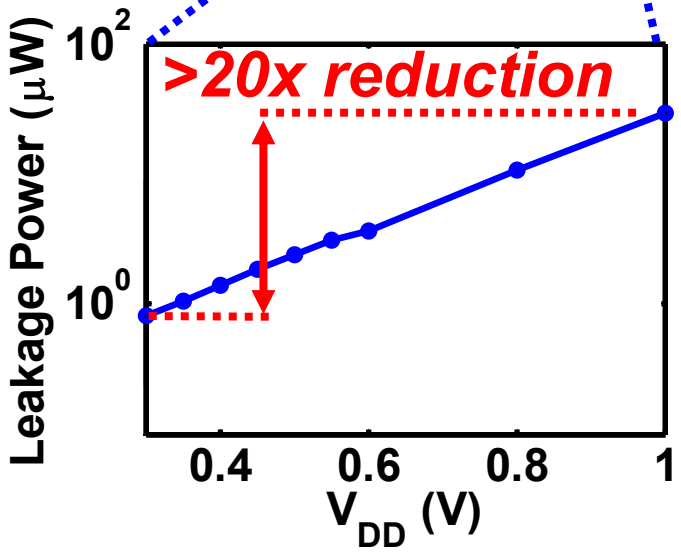
ISSCC 2008

Motivation

Voltage scaling enables drastic energy and power reduction in sub-V_t SoC





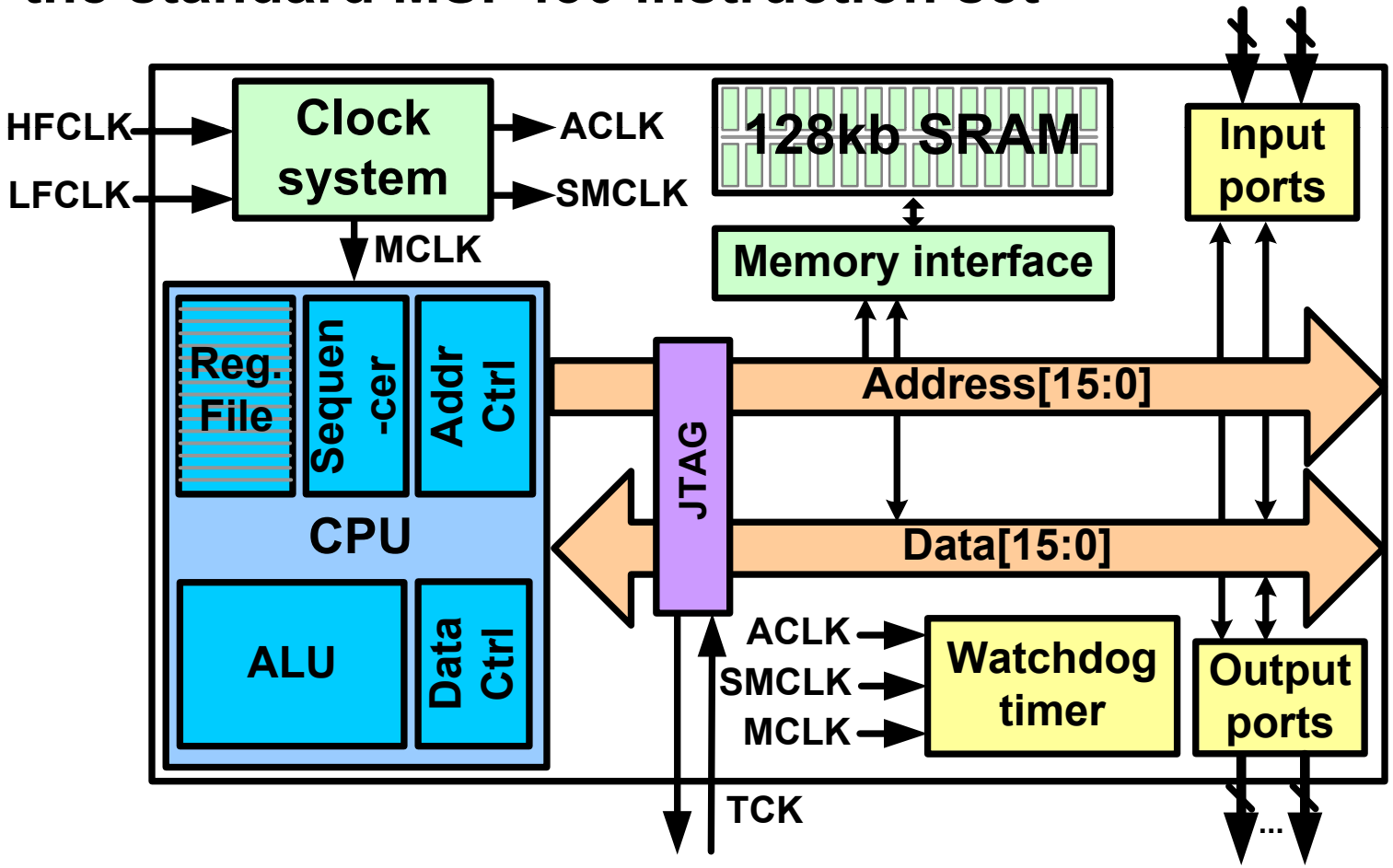


Outline

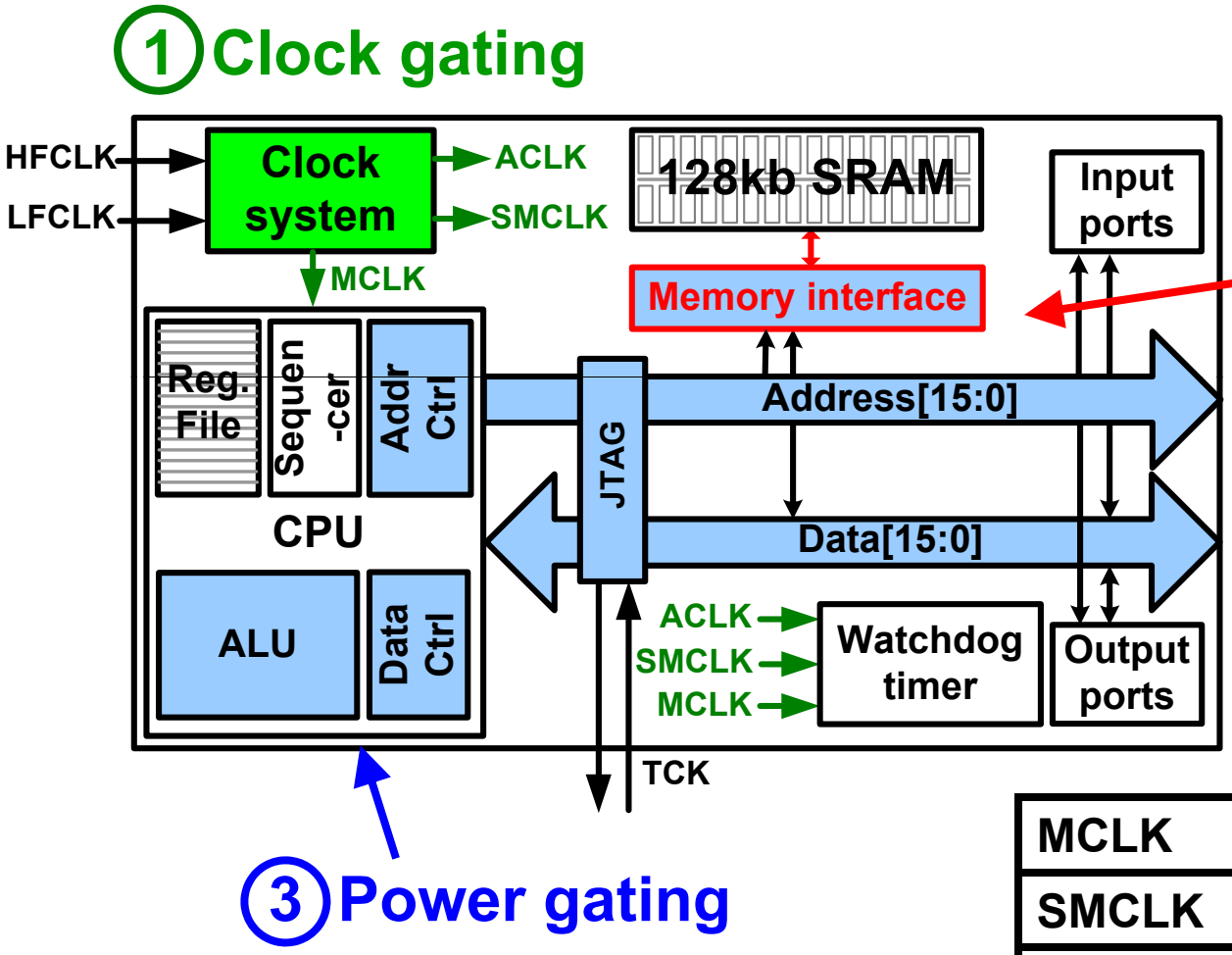
- Logic design challenges
- SRAM design challenges
- Timing verification
- DC-DC converter
- Prototype measurements
- Conclusions

Sub-V_t Microcontroller

- 16-bit RISC architecture
- Supports 27 instructions and 7 addressing modes of the standard MSP430 instruction set



Power Management Features

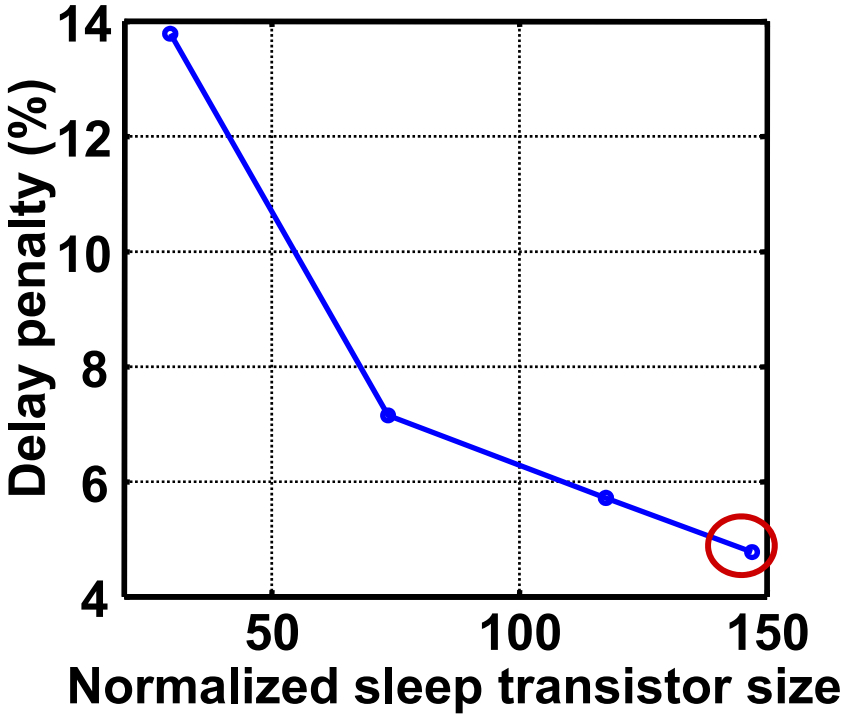


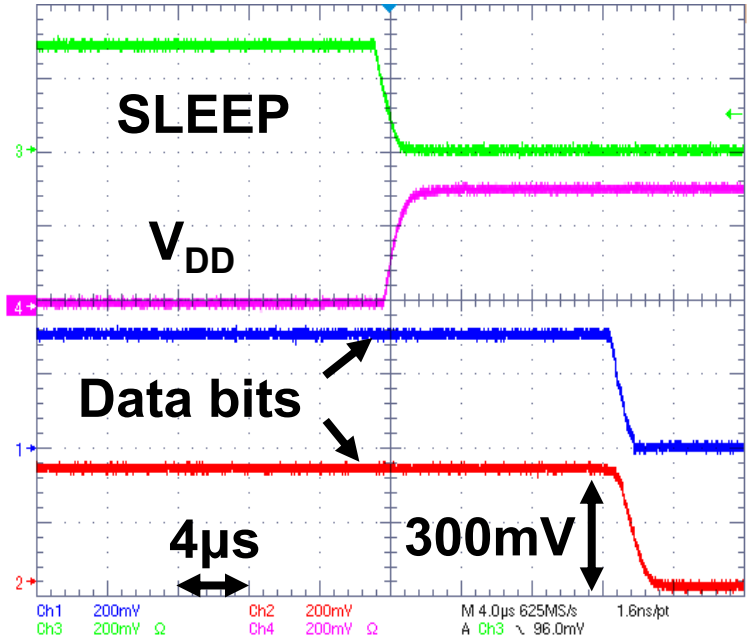
Low Power Modes

	LPM0	LPM2	LPM4
MCLK	OFF	OFF	OFF
SMCLK	ON	OFF	OFF
ACLK	ON	ON	OFF
Sleep Transistor	ON	ON	OFF

Power Gating

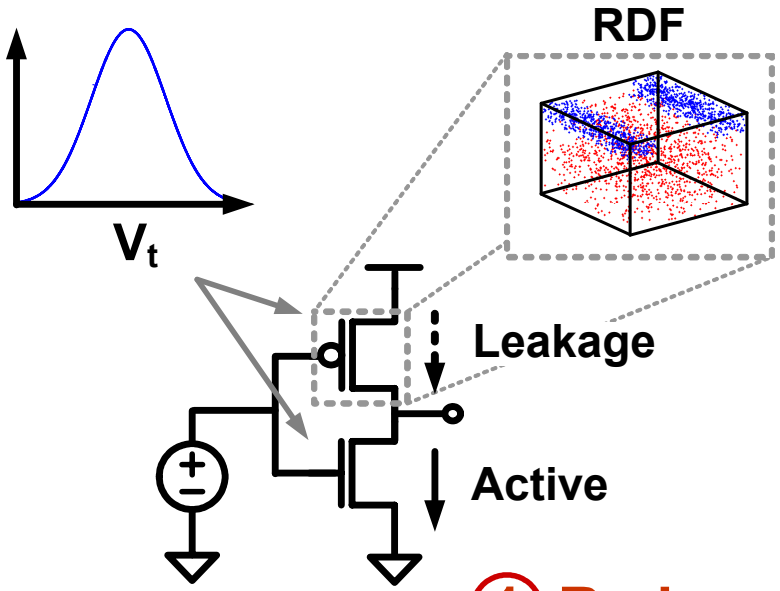
- On-chip PMOS sleep transistor
  - Sized for 5% delay penalty at 300mV
  - $E_{overhead} = \Delta P_{leakage} T_{breakeven}$, $T_{breakeven} \approx 77\mu s$

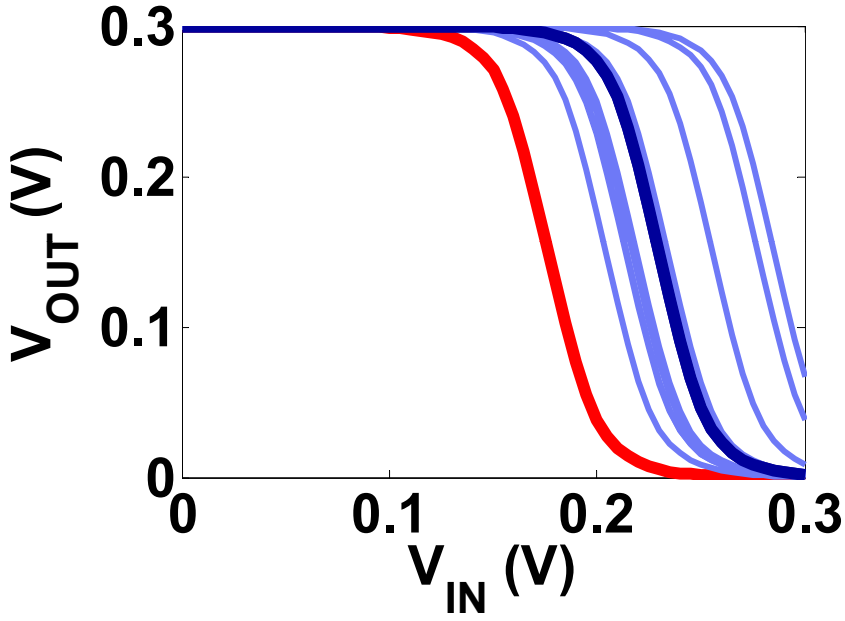




Sub-V_t Design Challenges

② Process variation



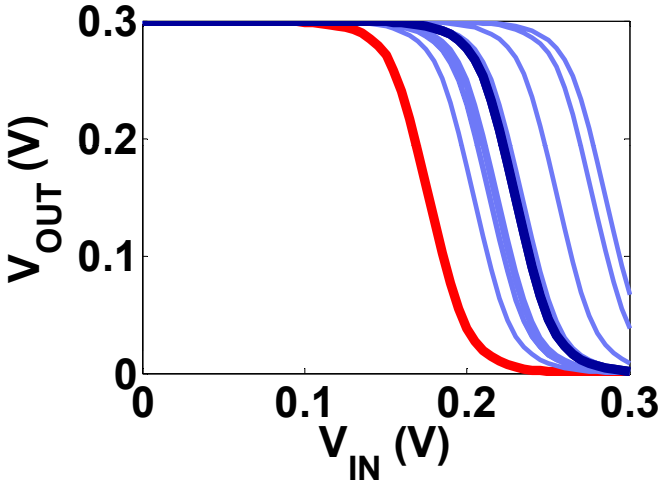


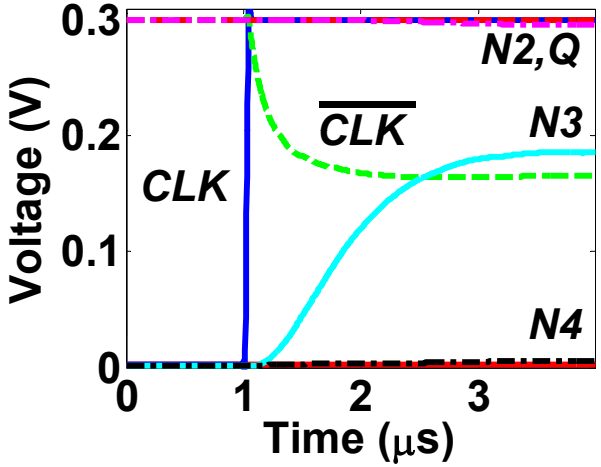
① Reduced I_{on}/I_{off}

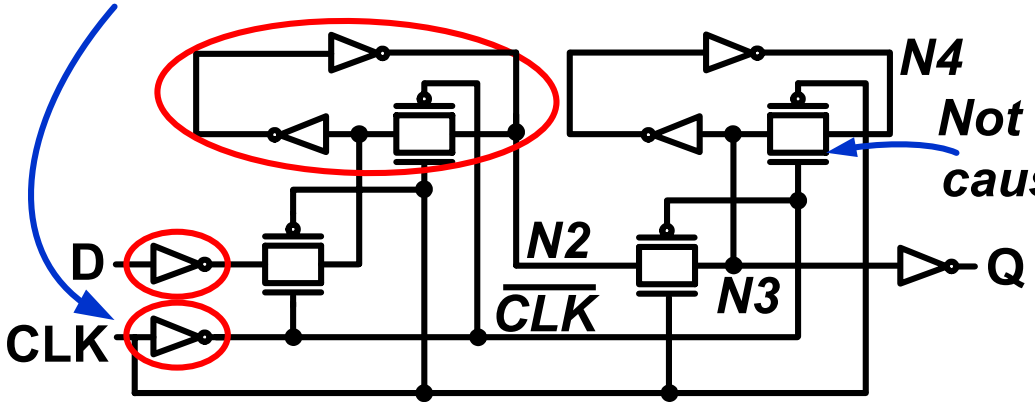
Sub-V_t static CMOS gates exhibit variation in logic levels (V_{OH}, V_{OL})

Sub-V_t Logic Functionality

Degraded logic levels adversely impact functionality

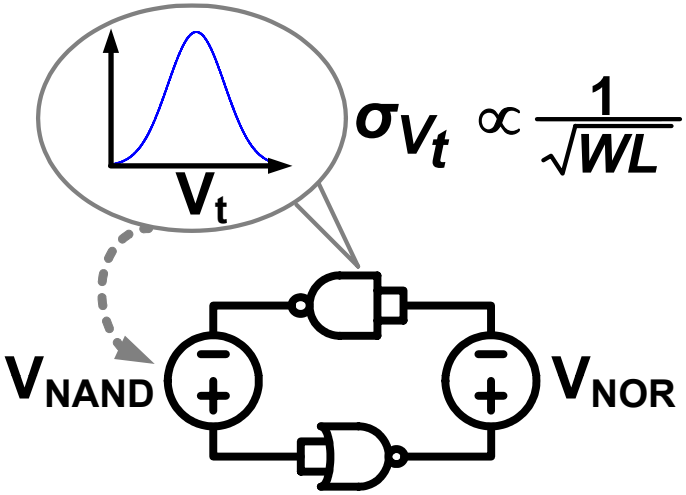


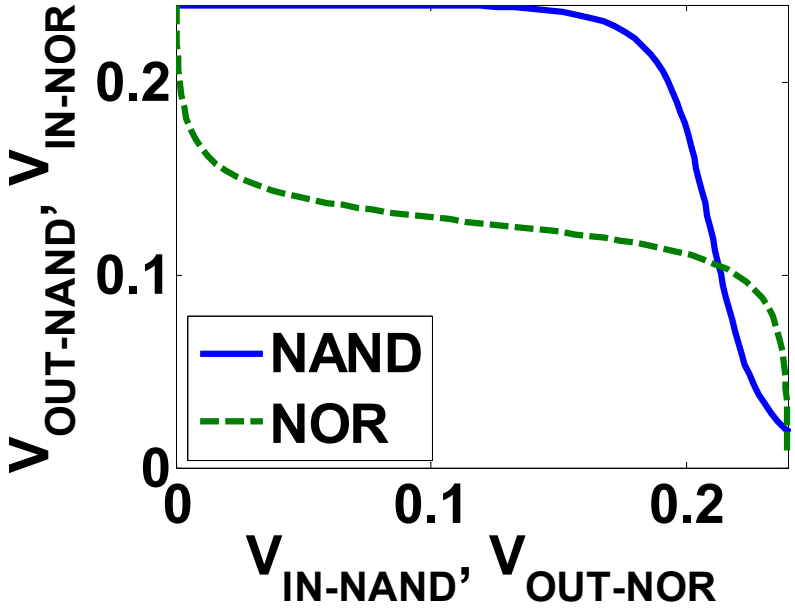


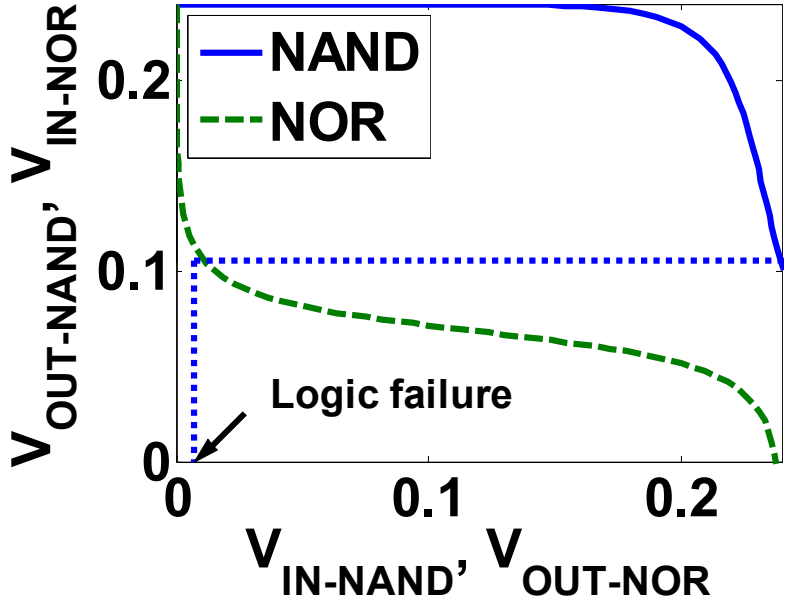


Sub-V_t Logic Design

Functional metric necessary to manage sizing trade-off

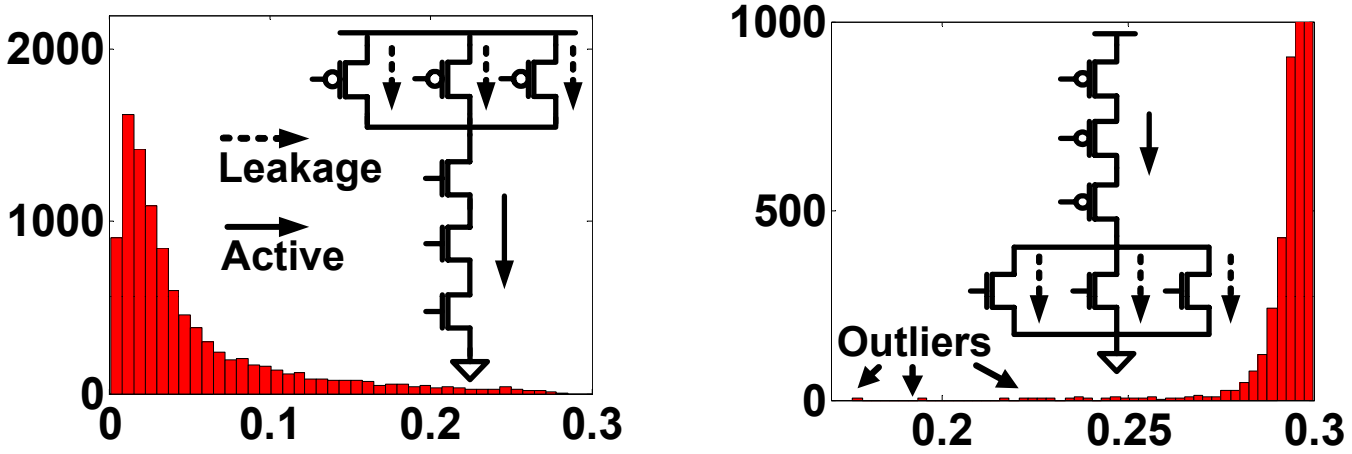




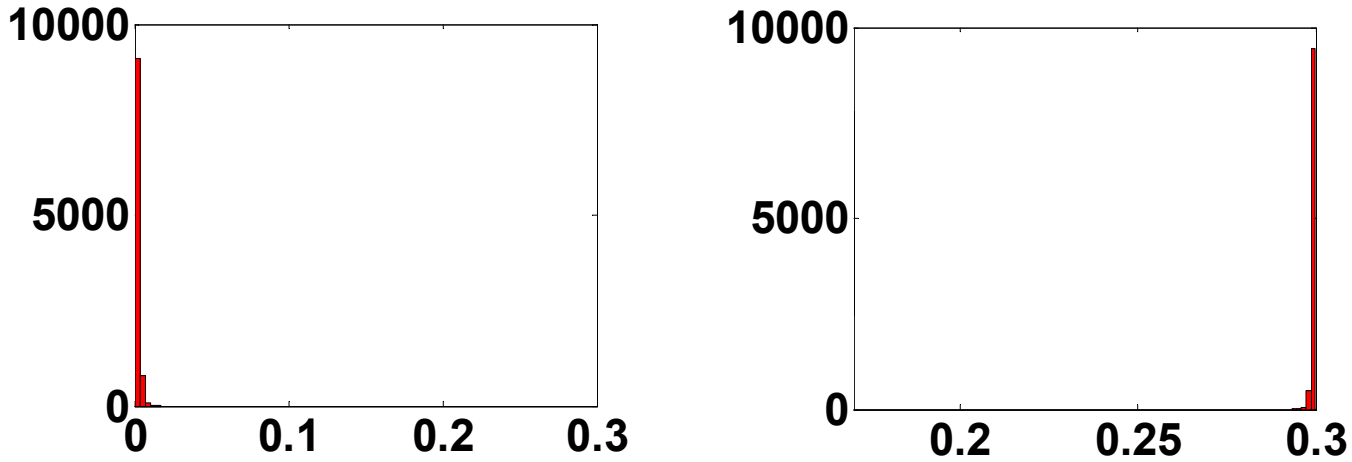


Sub-V_t Standard Cell Library

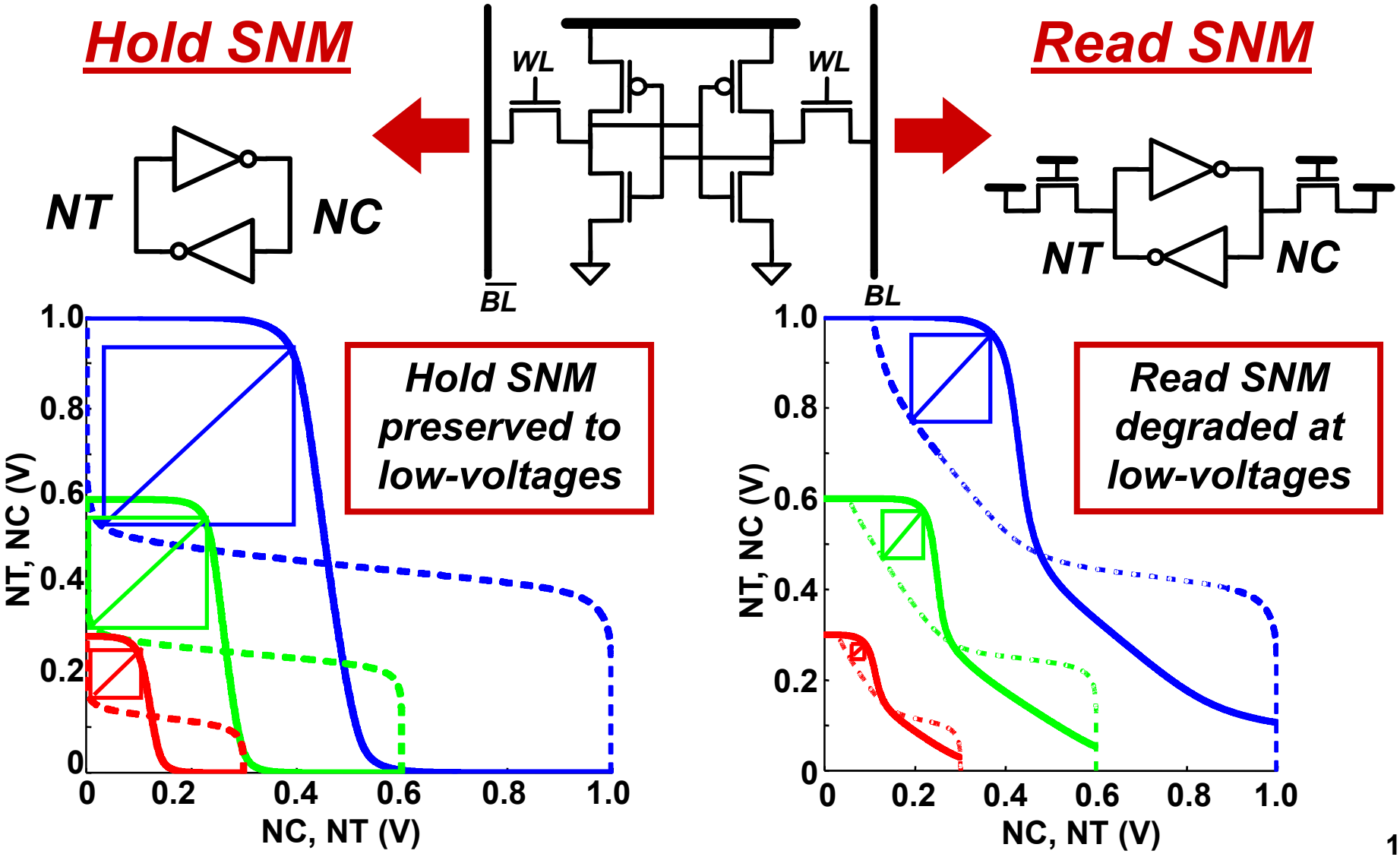
Above-V_t Library @ 0.3V



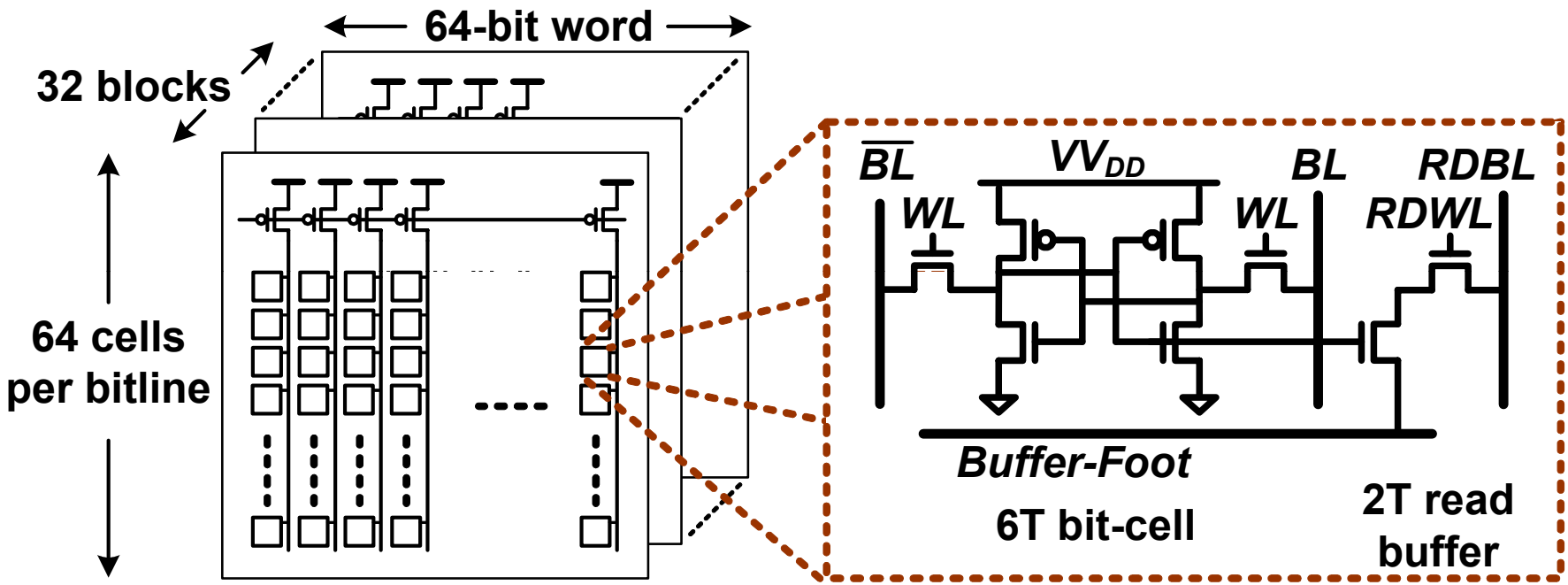
Sub-V_t Library @ 0.3V



Sub-V_t SRAM Challenges



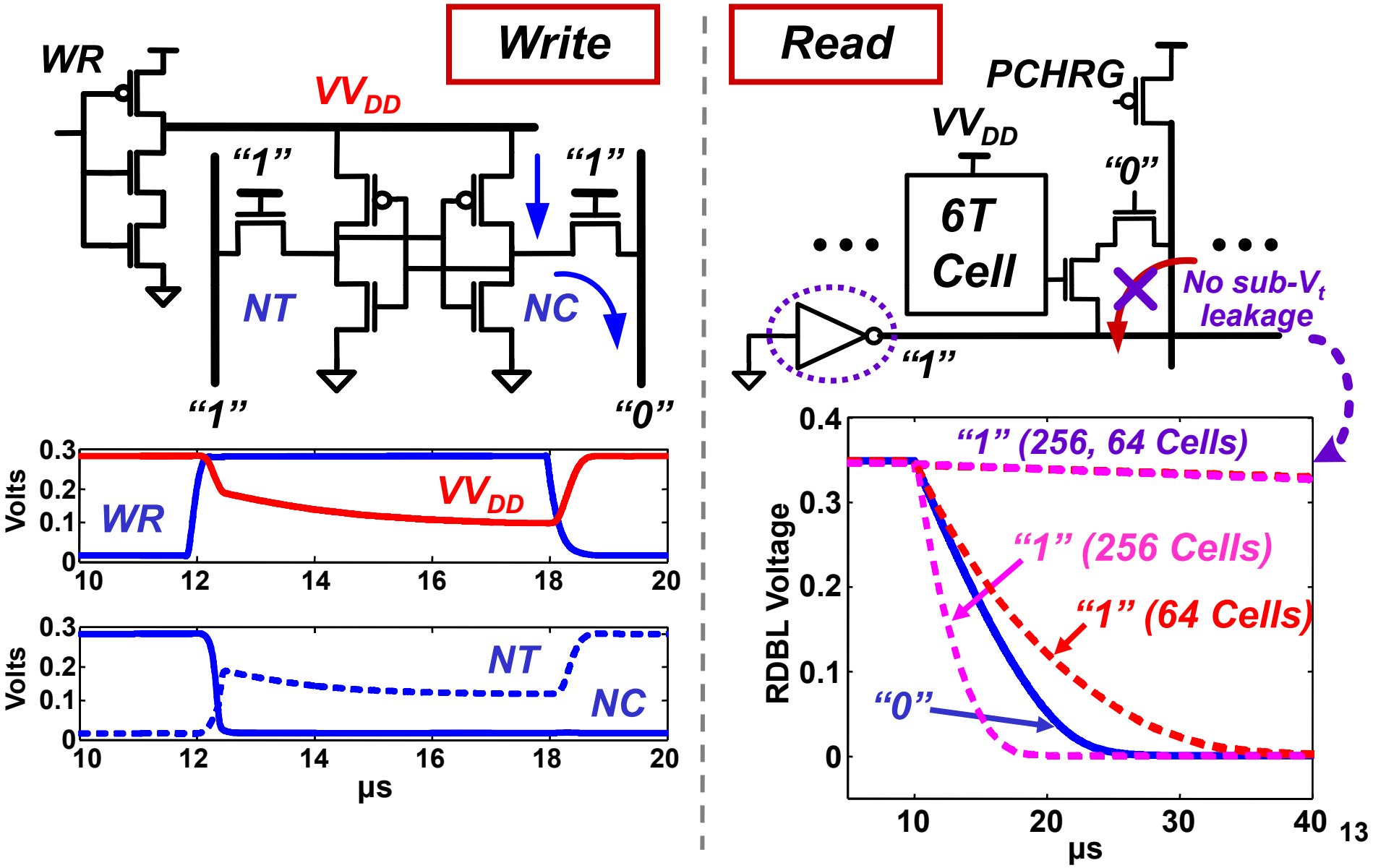
SRAM Architecture and Bit-Cell



Based on Verma, ISSCC 2007

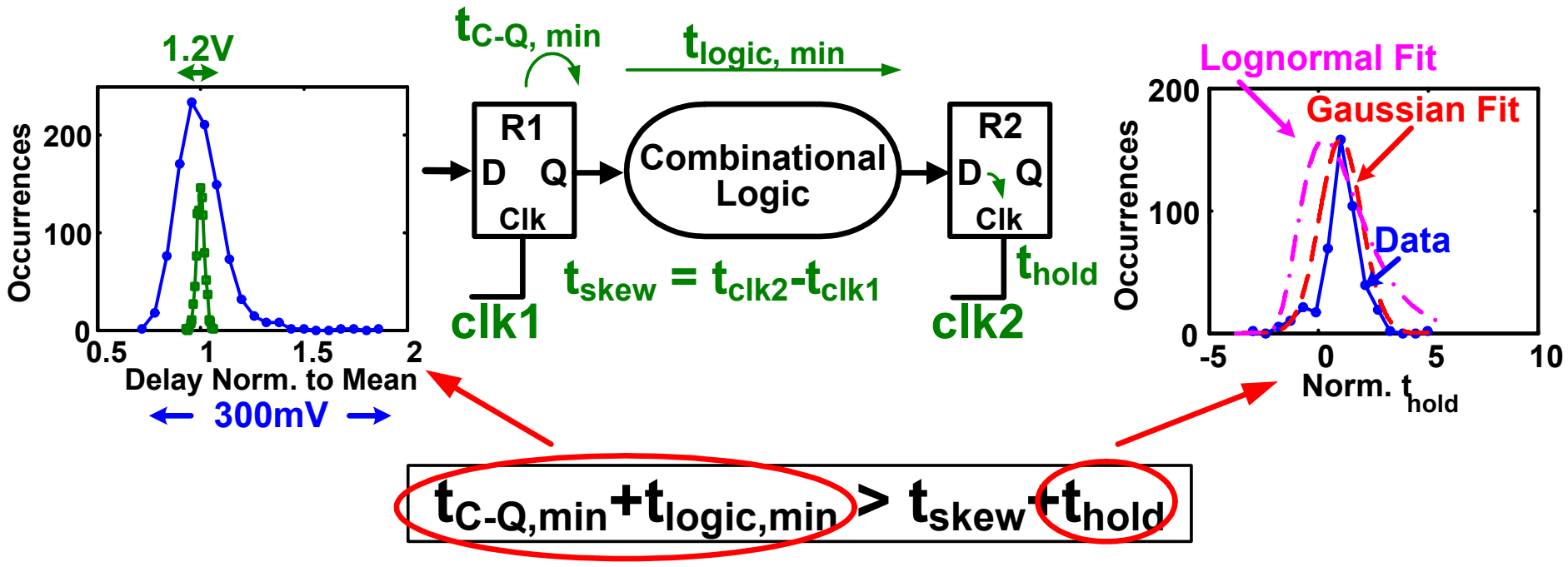
Buffer eliminates read SNM limitation
Peripheral assists allow sub-V_t writing and sensing

Peripheral Assists



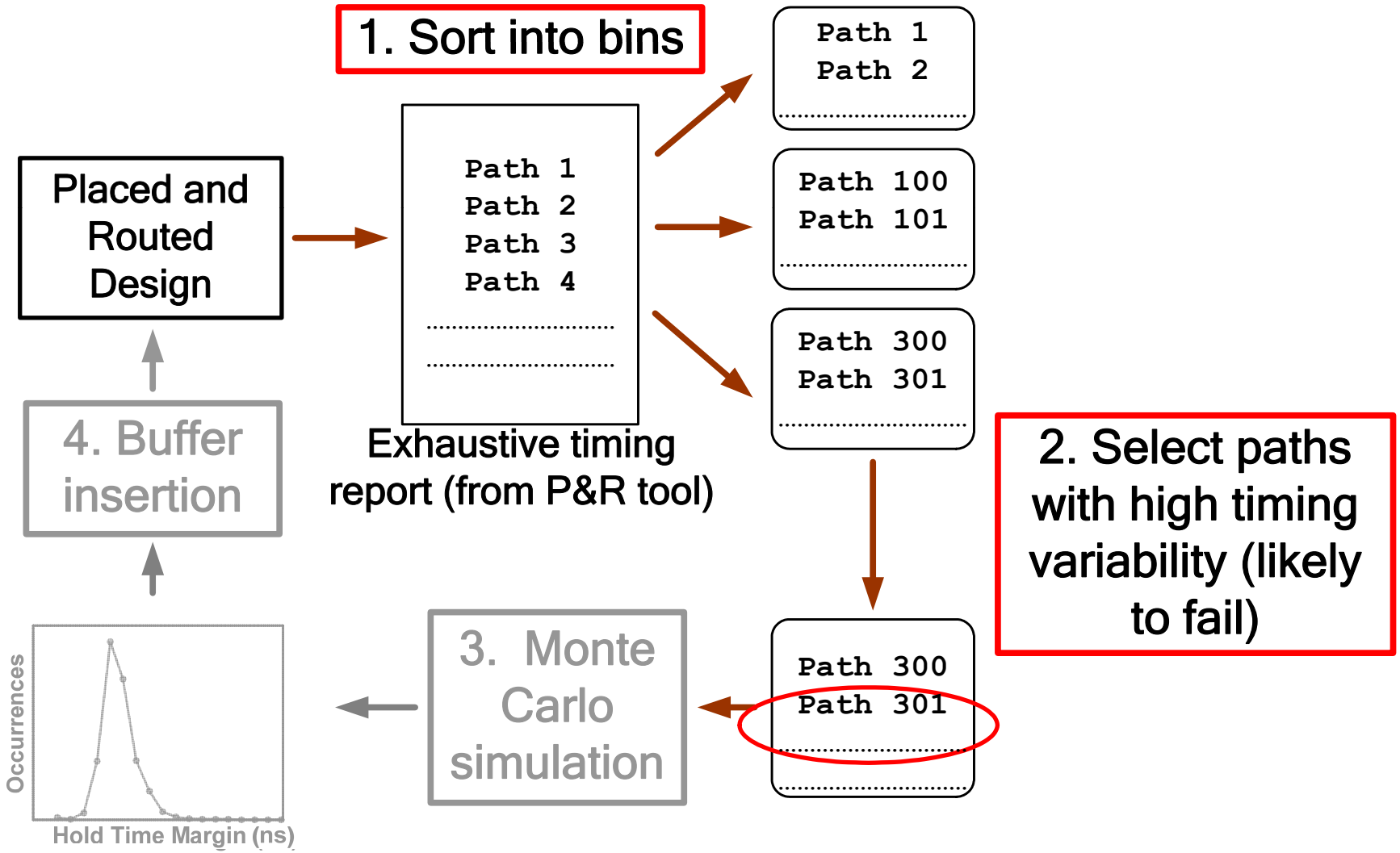
Sub-V_t Timing Analysis Challenges

Order-of-magnitude higher delay variation in sub-V_t



Timing Analysis Methodology

- **Focus on hold time violations**

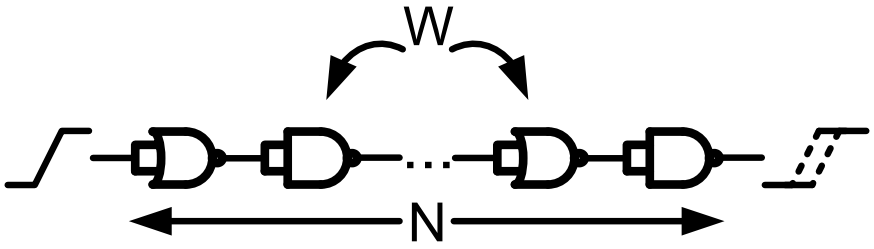


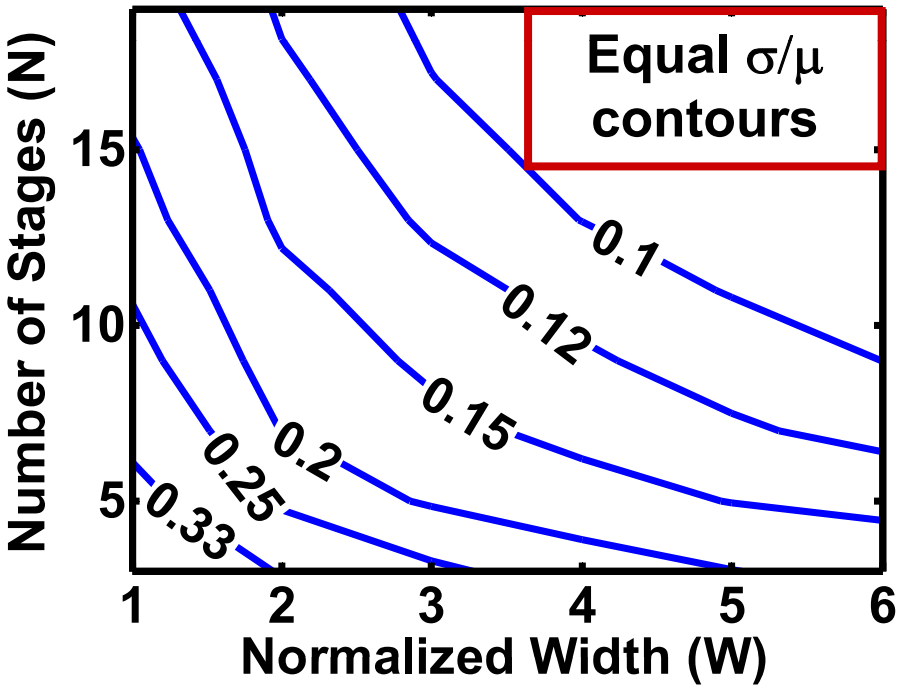
Path Selection

- **Select paths with large σ/μ:**

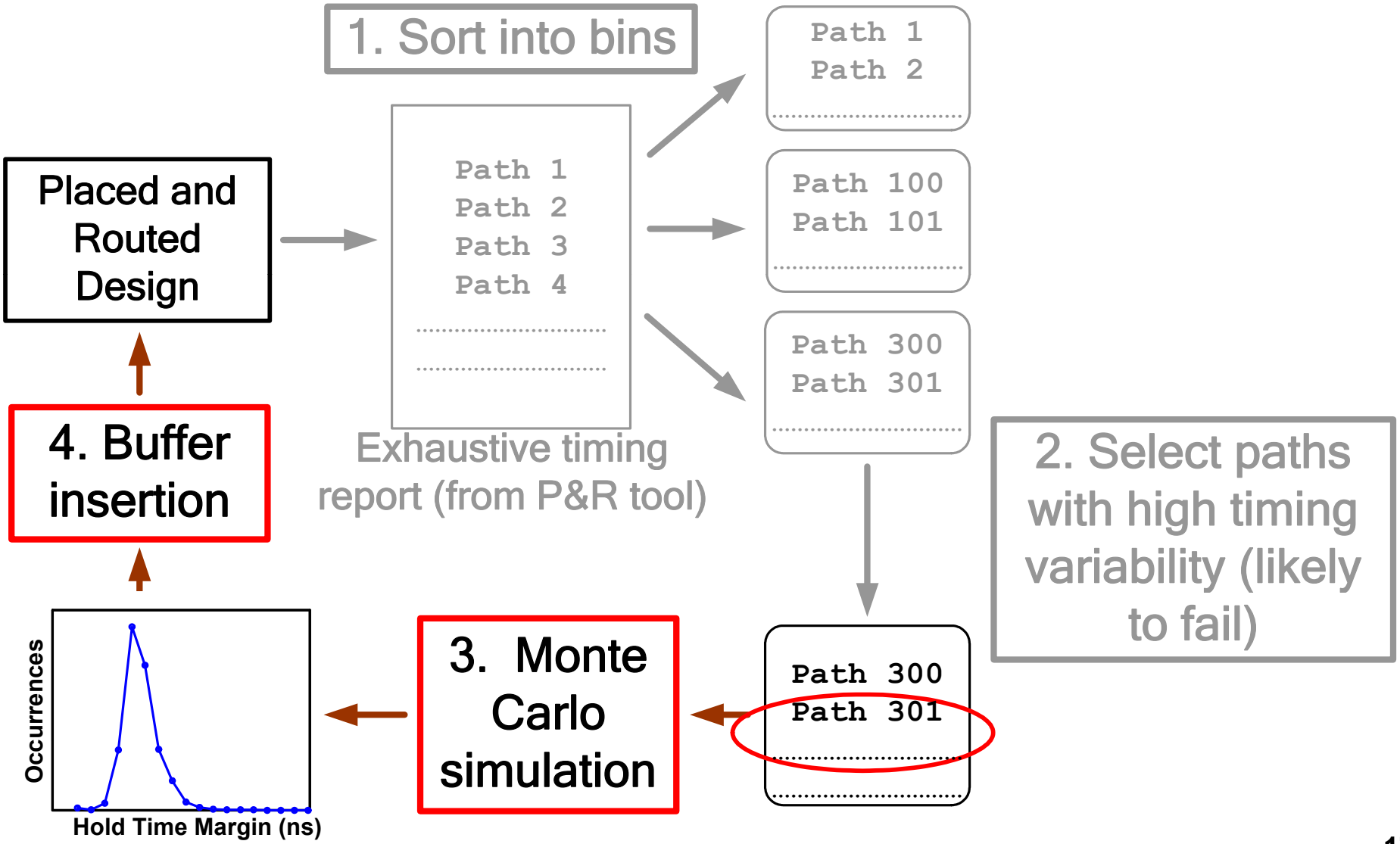
(1) Consider effect of transistor sizes on σ/μ of logic gates in path

(2) Assign weighting to each path according to logic depth



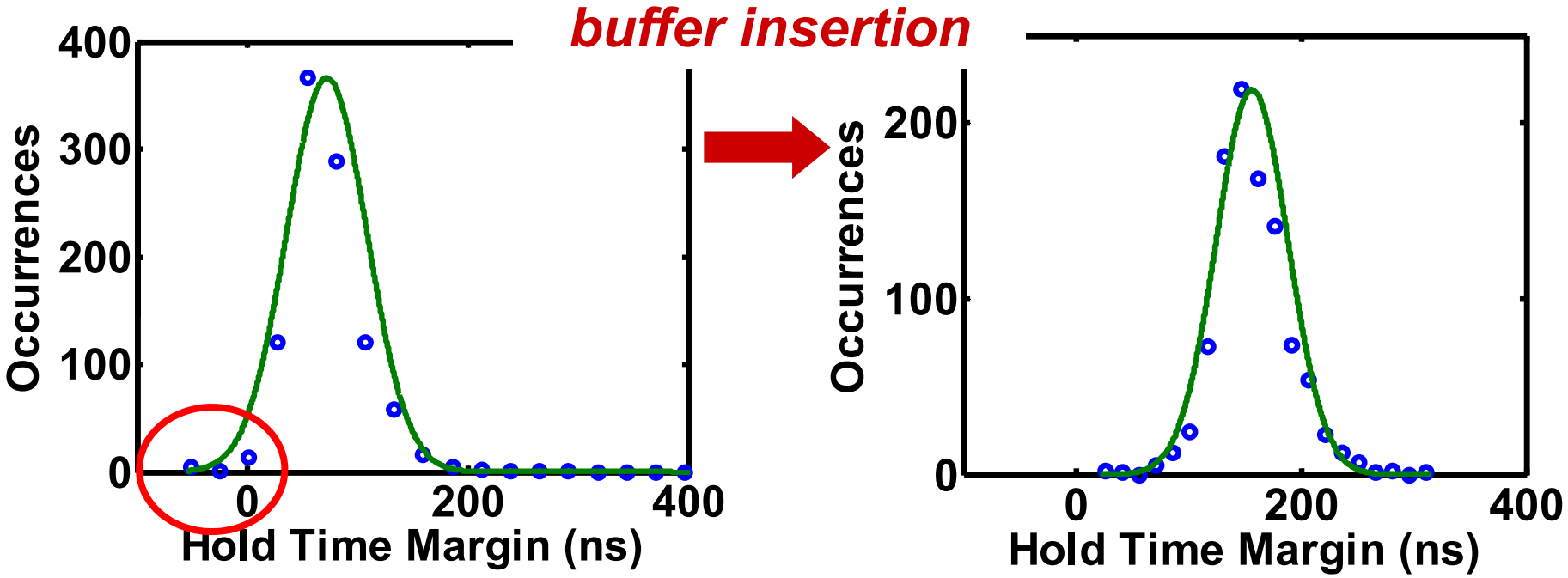


Timing Analysis Methodology



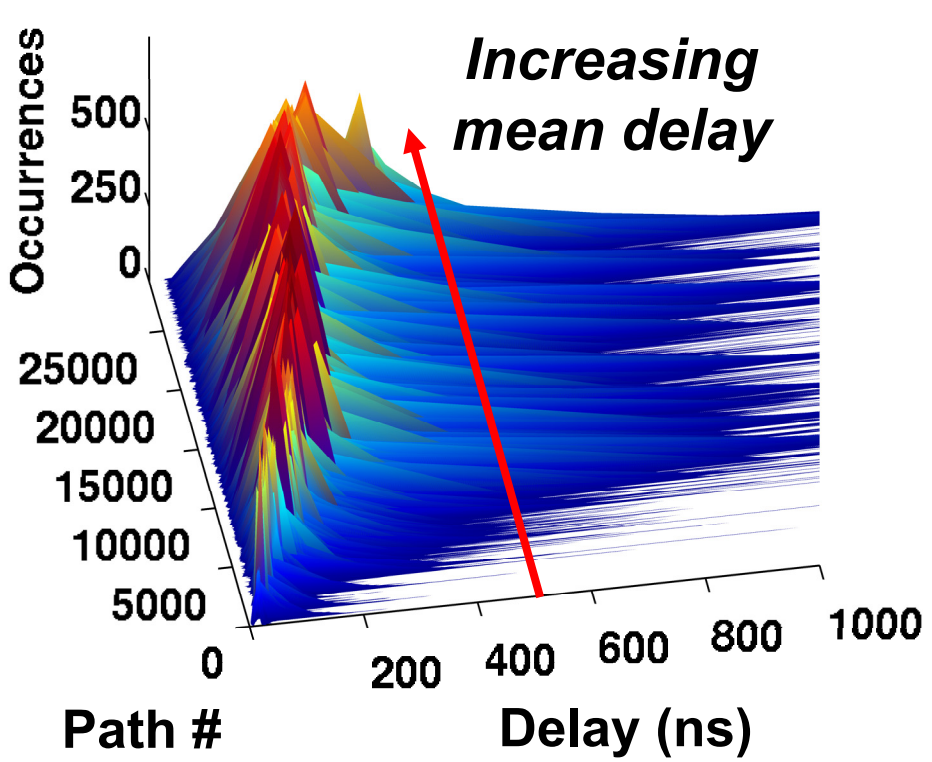
Simulation and Buffer Insertion

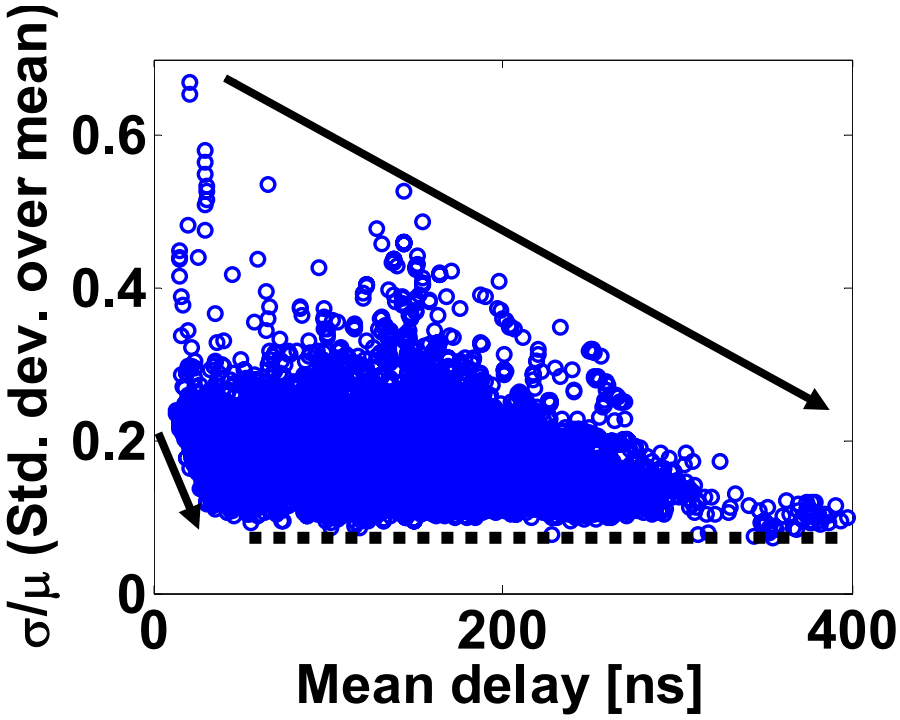
- Monte Carlo simulation of selected paths gives accurate hold time margin distribution
- Delay buffers added as necessary to reduce probability of hold violation



Comprehensive Timing Simulations

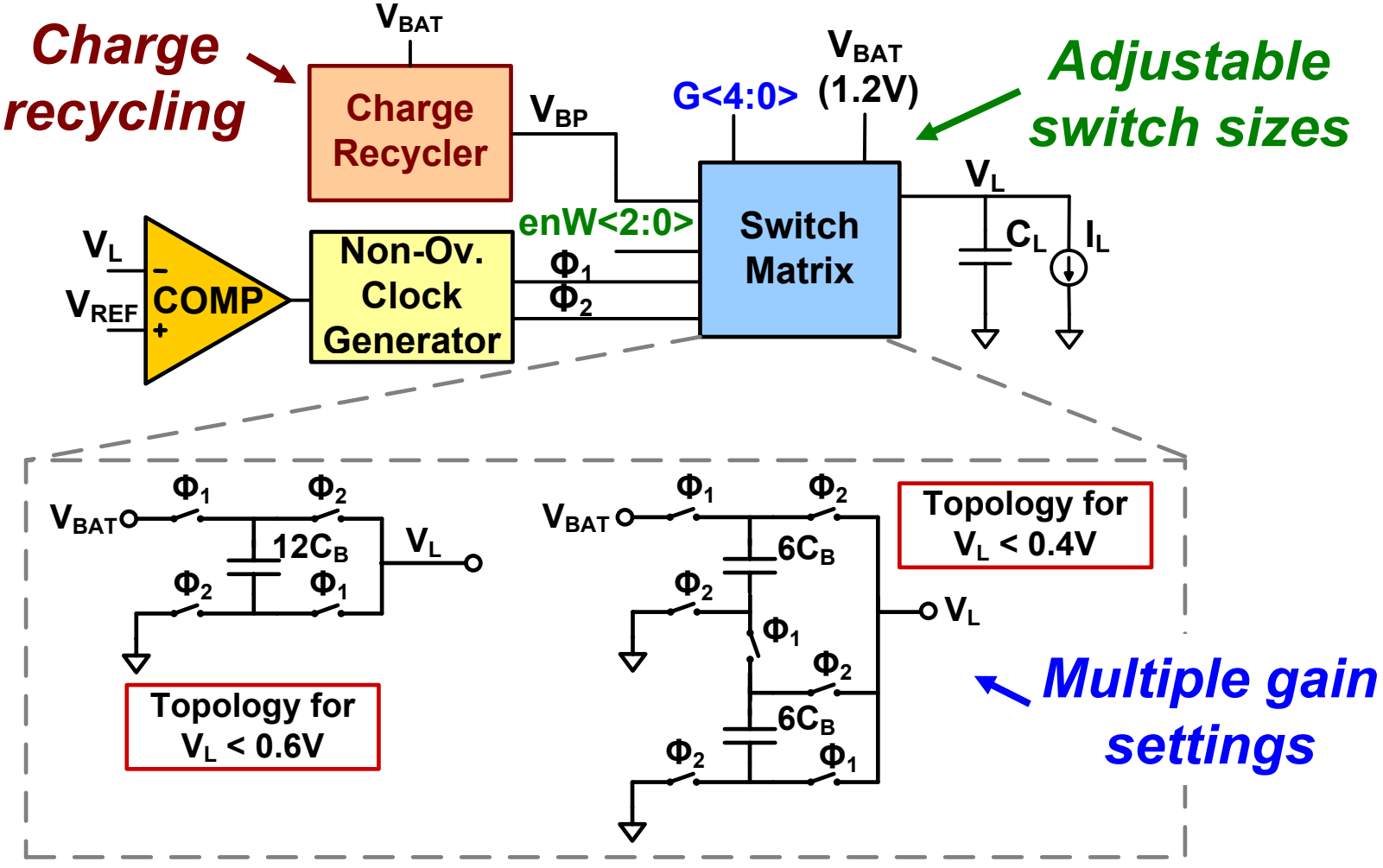
Simulation of 30000 timing paths illustrates trends in sub-V_t delay variability





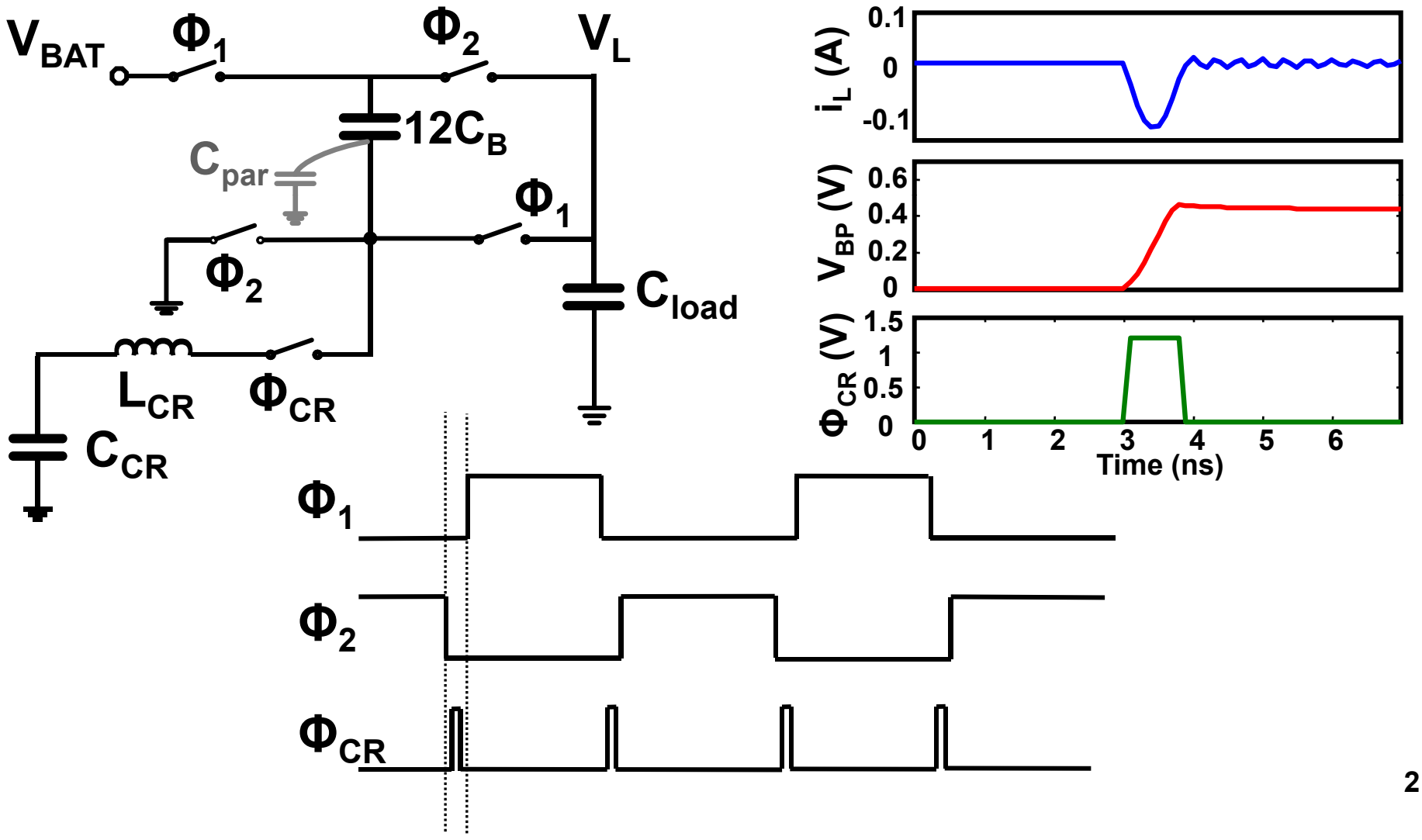
DC-DC Converter Architecture

Programmability helps maintain efficiency over wide range of voltage and power levels



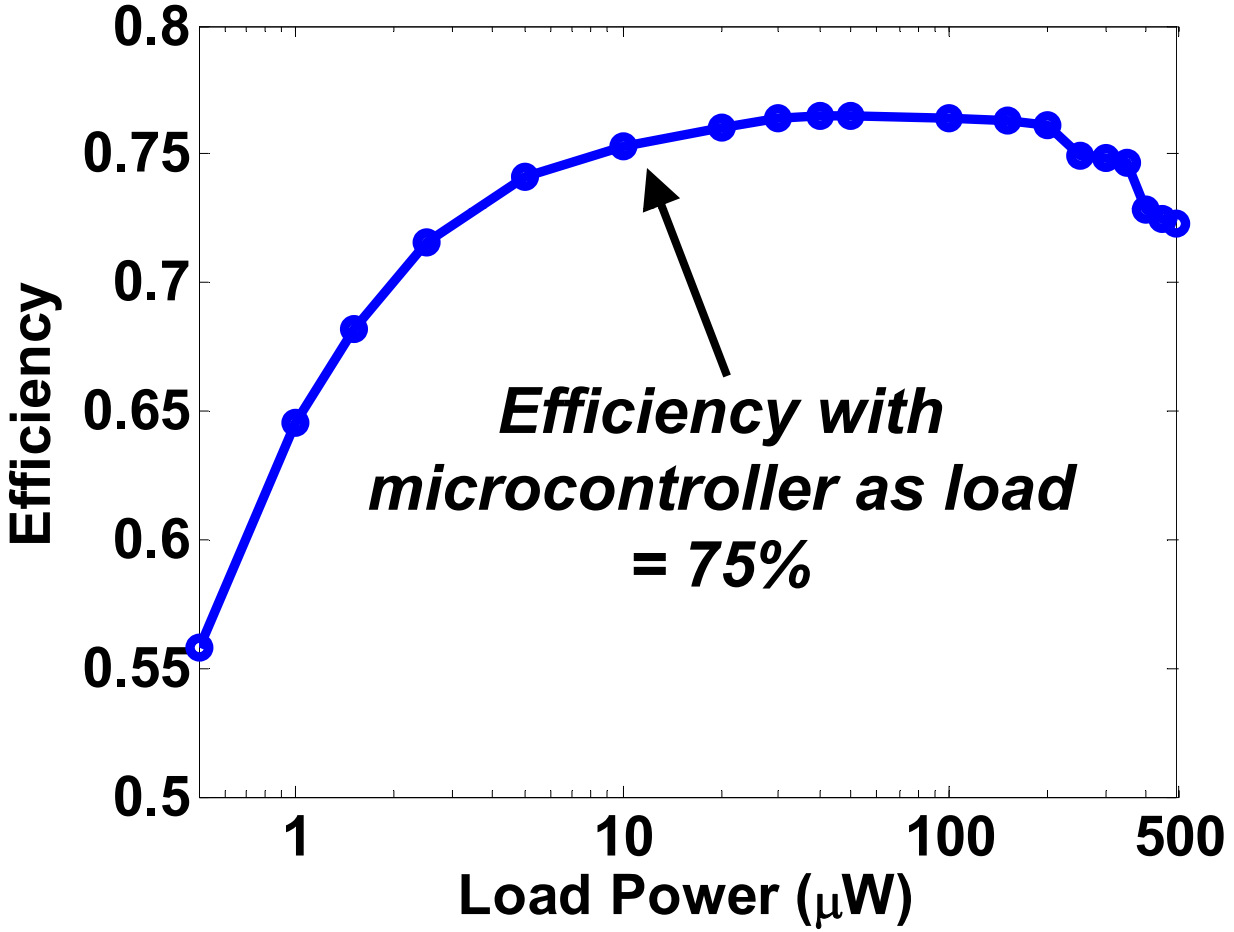
Charge Recycling

Reduce losses due to bottom plate parasitic capacitance



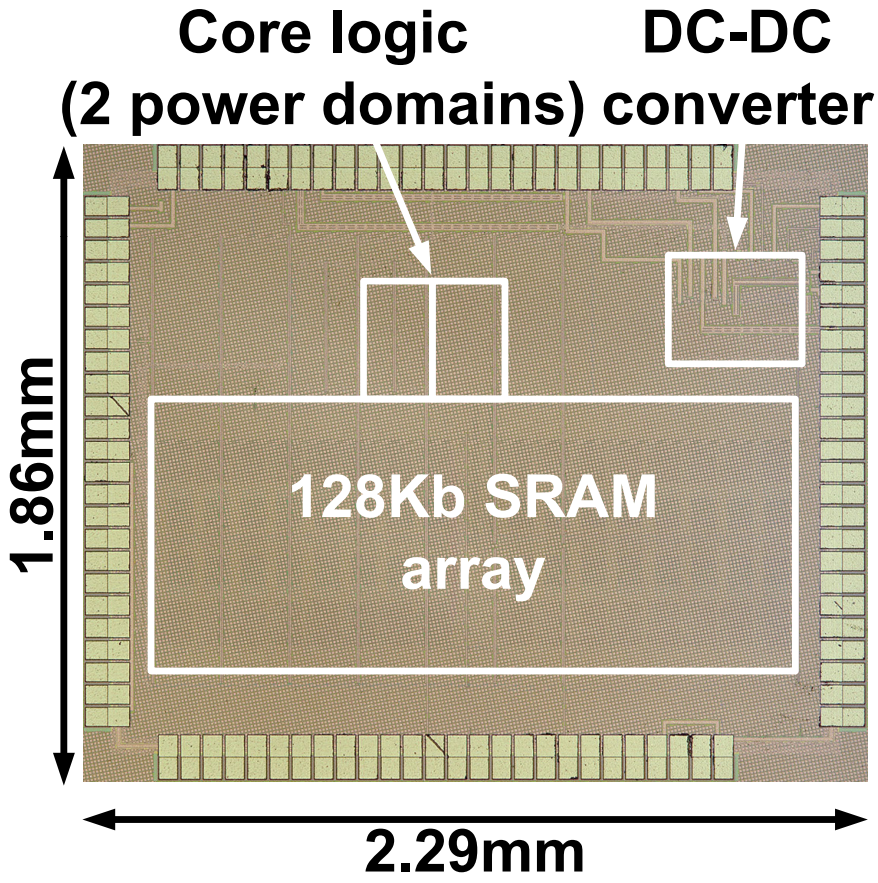
DC-DC Converter Efficiency

Measured efficiency while delivering 500mV

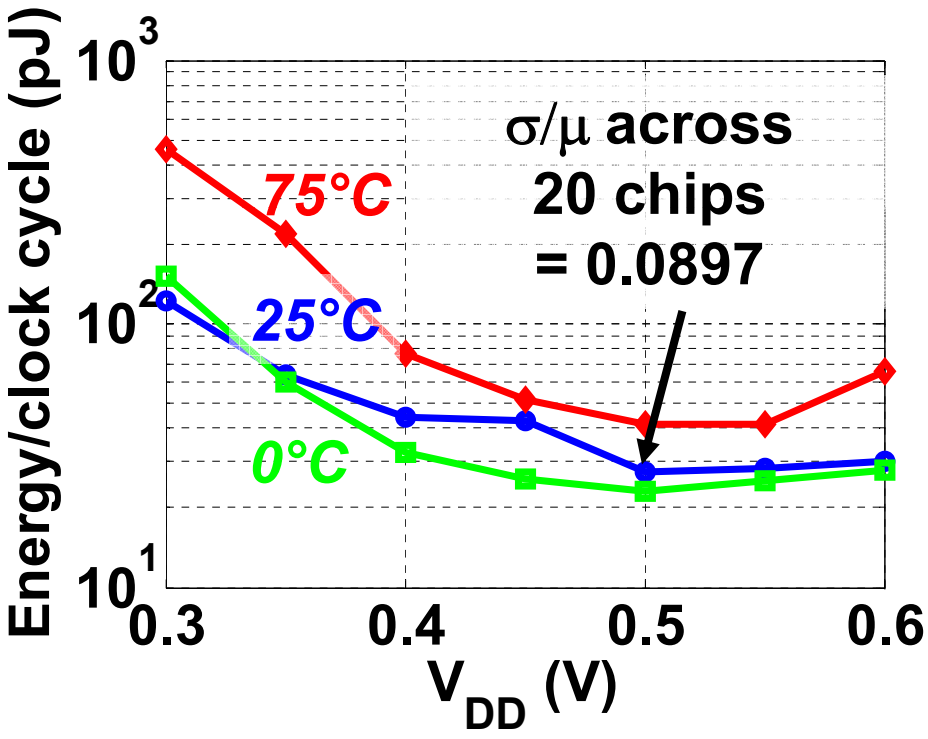


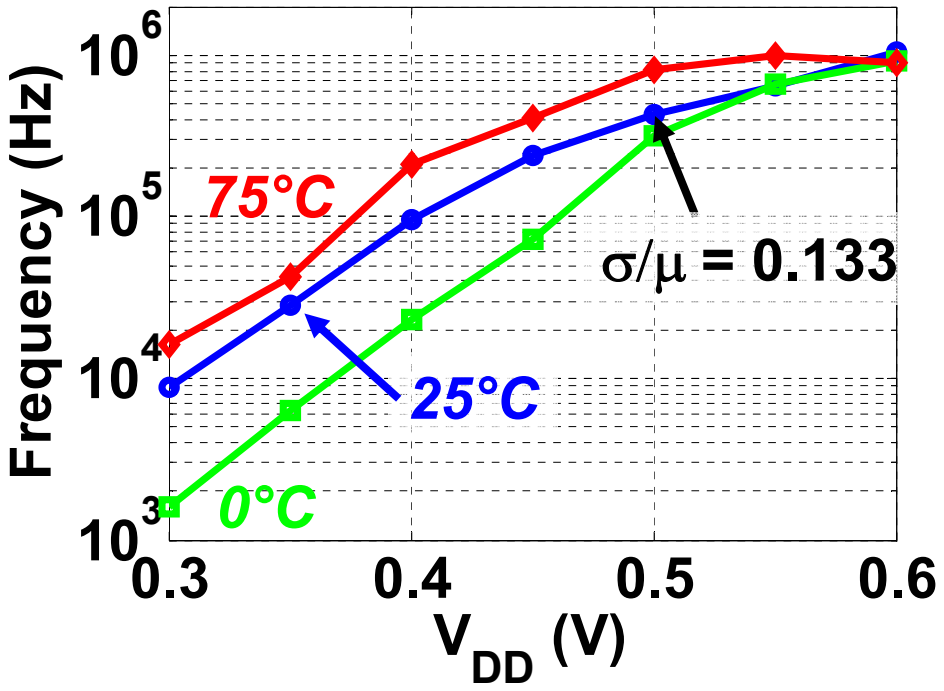
Test-Chip Summary

Process	65nm CMOS
Area	
DC-DC Converter	0.12mm^2
SRAM	1.36mm^2
Logic	0.14mm^2
Performance	
Minimum Energy Point	V_{DD} = 500mV
Minimum Functional V_{DD}	V_{DD} = 300mV



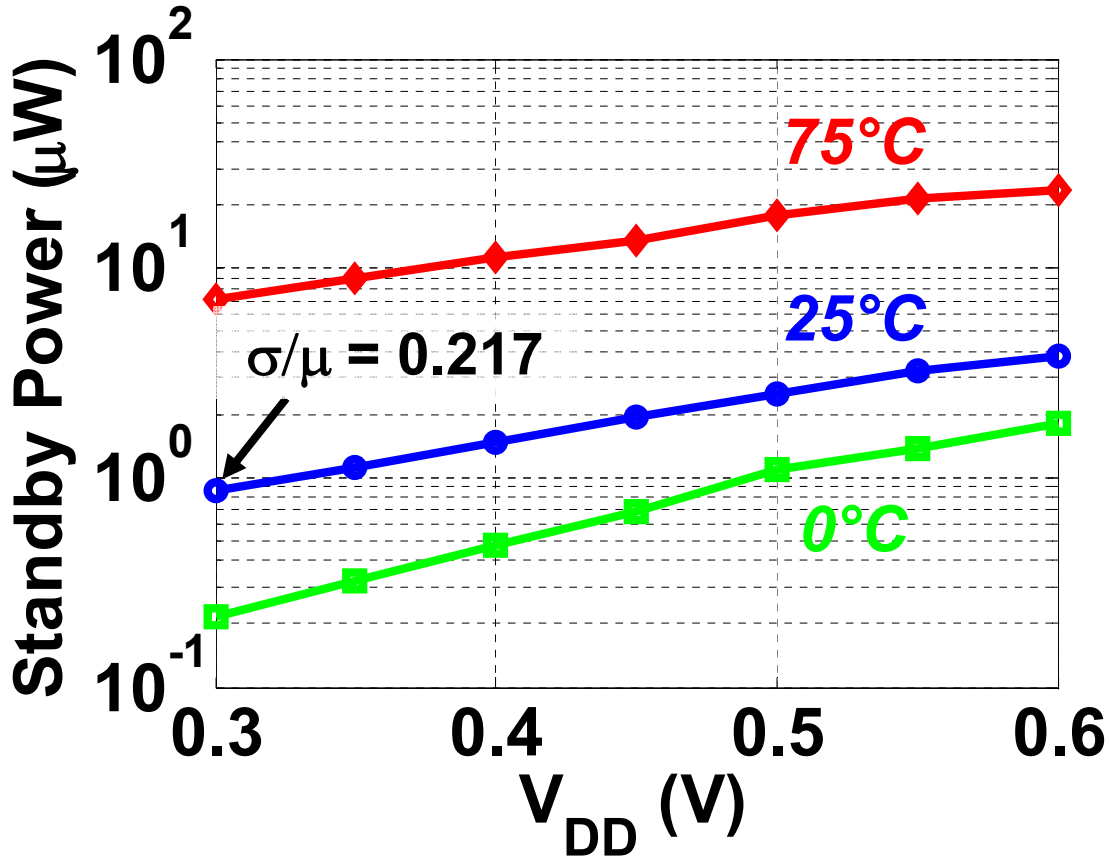
Measured Energy and Frequency





Measured Standby Power

Dynamically scale V_{DD} to 300mV during standby



Conclusions

- Demonstrated 65nm SoC functional down to 300mV
- Sub-V_t design techniques mitigate effects of process variation in logic and memory
- Switched capacitor DC-DC converter provides efficient power delivery with low area overhead

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