An All-Digital, Highly Scalable Architecture for Measurement of Spatial Variation in Digital Circuits

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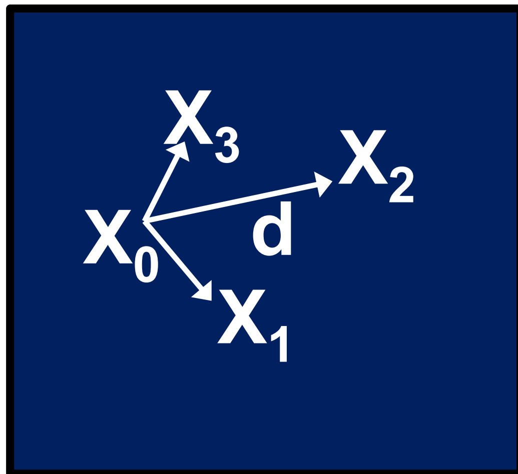
Outline

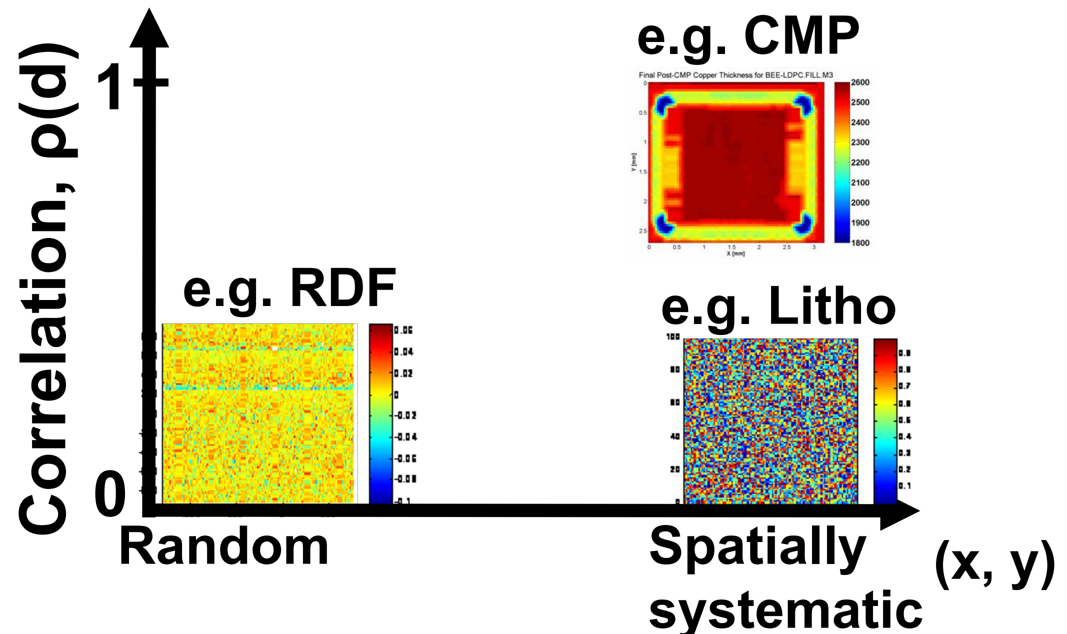
- **Motivation: Variation**
- **Chip Architecture: Characterize *Spatial* Variation**
- **All-Digital, High-Resolution Delay Measurement**
- **Results & Analysis**
- **Conclusion**

Motivation

- Relative variation increasing with scaling
- Mitigation techniques highly dependent on scale/type of variation
- Distinction between separation-distance dependent and position dependent

$$\rho_{x,x\pm d}(d) = \frac{Cov(x,x\pm d)}{\sigma_x^2}$$





Spatial Variation Modeling

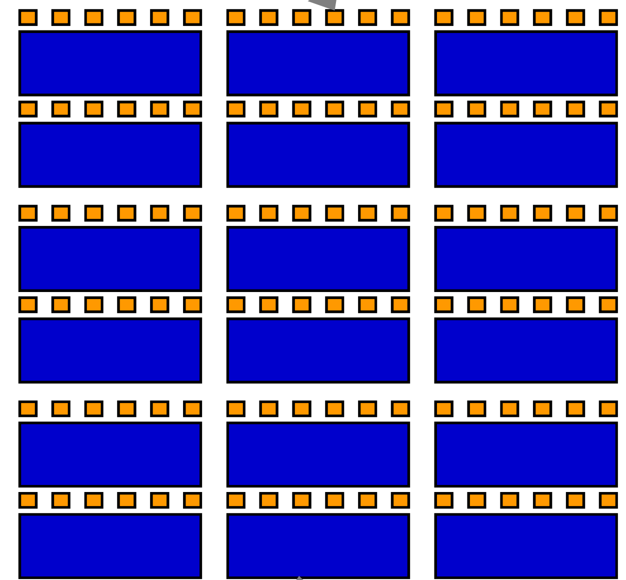
- Characterization and appropriate modeling critical to robust design
- Many statistical static timing approaches seek to include spatial variation
  - Attempt to bridge between completely systematic and completely random
  - Assume spatially correlated variation
  - Typically not validated with manufacturing data

Previous Work

- **Many arrayed *device* structures**
  - **Do not propagate to circuit performance**
- **Recently more interest in arrayed *circuit* structures:**
  - **L.-T. Pang et al., "Impact of Layout on 90nm CMOS Process Parameter Fluctuations," VLSI Symp., 2006.**
  - **M. Kotani, et al., "A 90nm 8x16 LUT-based FPGA Enhancing Speed and Yield Utilizing Within-Die Variations," ESSCIRC, Sept. 2006.**
- **Our features:**
  - **Additional analysis of spatial variation**
  - **Increased spatial/temporal resolution**

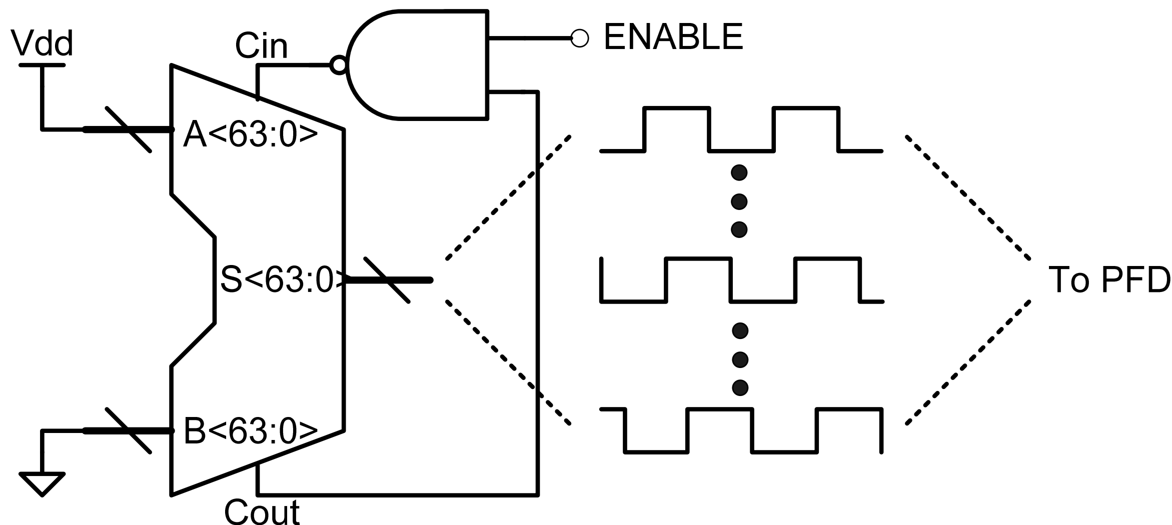
Chip Architecture (High-level)

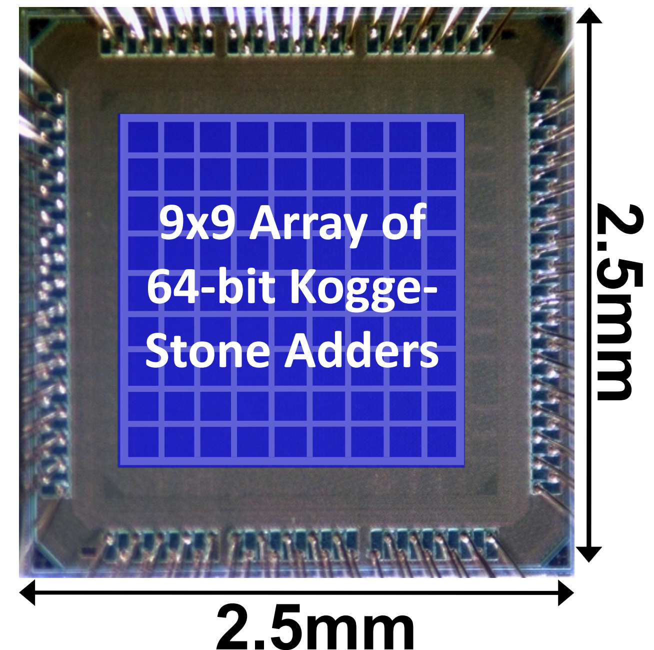
- **Measuring spatial variation requires large numbers of:**
  - Replicated "critical" circuits
  - Interspersed "sensor" circuits
- **In-situ, high-resolution (temporal) delay measurement**
  - Random sampling technique achieves ~200fs delay resolution
  - No lower-bound on minimum measureable delay



Chip Architecture (Details)

- 9x9 array of 64-bit Kogge-Stone adders in oscillating configuration
- 16 interspersed ring-oscillators of varying types with each adder
- Frequency counters

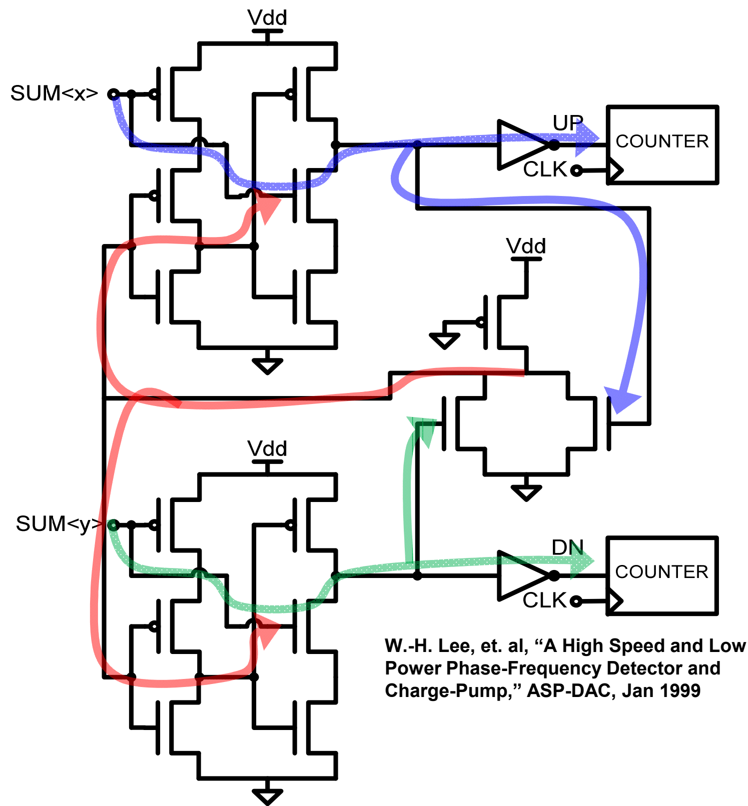


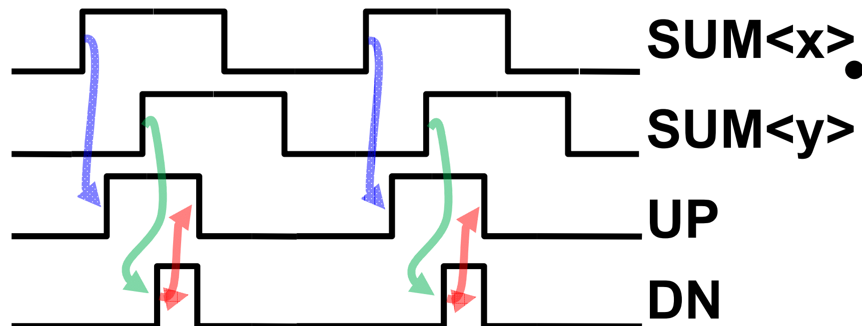


All-Digital Delay Measurement

- Each bit of 64-bit adder oscillates at same frequency, but slightly out of phase
  - Phase difference equivalent to delay difference between bits
- XOR gates typically used to measure phase difference, but limited by gate delay
- Can avoid this by transforming to measure difference in two pulse widths
- Random sampling technique used to sample pulses over large number of cycles

Pulse-Width Measurement (PWM)





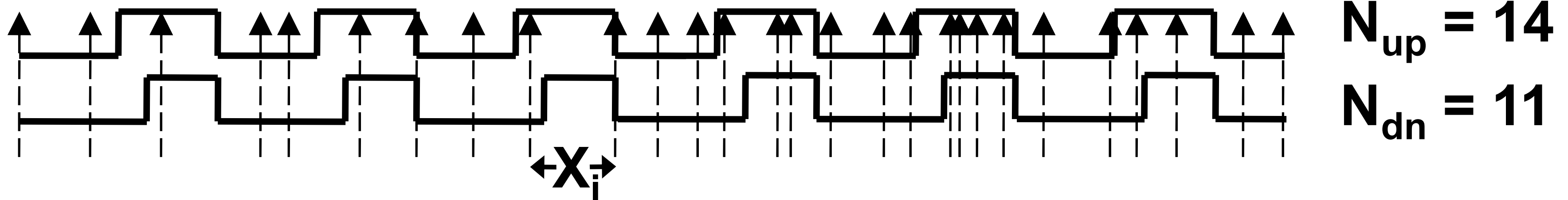
- Phase Frequency Detector (PFD): Modified TSPC DFF with self-reset
- Early signal’s edge passes through
- Late signal’s edge passes through but also triggers reset
- Reset *simultaneously* causes falling edge on both UP and DN

PWM: Random Sampling

- **Goal: randomly sample UP/DN pulses with *uniform probability* across cycle**
- **Count number of "1" samples**
- **Delay difference (ΔD) resolution gets better with number of samples**

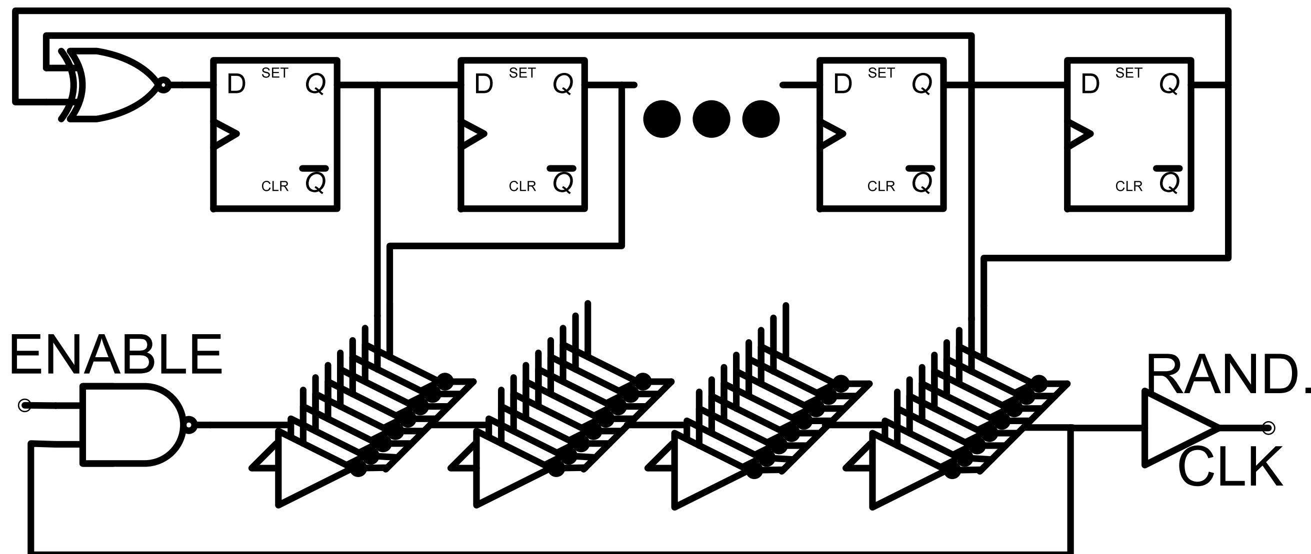
$$\lim_{N\to\infty} \frac{N_{up}}{N} = P_{up} \qquad \triangle D = \tau_{CYCLE}\frac{N_{up}-N_{dn}}{N}$$

P_{up} = Pulse Width as percentage of cycle



PWM: Random Sampling (cont.)

- **Generating random sampling clock:**
  - **5-stage RO with 32 tri-state drivers**
  - **Linear Feedback Shift Register (LFSR)**
    - **Generates pseudo-random bit sequences**
    - **Controls tri-state drivers**

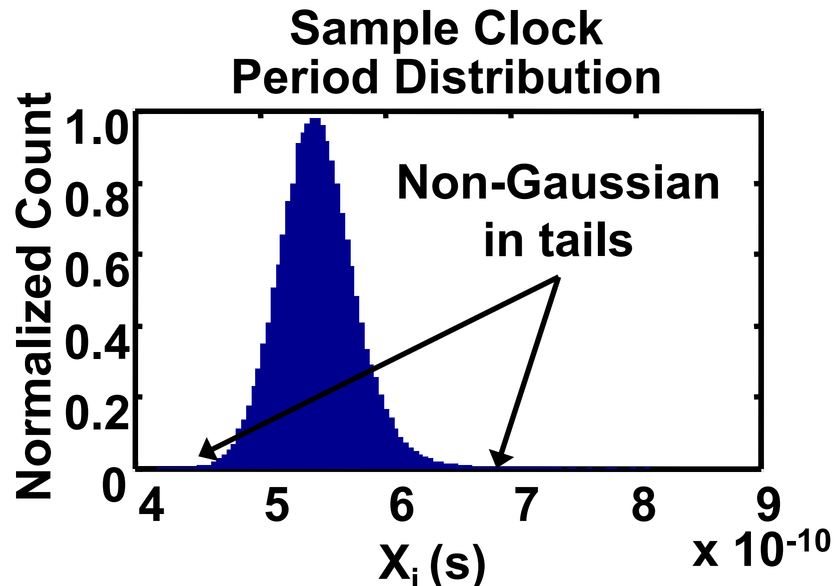


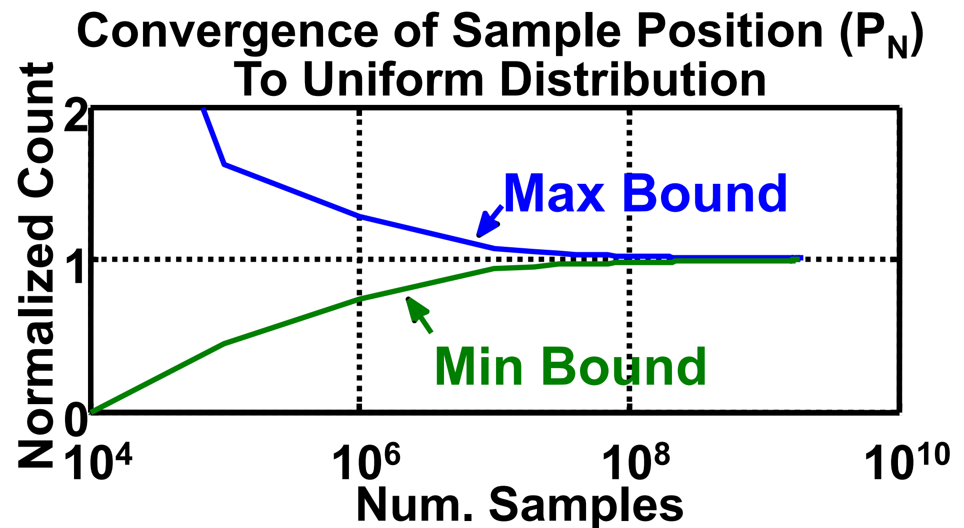
PWM: Clock Period Distribution

- Clock periods close to normally distributed
- Distribution of sample position in cycle *converges to uniform* → higher linearity

$$P_N = mod\left(\sum_{i=1}^{N} X_i, t_{cycle}\right)$$ where t_{cycle} is period of sampled signal

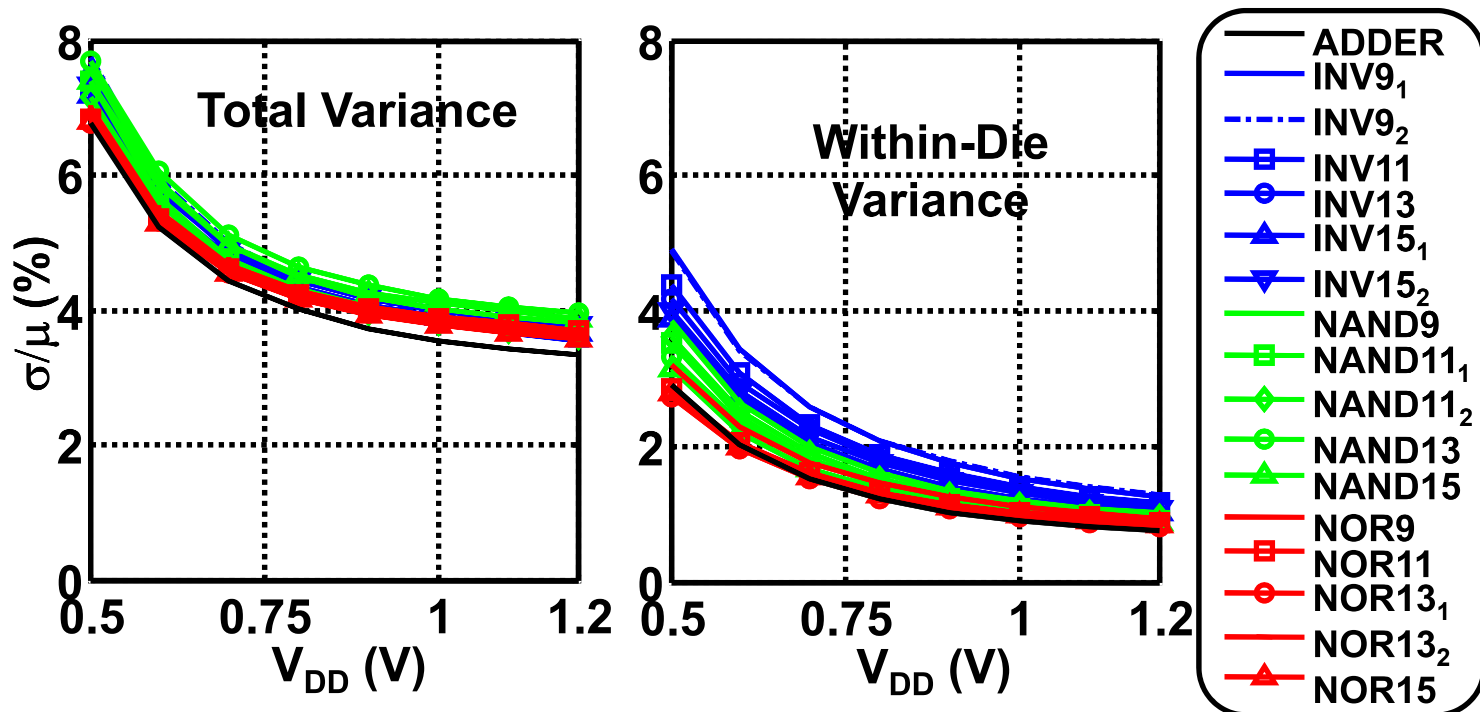
- ~200fs resolution with 99.9999% confidence using analysis in R. Bhatti, et al., ISCAS, May 2006.





Results: Variation Measurements

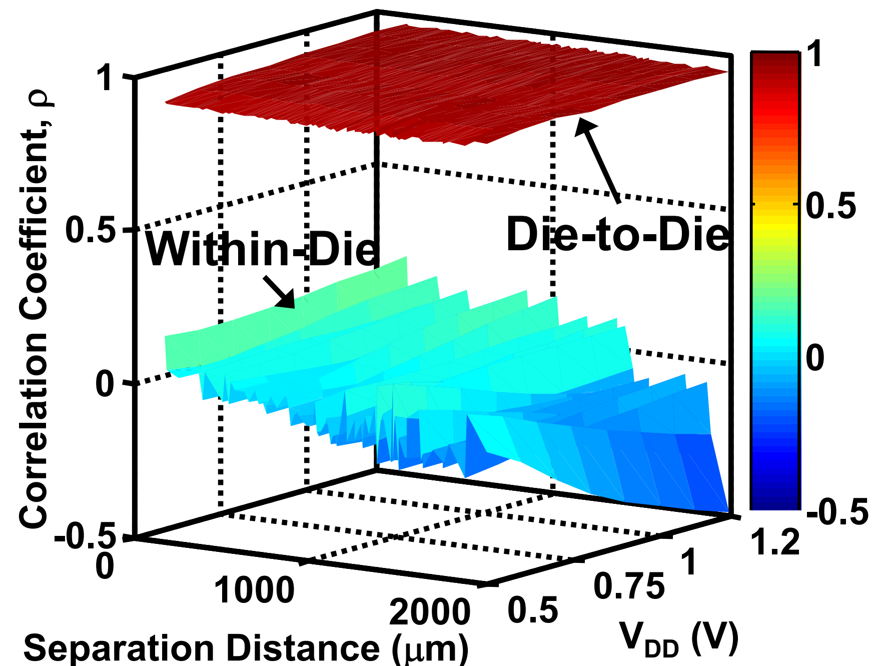
- Measured 41 chips over 2 wafers
- Variation measurements show expected trends
  - Decreases with larger gate size and longer path length
  - Increases at low voltages (lower gate-overdrive)
  - Within-die is increasing fraction of total as voltage decreases



Results: Spatial Correlation

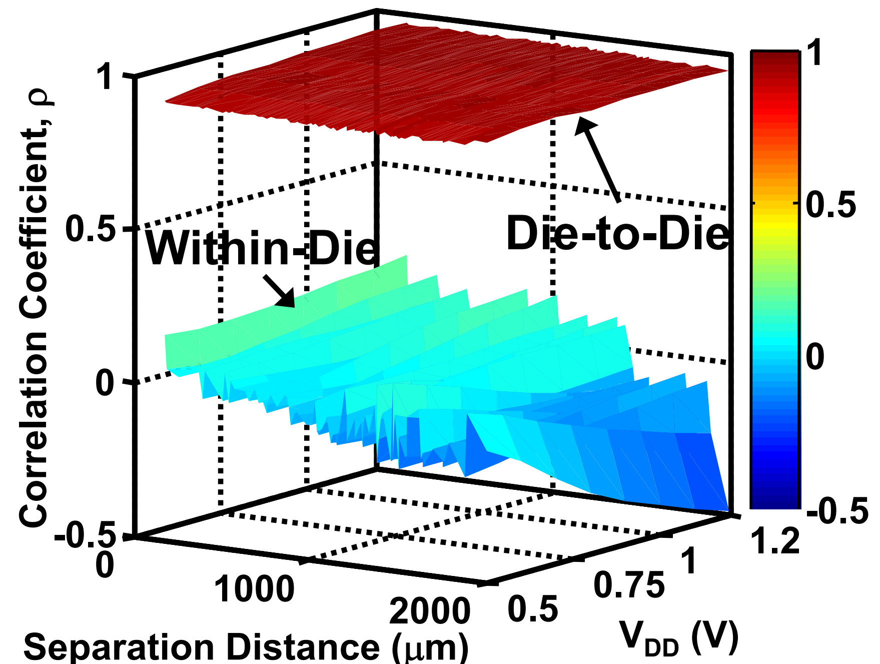
- Large number of circuits enables extraction of spatial correlation
  - Over 1000 pairs of adders at closest separation distance, 82 pairs at largest separation distance

- No statistically significant within-die spatial correlation
  - Correlation shown with adder mean for each chip subtracted

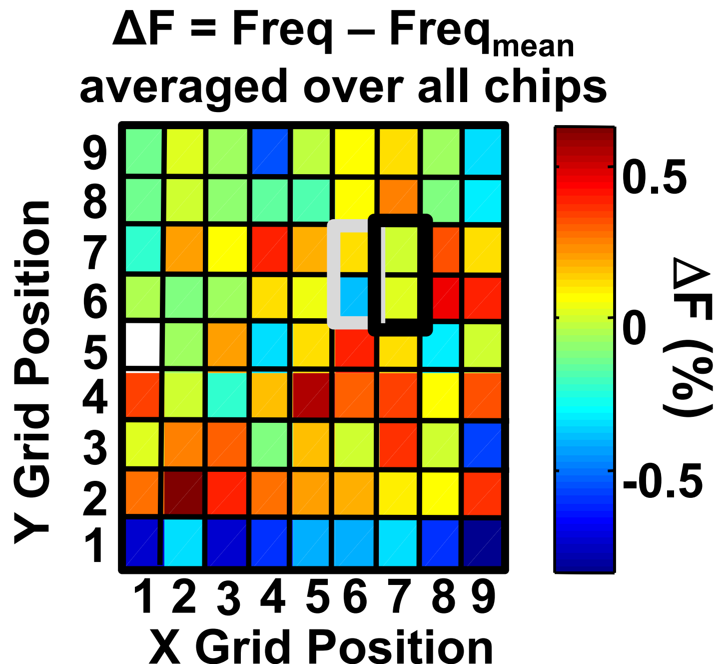


Results: Spatial Correlation

- **Strong die-to-die correlation**
  - Correlation shown retaining adder chip means
- **Weak spatial dependence**
- **Correlation decreases with power-supply voltage**
  - Effect of random V_T variation increases due to lower gate-overdrive
- **Adder shown here but same trends for all RO circuits**



Results: Spatial Variation



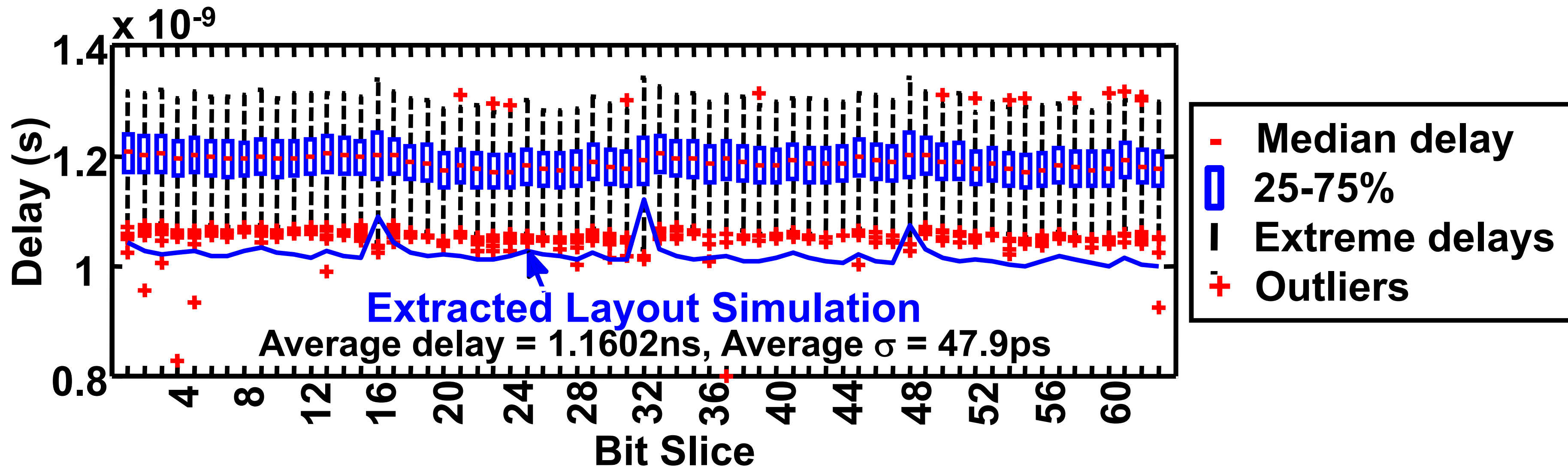
- Lack of correlation ≠ lack of within-die systematic variation
- Weak repeatable systematic variation pattern is seen
  - Small fraction of total variation

- Equidistant pairs of adders can have:
  - Different magnitudes of ΔF (deviation from mean)
  - Directionally opposite ΔF
- Systematic effect: Position-dependent *(x, y)*, *not* distance-dependent *ρ(d)*

Results: Delay Measurement

- Random sampling circuits used to measure adder bit delays
  - All bits measured relative to Sum<0>
  - Single PFD per adder
    - Sum<0> into one PFD input
    - All bits mux-able into other PFD input
    - Offsets subtracted by measuring Sum<0> versus itself
- $1.7x10^8$ samples per measurement
  - Uniform distribution of samples within cycle
  - Noise reduced due to large number of samples

Results: Delay Measurement



- Good agreement with post-layout simulation
  - 20% slower than simulation → slow process
  - Consistent with slower adder/RO frequencies
- Able to track peaks due to high resolution
  - Peaks at bits 16, 32 and 48 not as pronounced
    - Due to specific layout – longer wires

Implications for Variation Mitigation

- **High-performance (gate overdrive >2V_T)**
  - Die-to-die variation dominant
  - Replica/monitor circuits sufficient
  - σ/μ small (~1%) → Small margins required (~2-3%)
  - Distance from actual critical path not significant
- **Low-power (V_{DD} <2V_T)**
  - Within-die variation becomes more substantial
  - σ/μ larger (3-5%) → Required margins >10%
  - Cannot rely upon closely spaced replicas
  - Larger devices/gates, longer paths or in-situ monitoring likely required
- **Dynamic Voltage Scaling applications**
  - Need careful analysis of trade-offs between strategies

Conclusion

- **Developed highly scalable architecture for characterization of spatial variation**
- **All-digital, random sampling technique with ~200fs temporal resolution and no minimum bound on measureable delay**
- **Within-die variation larger fraction of total variation as V_{DD} decreases**
- **No discernible within-die spatial (separation distance dependent) correlation, but weak systematic variation**
- **Mitigation techniques must account for operating conditions**

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