A 25µW 100kS/s 12b ADC for Wireless Micro-Sensor Applications

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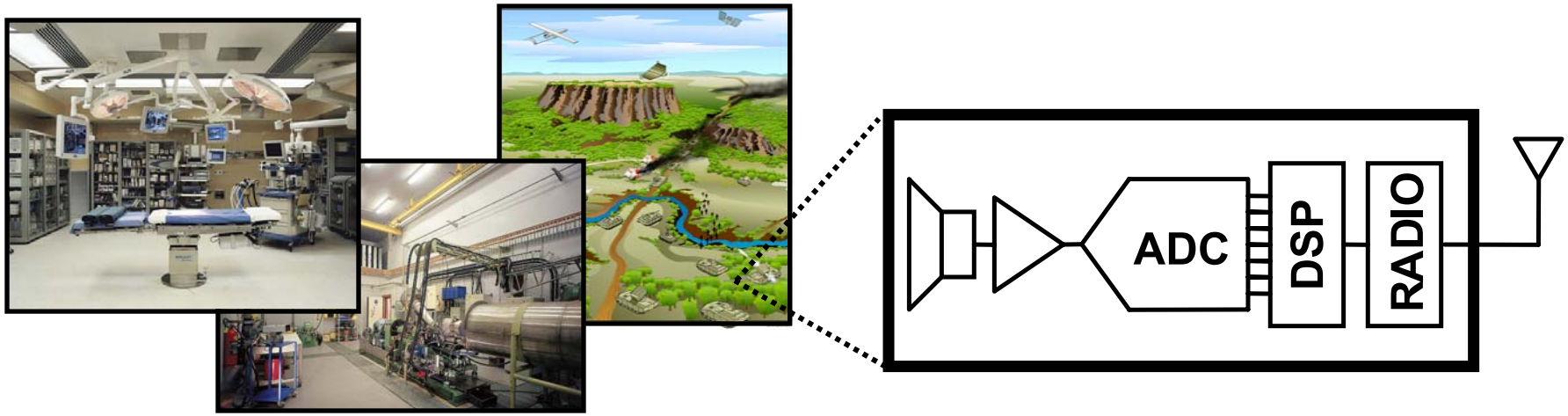
Ultra Low Power Sensor Networks

- **Nodes are intelligent, autonomous, and ubiquitous**



Short bursts of activity between long idle periods

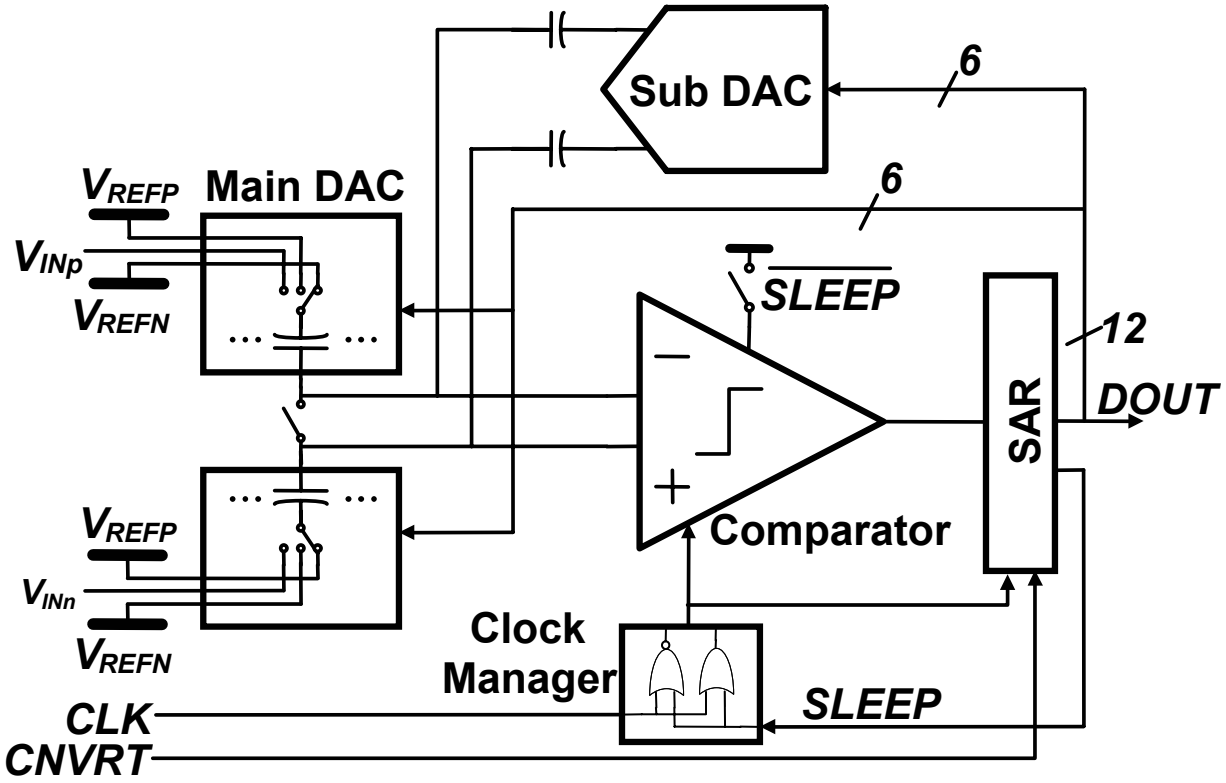
- **ADC specifications**

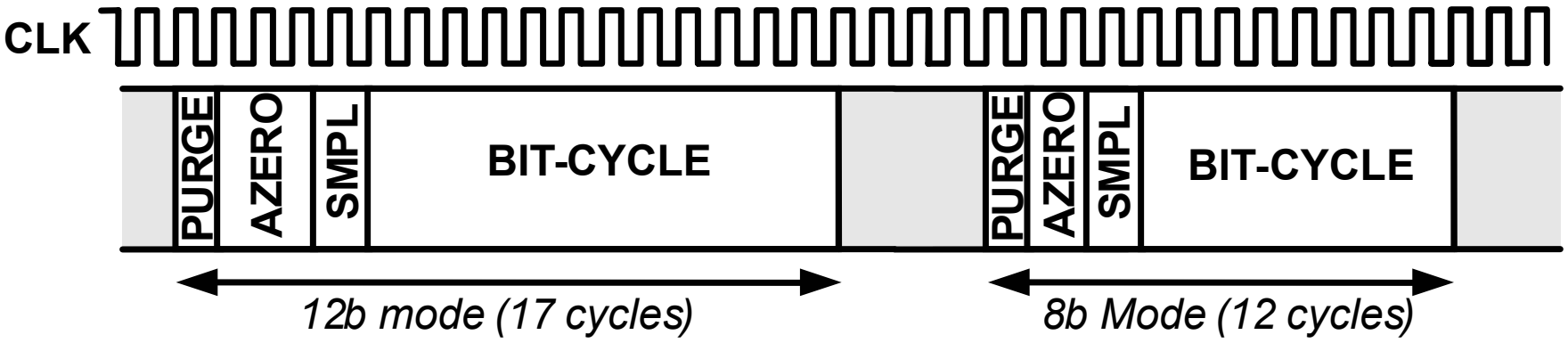
Resolution	12 bits	8 bits
Sampling rate	0-100kS/s	0-200kS/s

Outline

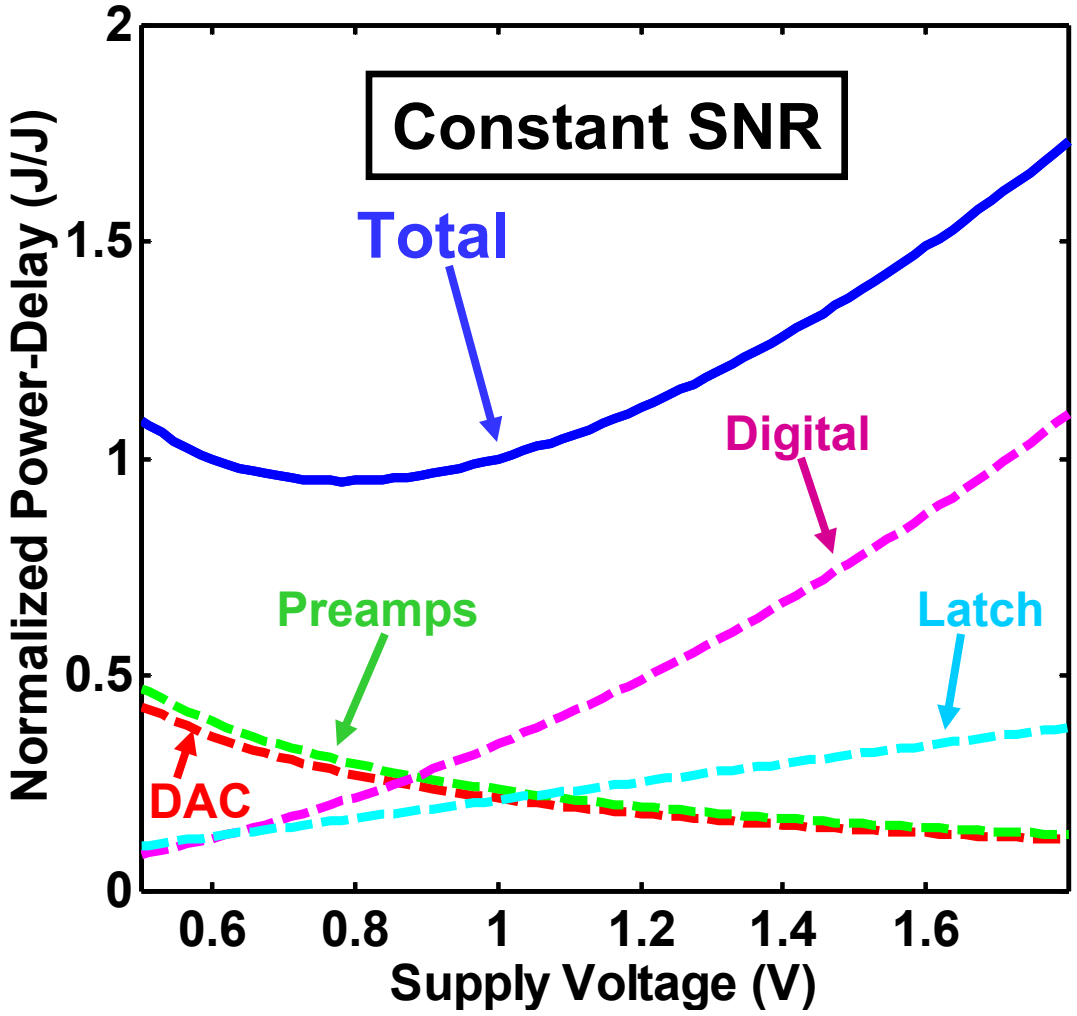
- Architecture
- Global operation and optimization
- Circuit and block level optimizations
- Prototype
- Measurements
- Conclusions

Scalable, Low-Power SAR ADC





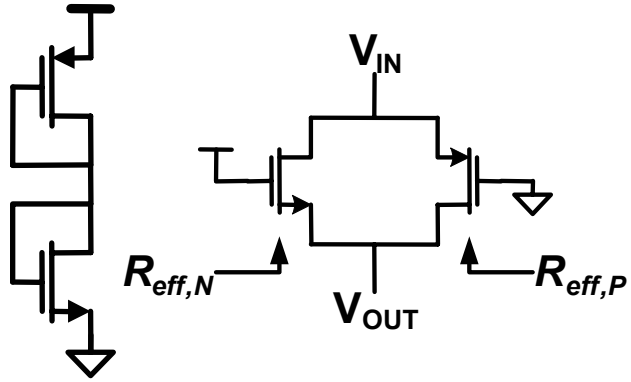
Optimal V_{DD} (1V)



Low Voltage Challenges

1) Noise limitations

2) Biasing, settling time:

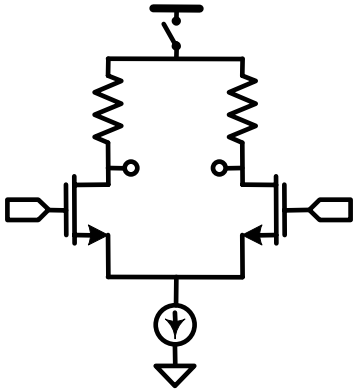


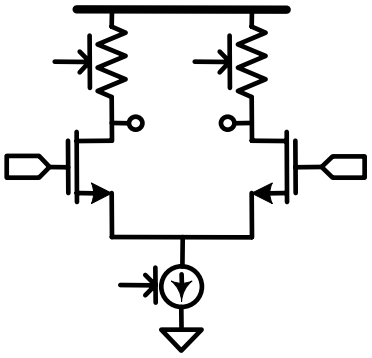
3) Distortion (in SAR):

Active circuits don't require large linear range

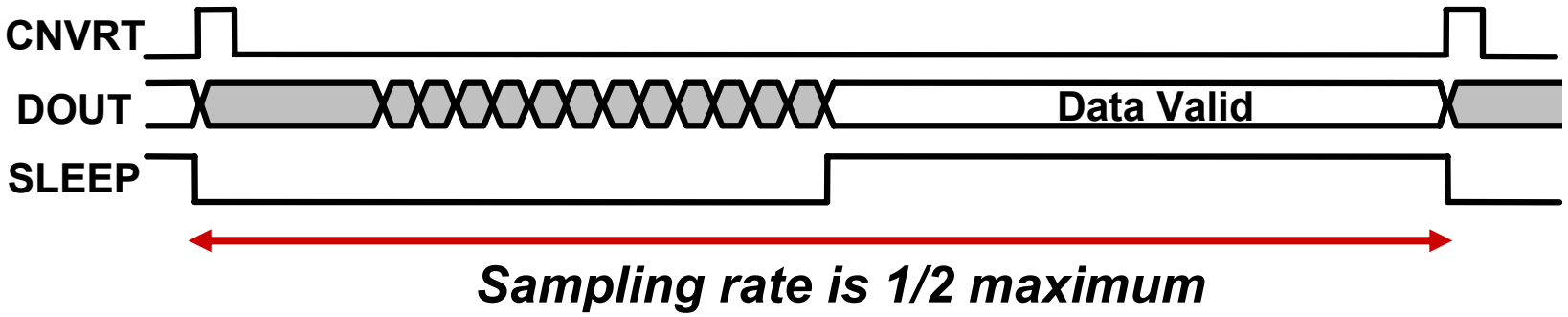
Sample Rate Scaling

Clock-gate to scale digital power. Power-gate to scale analog power

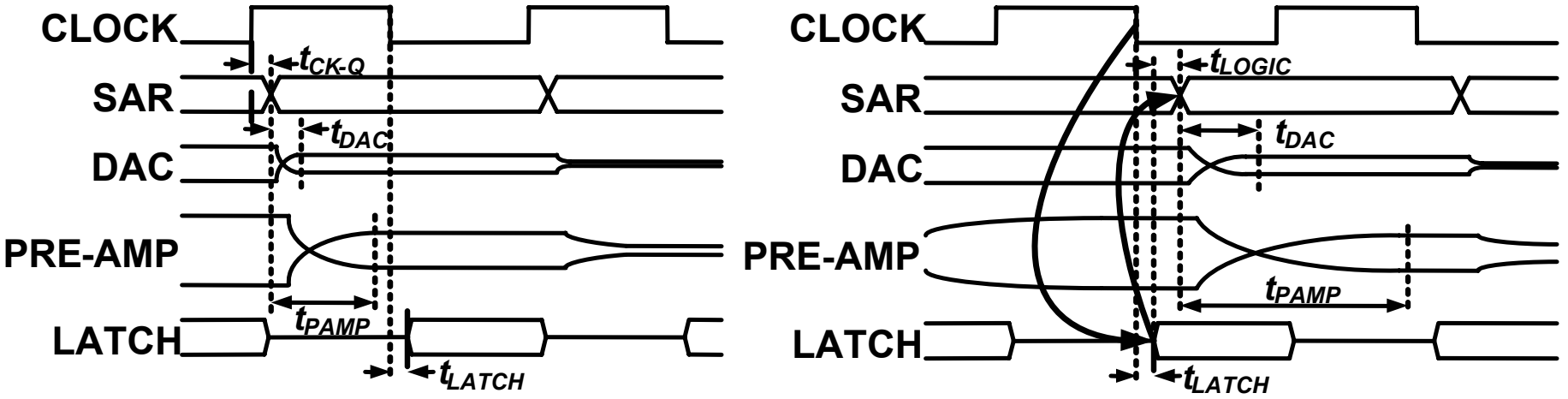




	Power-Gate	Bias Trimming
Power-Delay ($g_m\tau$)	$(\alpha I_B)(R_{OUT}C_{OUT})$	$(\alpha I_B/2)(2R_{OUT}C_{OUT}) = (\alpha I_B)(R_{OUT}C_{OUT})$
Noise $\left(\frac{NqI_B}{4g_m^2R_{OUT}C_{OUT}}\right)$	$\frac{\beta}{I_BR_{OUT}C_{OUT}}$	$\frac{\beta}{(I_B/2)2R_{OUT}C_{OUT}} = \frac{\beta}{I_BR_{OUT}C_{OUT}}$



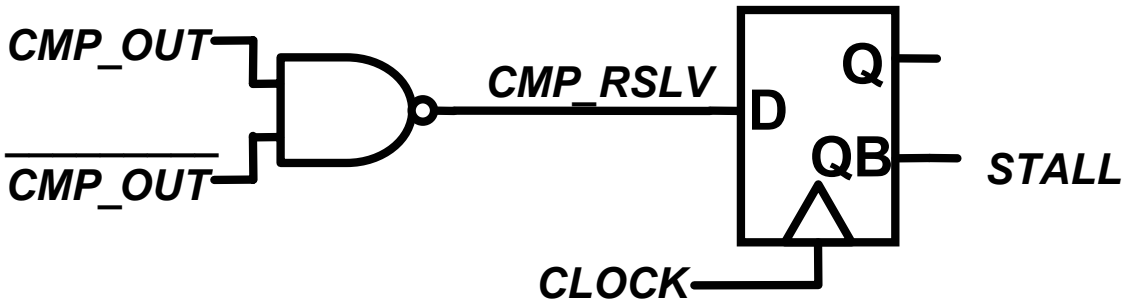
Self-Timed Bit-Cycling



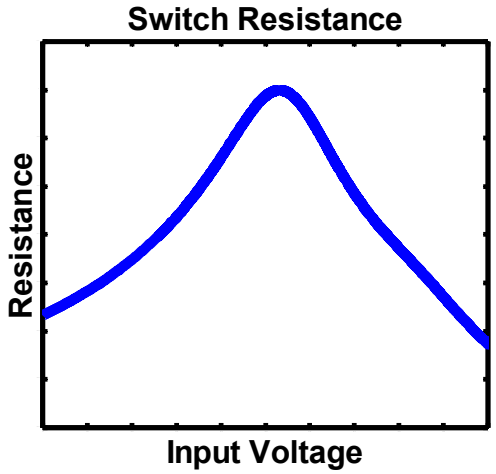
Adopted from [G. Promitzer, ESSCIRC, 2000]

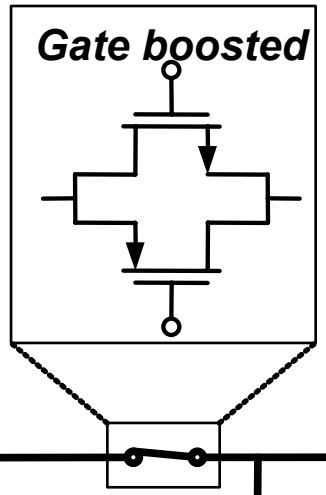
t_{PAMP} is longer by $t_{CK}/2 + t_{CK-Q} - t_{LOGIC} - t_{LATCH}$

If latch doesn't resolve in time, bit decision is forced

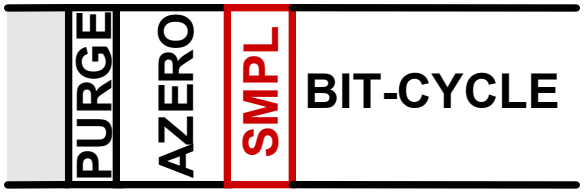


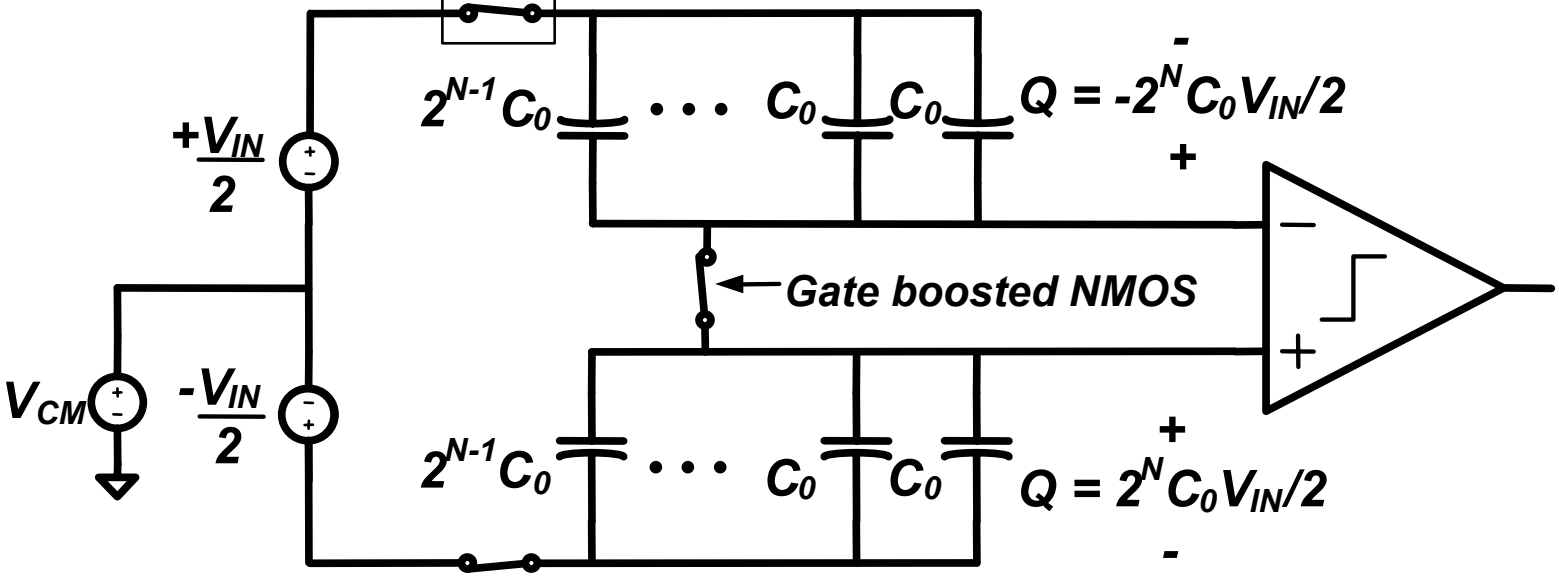
Common Mode Independent Sampling





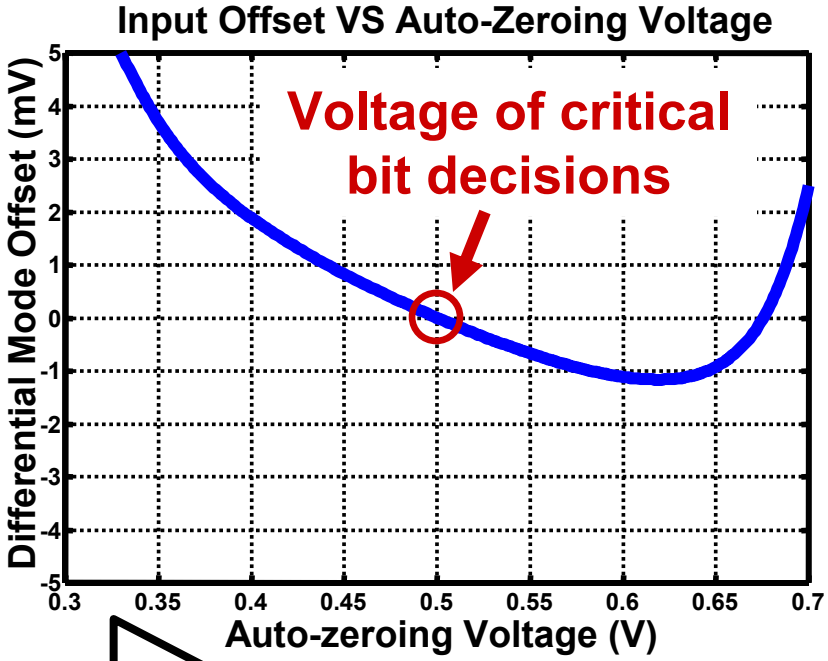
Set common mode by resetting capacitors and only sampling differential signal

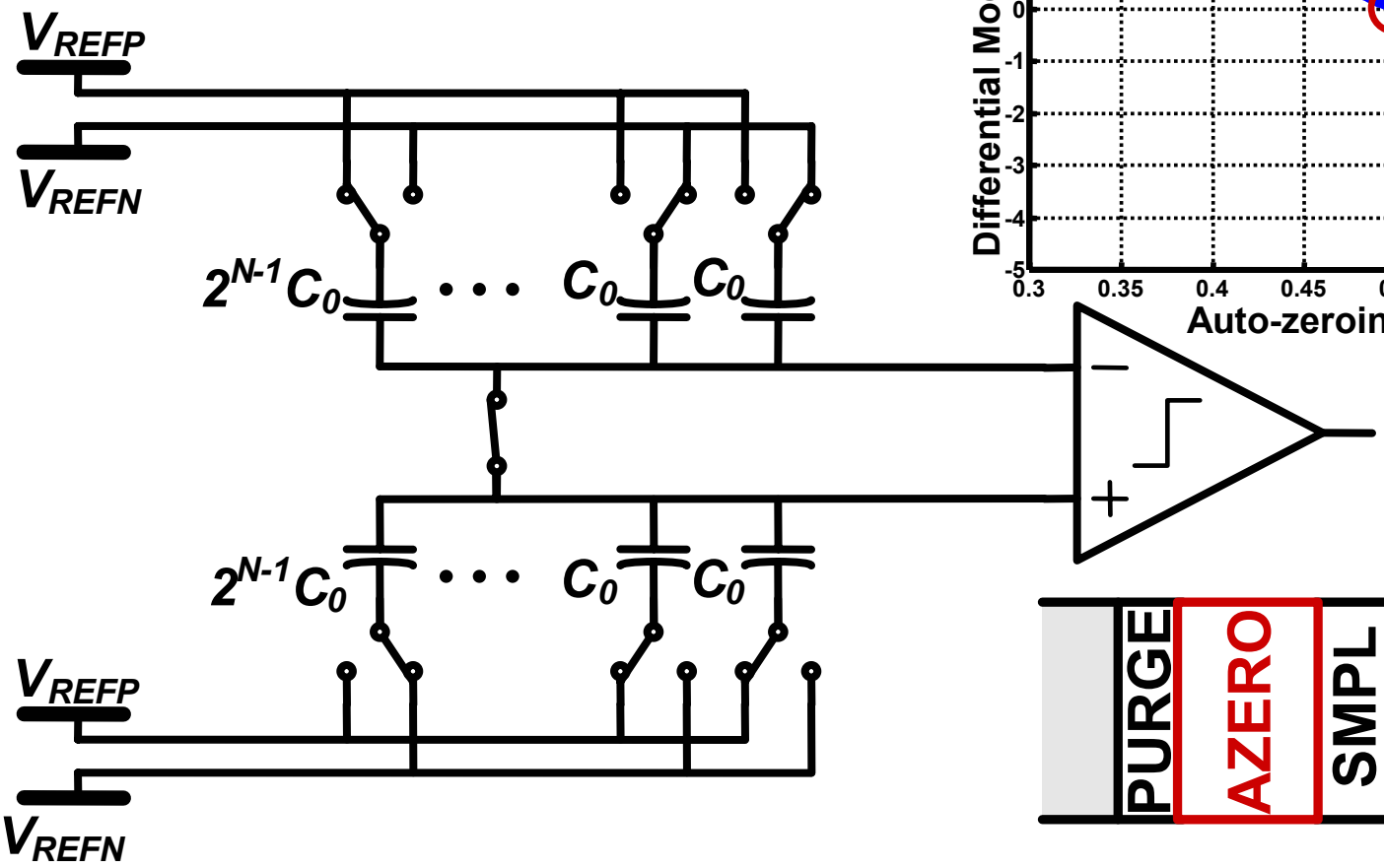


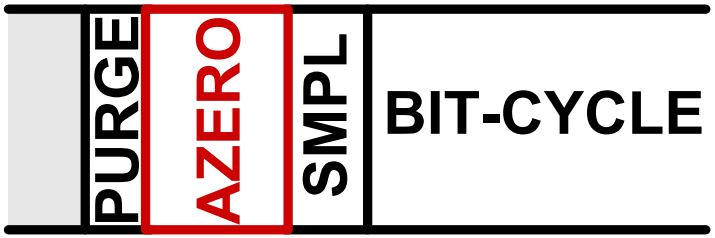


Preamplifier Common-Mode Rejection

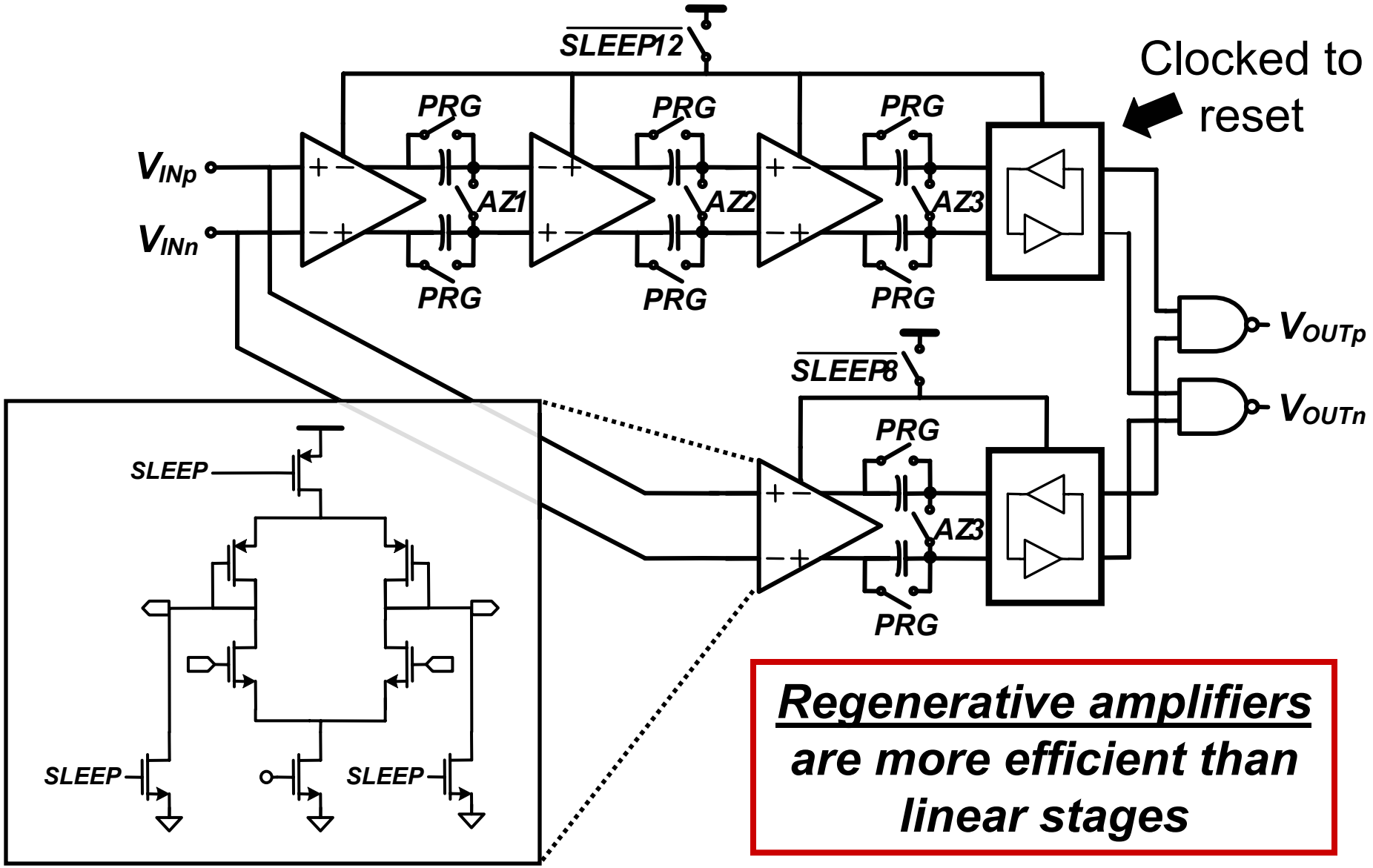
Auto-zero preamplifiers to voltage of critical SAR decisions





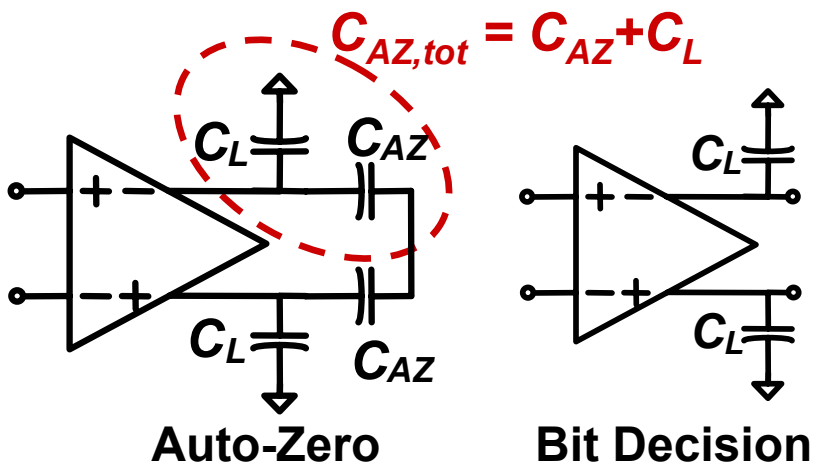


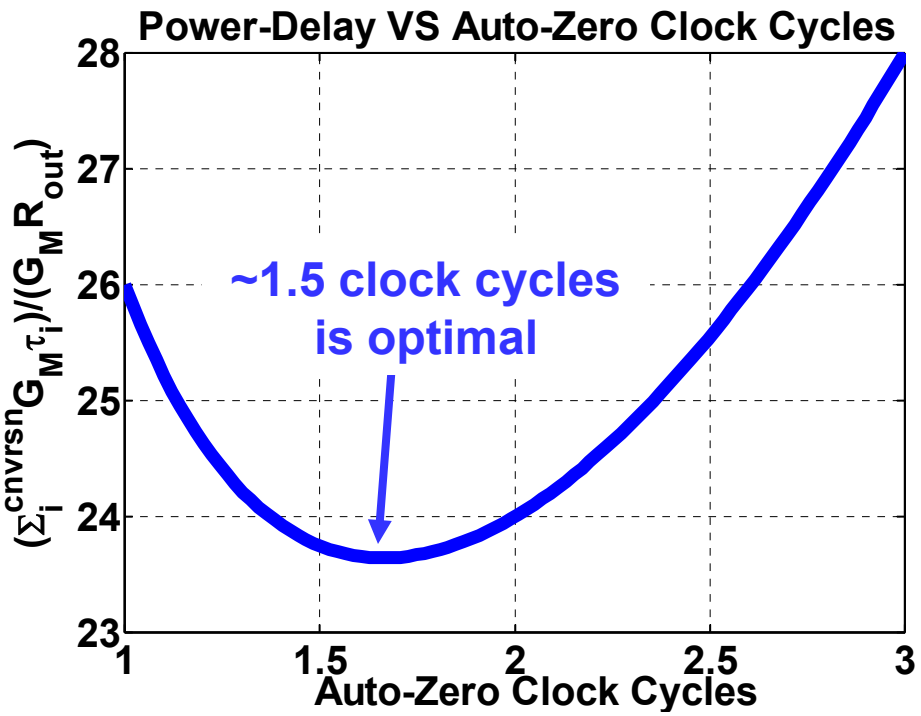
Scalable Comparator



Regenerative amplifiers ***are more efficient than linear stages***

Preamplifier Optimization





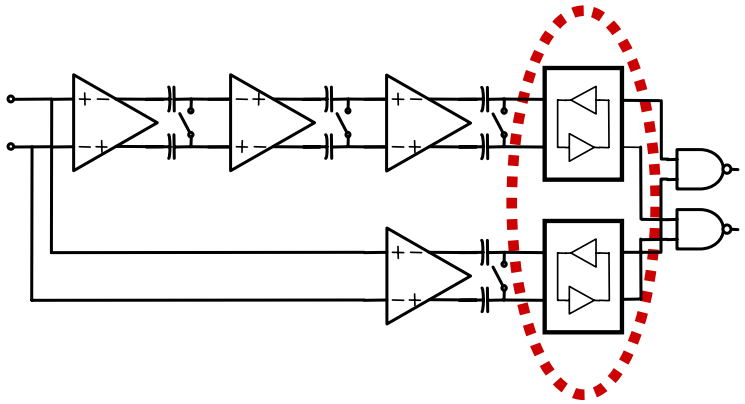
$$\overline{v^2}_{no,tot} \propto 1/C_L + 1/C_{AZ,tot}$$

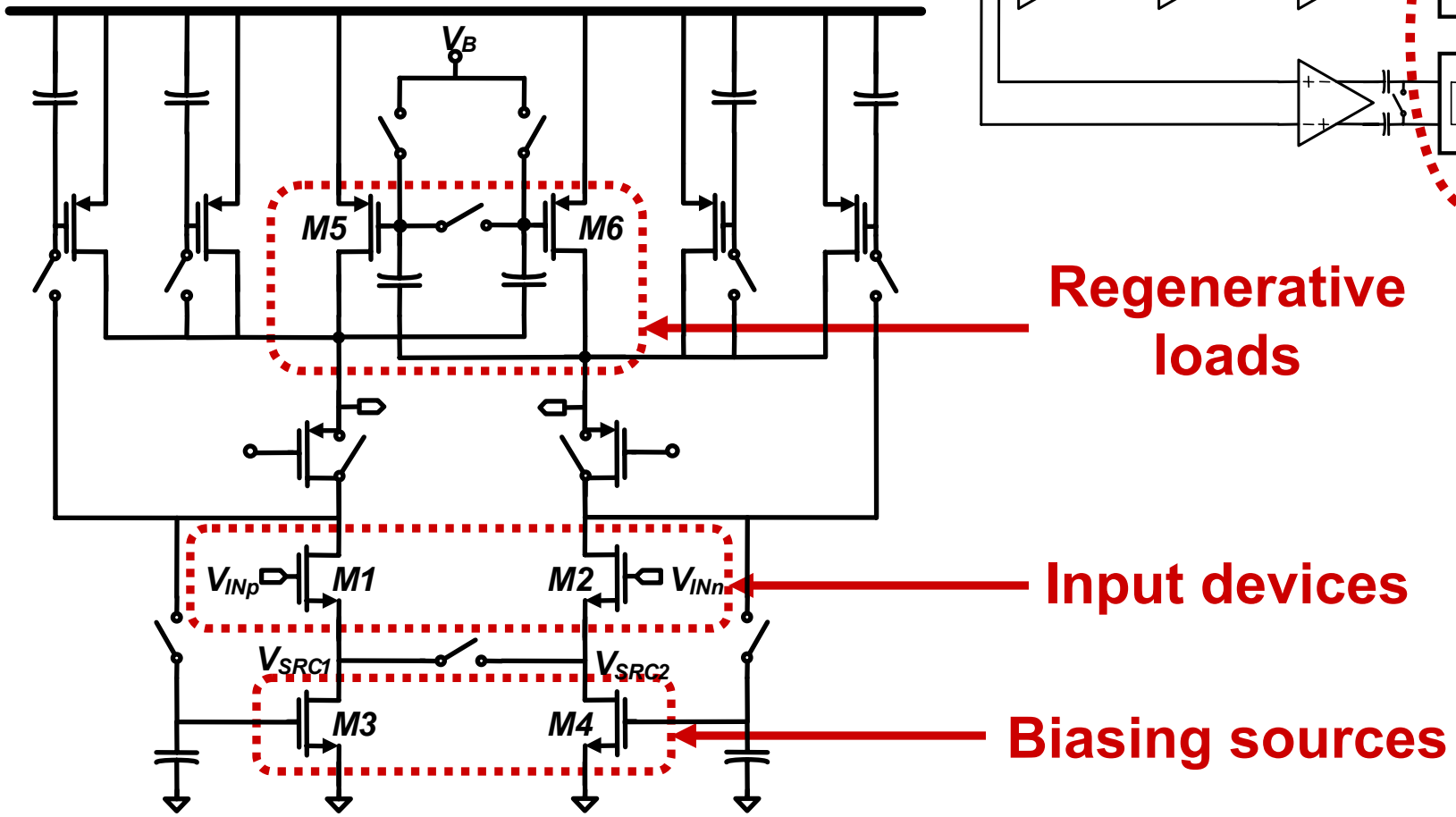
Reduce the auto-zeroing noise at the cost of increased settling time

For K auto-zero cycles: $1/K = \tau_{bit\text{-}cycle}/\tau_{AZ} = R_{OUT}C_L/R_{OUT}C_{AZ,tot} = C_L/C_{AZ,tot}$

Power-Delay: $\sum_{i=1}^{K+12} G_M\tau_i = KG_MR_{OUT}C_{AZ,tot} + 12G_MR_{OUT}C_L$

Offset Compensating Latch



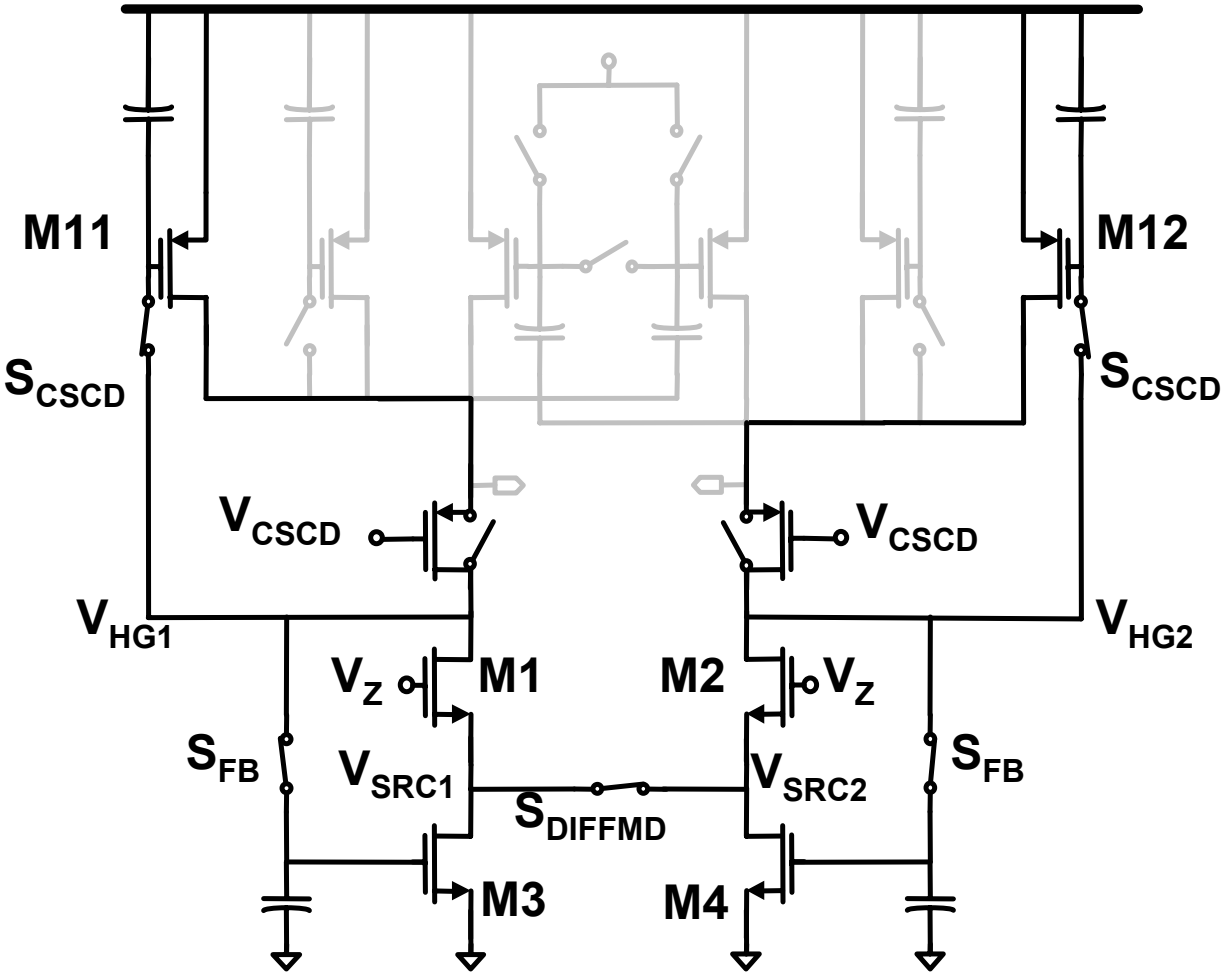


Regenerative loads

Input devices

Biasing sources

Offset Compensating Latch
(Auto-Zero Phase I)

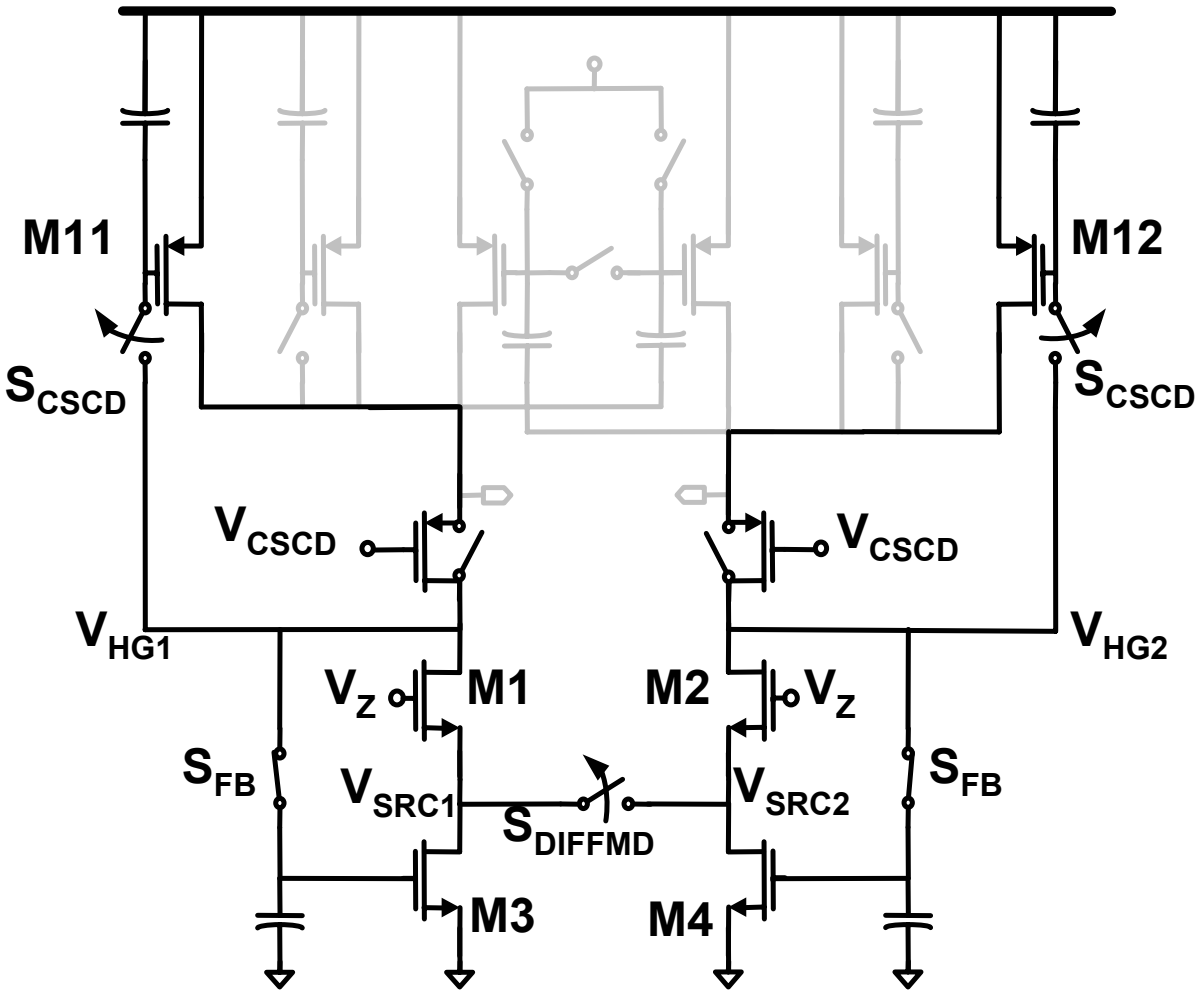


Purpose:
Bias M3, M4 so $V_{SRC1}=V_{SRC2}$

Close S_{CSCD}, S_{DIFFMD}, S_{FB}

- **$V_{SRC1}=V_{SRC2}$**
- **Bias M3,M4, M11, M12**

Offset Compensating Latch
(Auto-Zero Phase II)



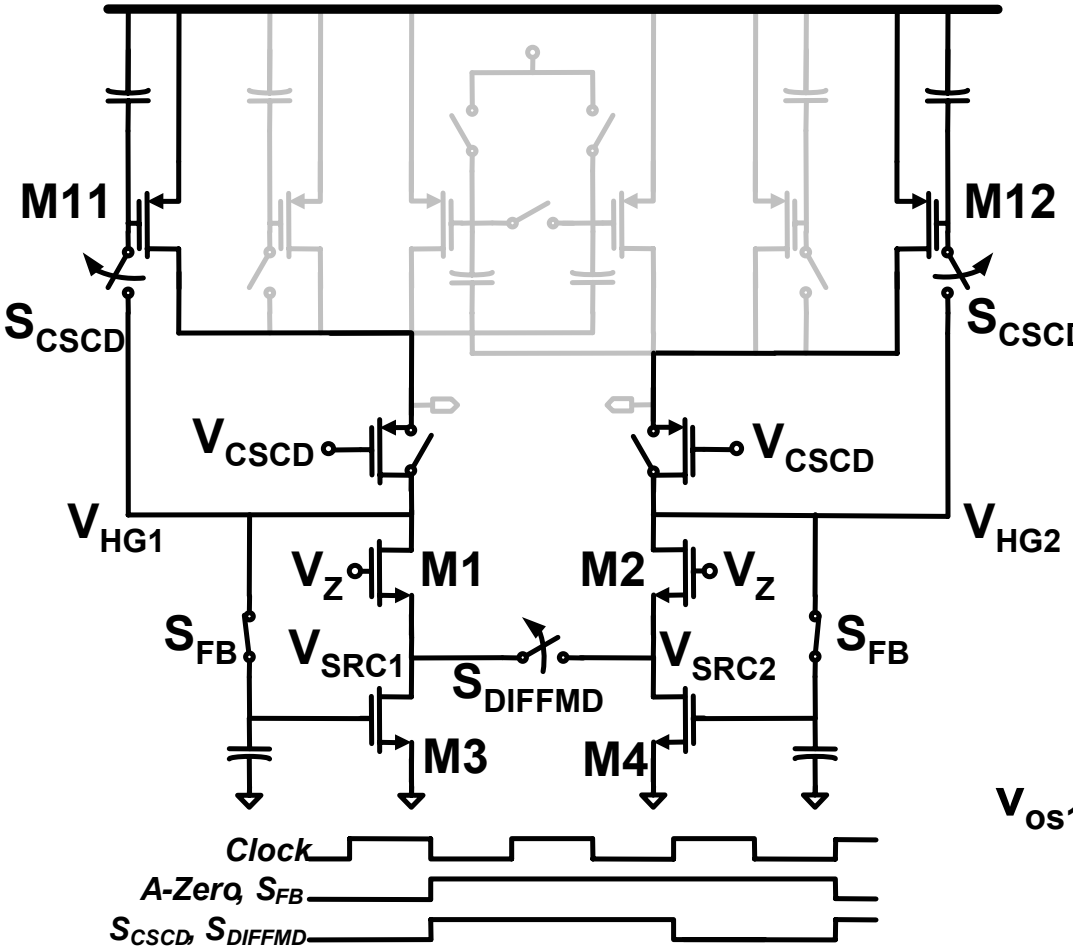
Purpose:
Bias M3, M4 so $V_{SRC1}=V_{SRC2}$

Open S_{CSCD}, S_{DIFFMD}

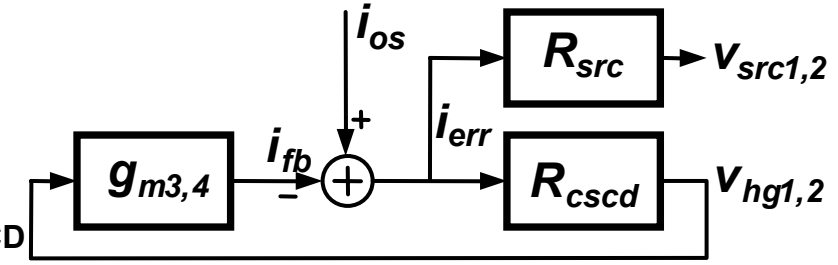
- **V_{HG1}, V_{HG2} are high impedance**
- **Branch currents change due to offsets**
- **Feedback loops restore currents**

Offset Compensating Latch
(Auto-Zero Phase)

Reduces offset, $V_{OS1,2}$, at $V_{SRC1,2}$ by $\approx 1/g_m r_o$



Feedback block

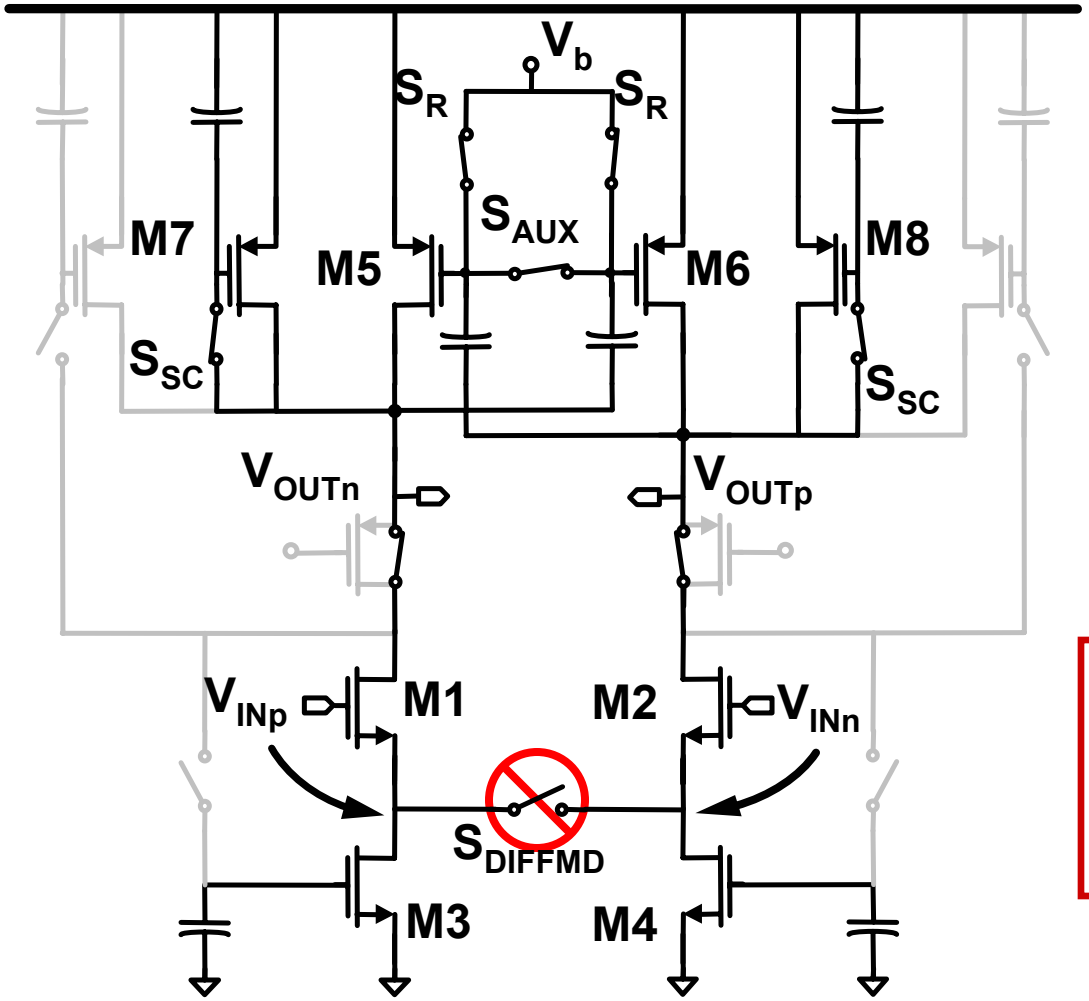


$$R_{SRC} \approx r_{o3,4} \; ; \; R_{CSCD} \approx g_{m1,2} r_{o3,4} r_{o1,2}$$

$$v_{src1,2} \approx \frac{i_{os}}{g_{m3,4} g_{m1,2} r_{o1,2}}$$

$$v_{os1,2} \approx i_{os}/g_{m1,2} \rightarrow \boxed{v_{src1,2} \approx \frac{v_{os1,2}}{g_{m3,4} r_{o1,2}}}$$

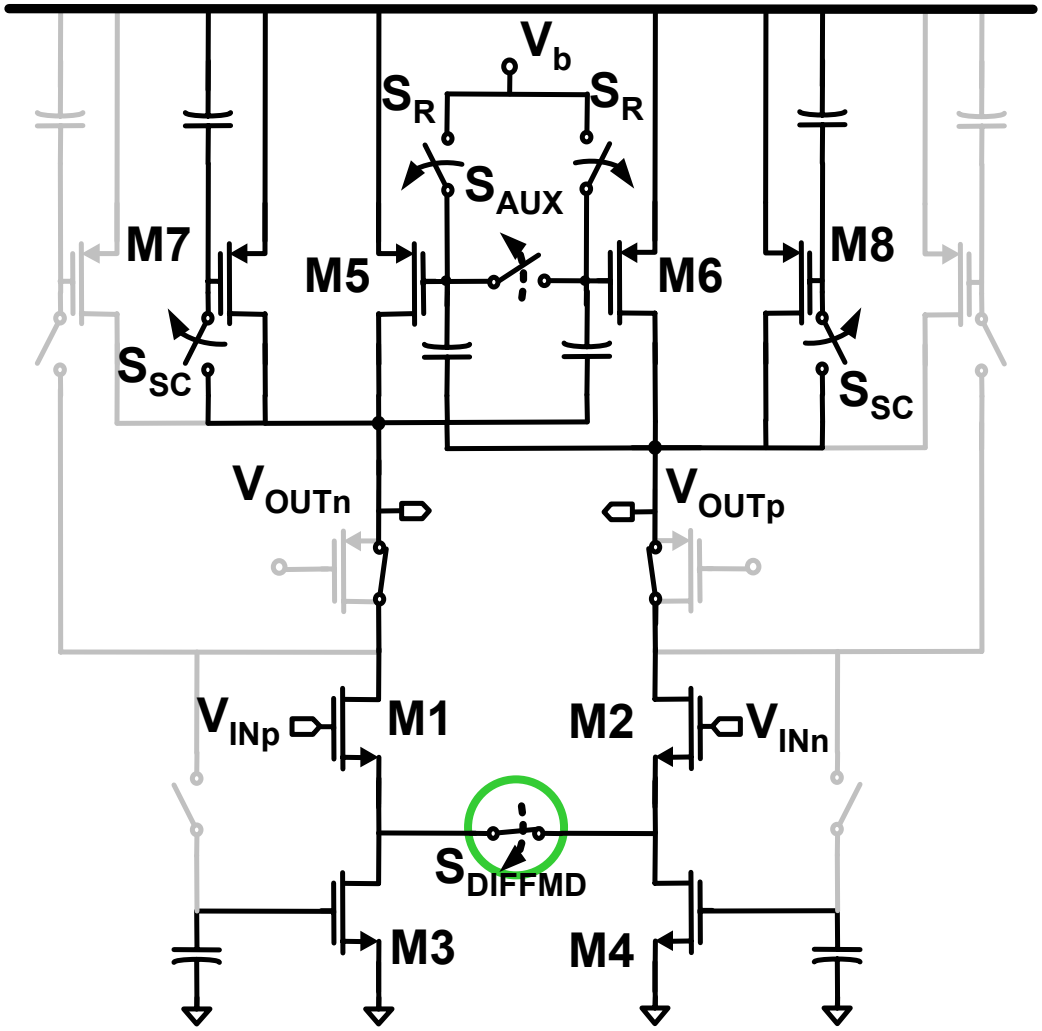
Offset Compensating Latch
(Reset-Resolve Phase I)



- Input voltages appear at source nodes
- Branch currents are set only by M3 and M4

Loads are held stable for given branch currents

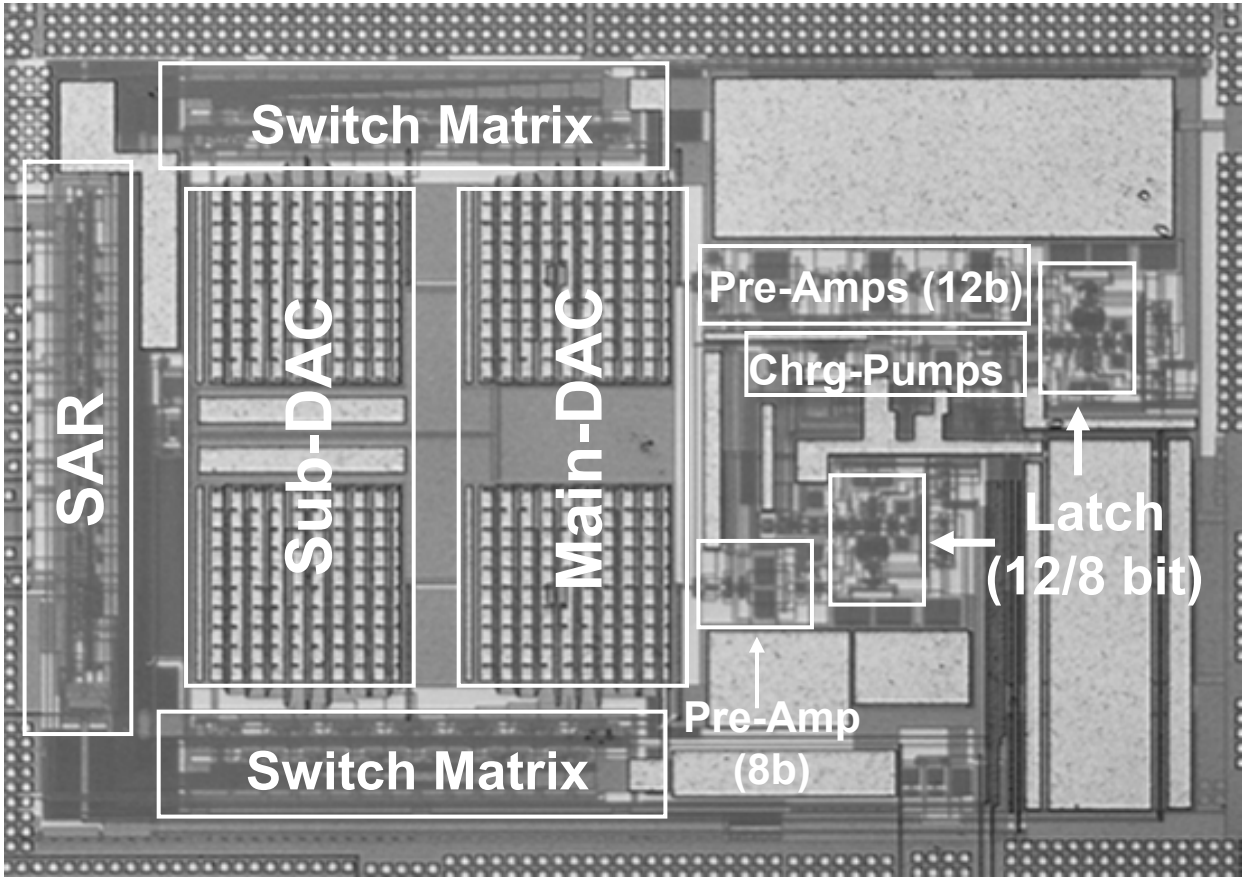
Offset Compensating Latch
(Reset-Resolve Phase II)



- Opening S_R and S_{AUX} makes loads metastable
- Closing S_{DIFFMD} perturbs the branch currents depending on the inputs

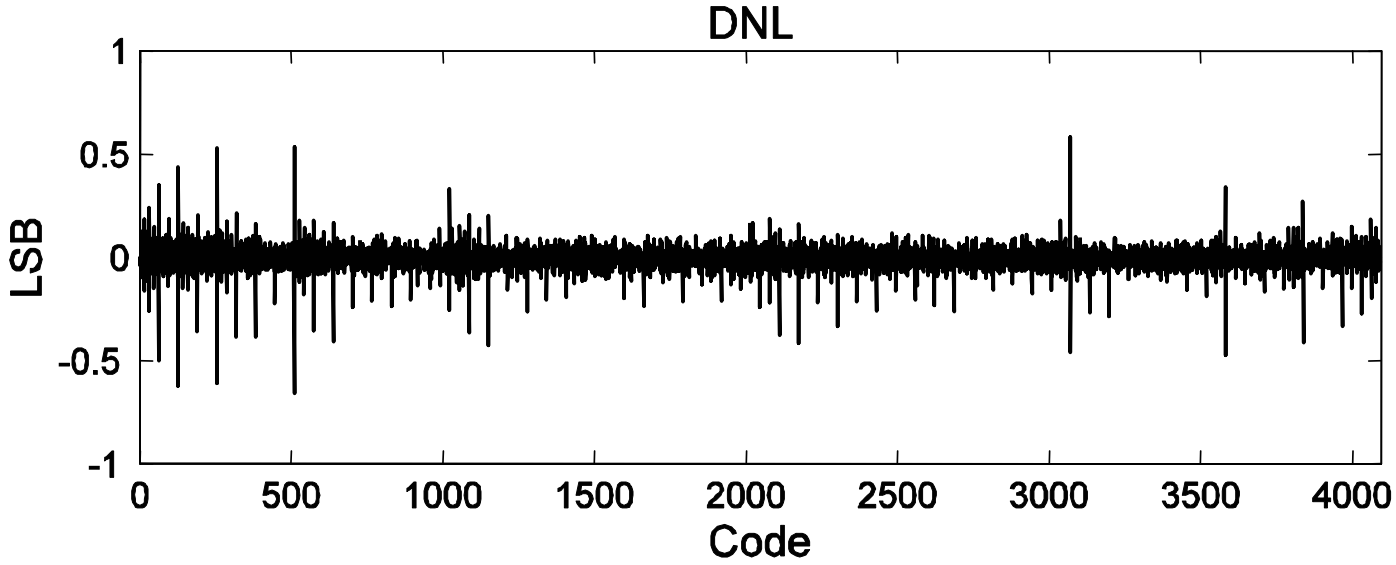
Input is applied to regenerative loads by shorting source nodes

Prototype ADC

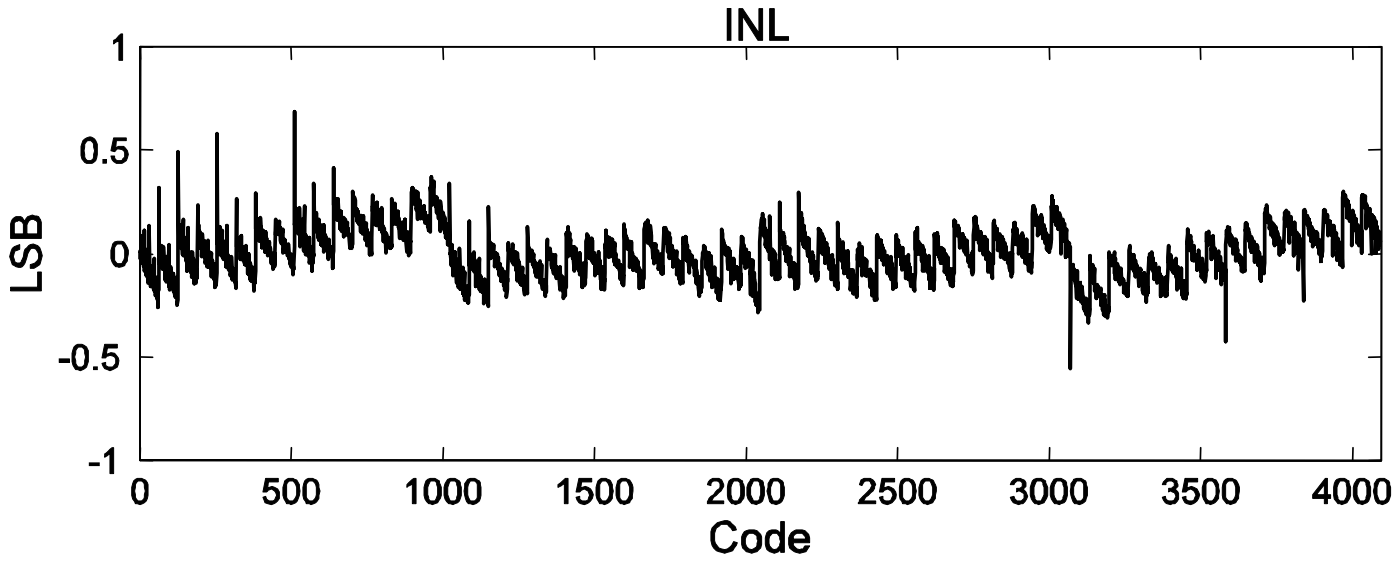


0.18µm 5M2P CMOS

Measured DNL/INL

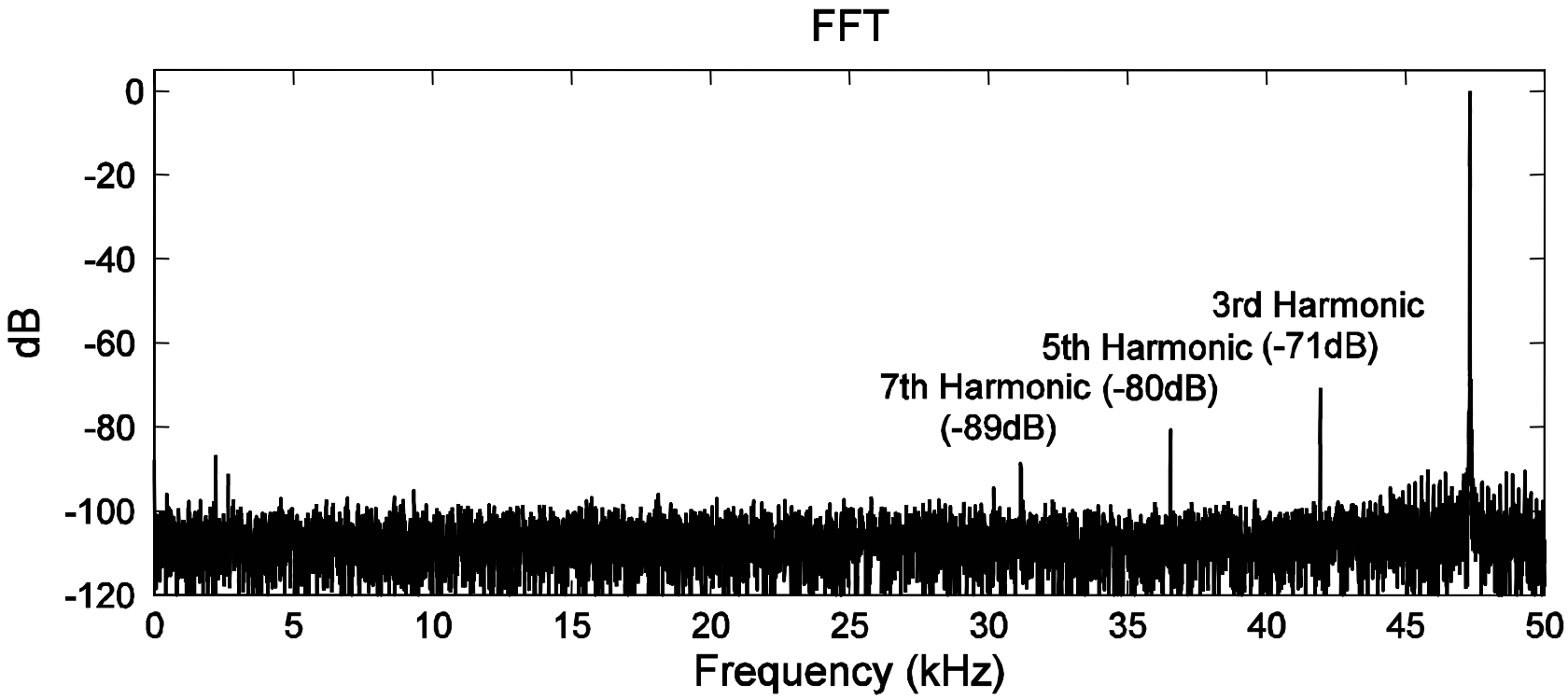


+0.58LSB
-0.66LSB



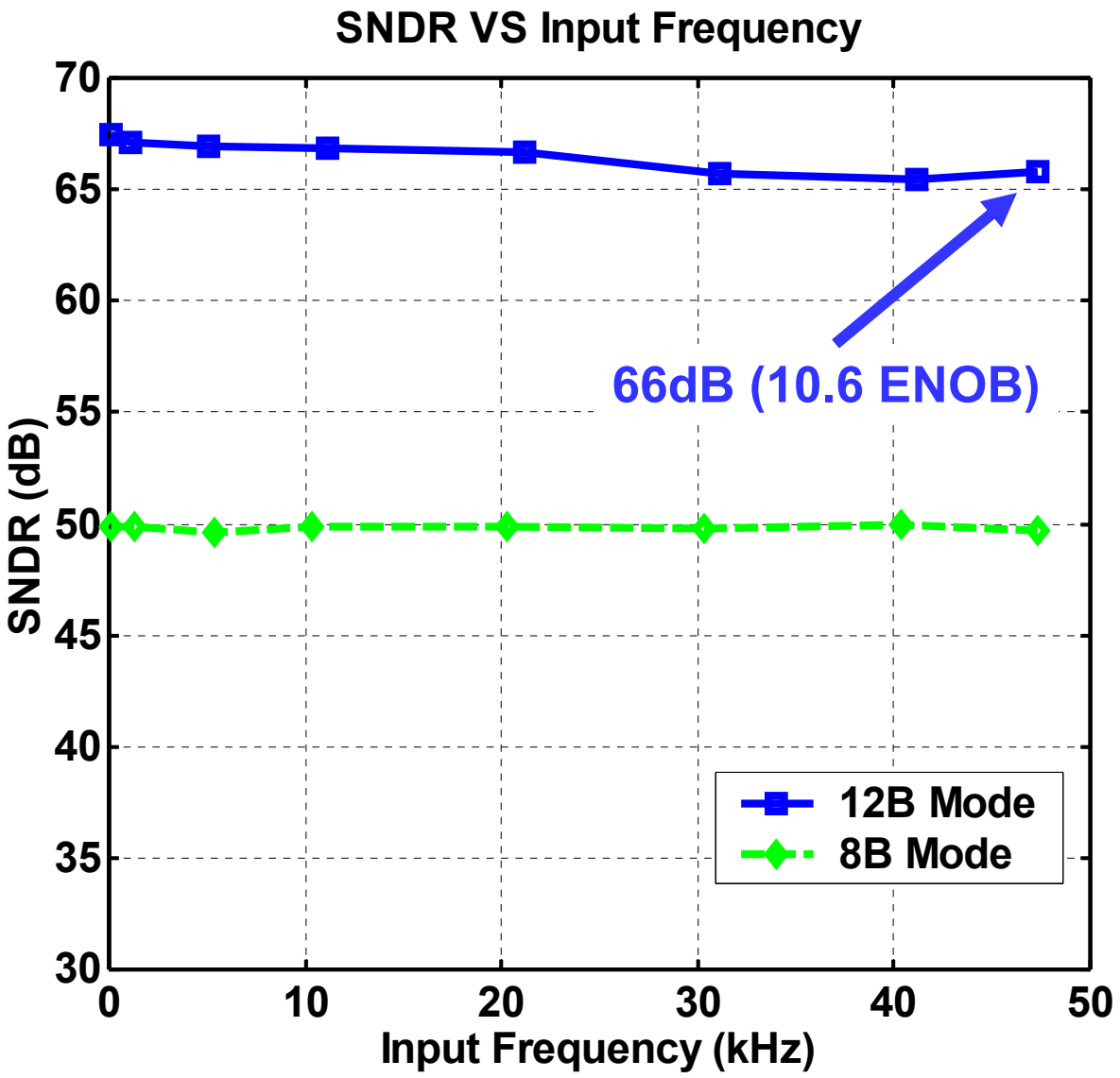
+0.68LSB
-0.56LSB

Measured FFT



F_S=100kS/s, F_{IN}=48kHz

Measured SNDR



Measured Power

Block(s)	Simulated Power	Measured Power
SAR, Switch Matrices	8.7μW	8.4μW
Charge Pumps	0.39μW	0.38μW
Pre-Amplifiers	4.9μW	5.8μW
Latch	3.9μW	5.2μW
Ref. Supply	5.9μW	5.3μW
Total	**23.8μW**	**25μW**

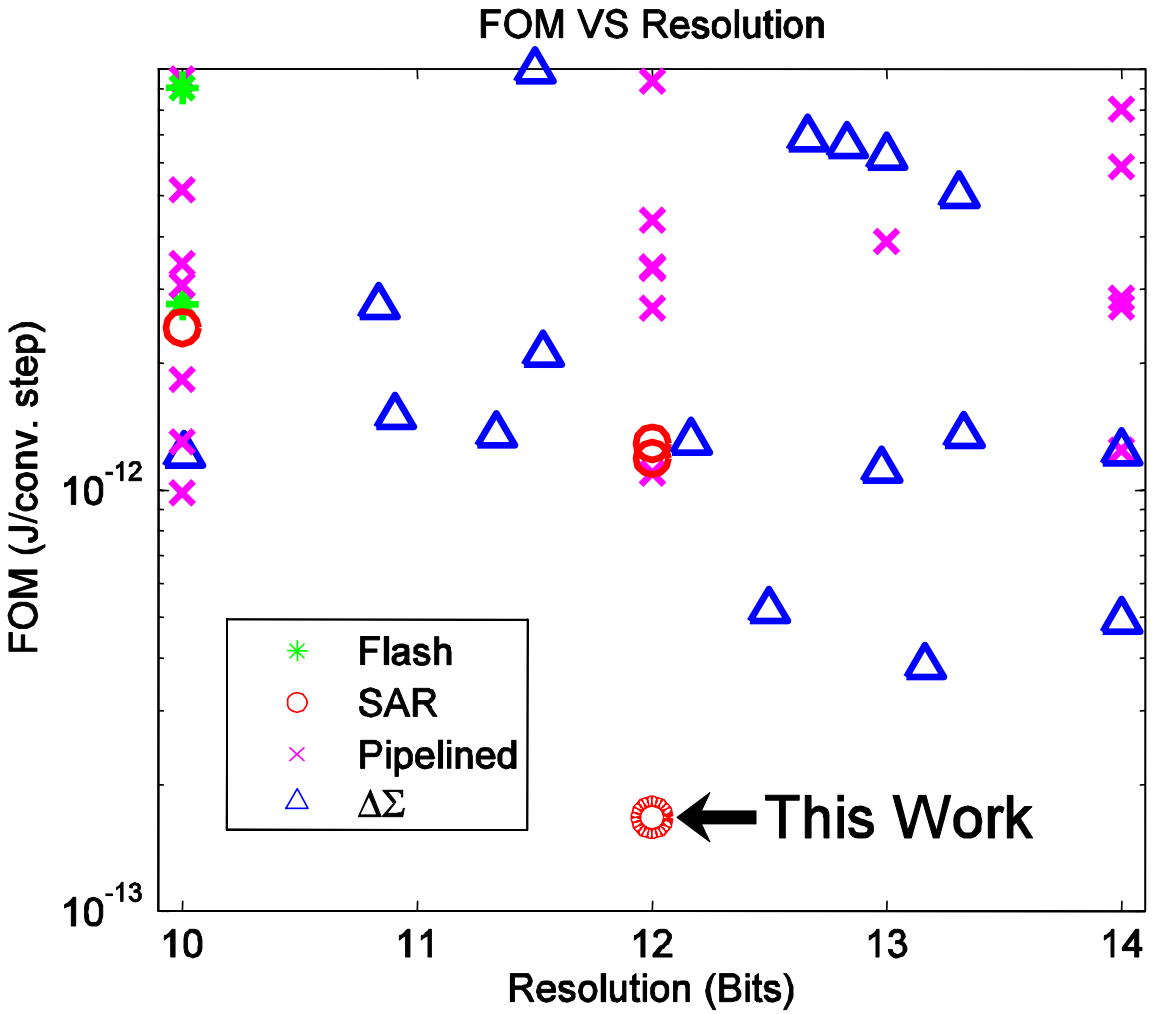
12b mode, 100kS/s

Performance Summary

	8 Bit Mode	12 Bit Mode
Process	0.18µm CMOS, National Semiconductor	
Area	900µm X 700µm	
Voltage Supply	1V	
Clock Frequency	4MHz	2MHz
Resolution	8 Bits	12 Bits
Maximum Sampling Rate	200kS/s	100kS/s
Power Consumption	19µW @ 100kS/s	25µW @ 100kS/s
SNDR (at Nyquist)	49.7dB (F_{in}=100Hz)	65.3dB (F_{in}=50Hz)
ENOB (at Nyquist)	7.96 Bits (F_{in}=100Hz)	10.55 Bits (F_{in}=50Hz)
SFDR (at Nyquist)	63.2dB (F_{in}=100Hz)	71dB (F_{in}=50Hz)

Figure-of-Merit

$$FOM = \frac{P}{2^{ENOB} 2F_{IN}}$$



Conclusions

- Ultra-low power SAR ADC
  (FOM: 165fJ/conv.step)
- Absence of active linear blocks and analog switches allows low supply (1V)
- Offset compensating regenerative latch efficiently eases linear gain requirement

Acknowledgments: Funding provided by DARPA, IC fabrication provided by National Semiconductor.