A 65nm 8T Sub-V_t SRAM Employing Sense-Amplifier Redundancy

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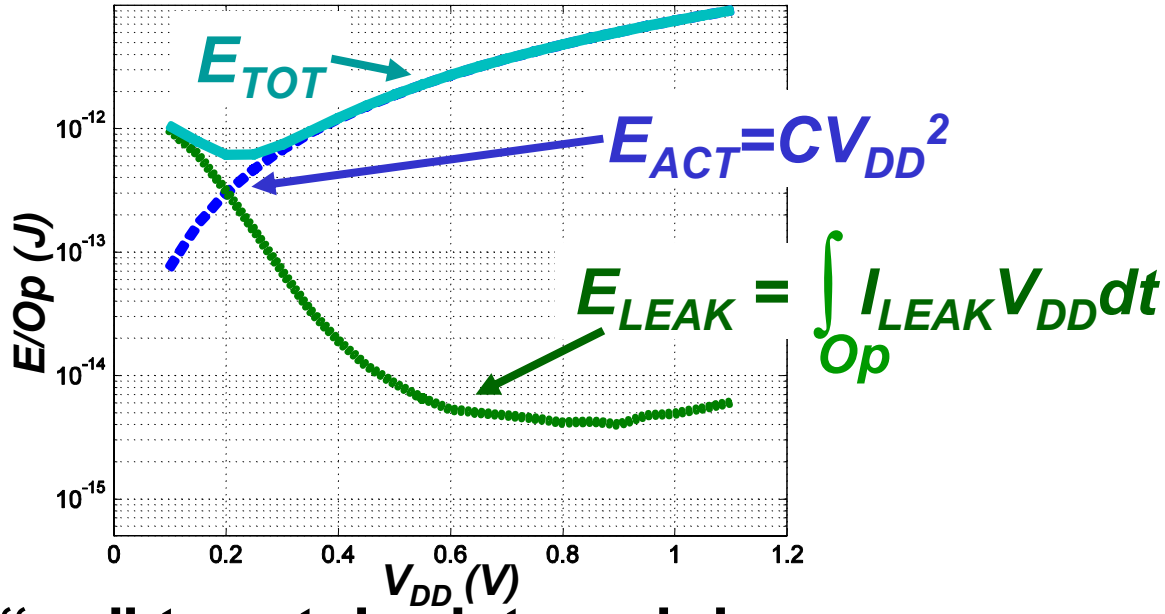
Energy Minimization

- Minimum energy V_{DD} for logic results from opposing active and leakage components

Simulation of CLA adder



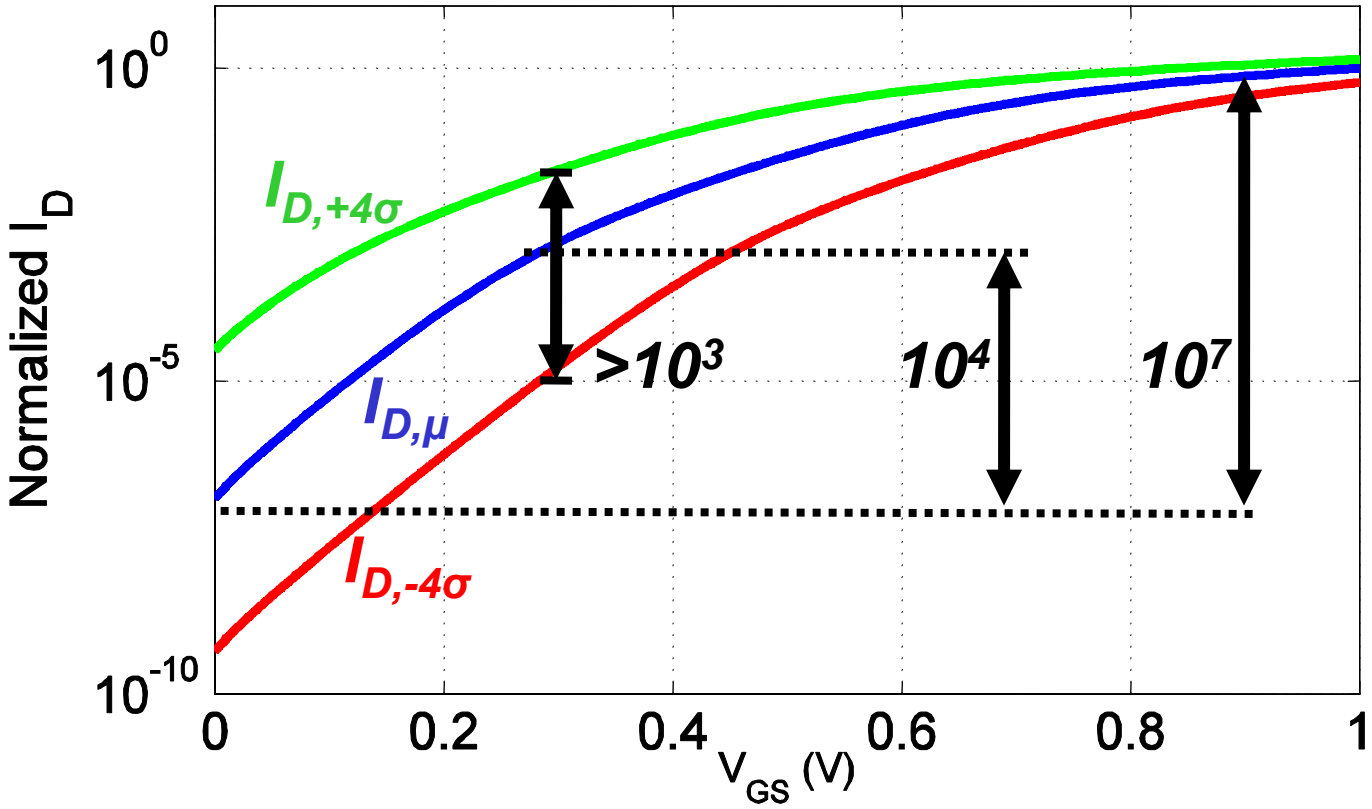
- SRAMs remain "on" to retain data: minimum energy V_{DD} is lowest functional V_{DD}
  - DIBL reduces I_{LEAK} by 4x from 1V to 300mV

Voltage scaling gives power savings of >10x

Outline

- Low-voltage SRAM challenges
- Sub-V_t bit-cell
- Read/write peripheral circuit assists
- Sense-amplifier redundancy
- Prototype measurements
- Conclusions

Sub-V_t MOSFET Characteristic



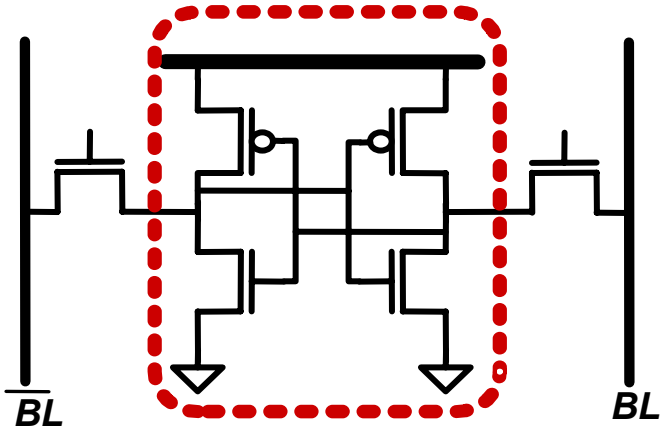
In Sub-V_t:

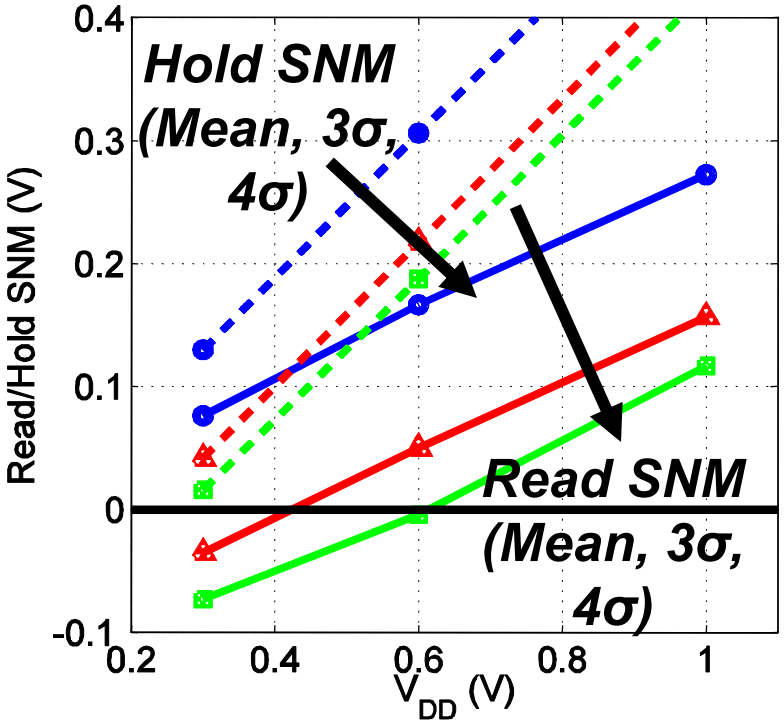
1) Device strength varies exponentially with V_t

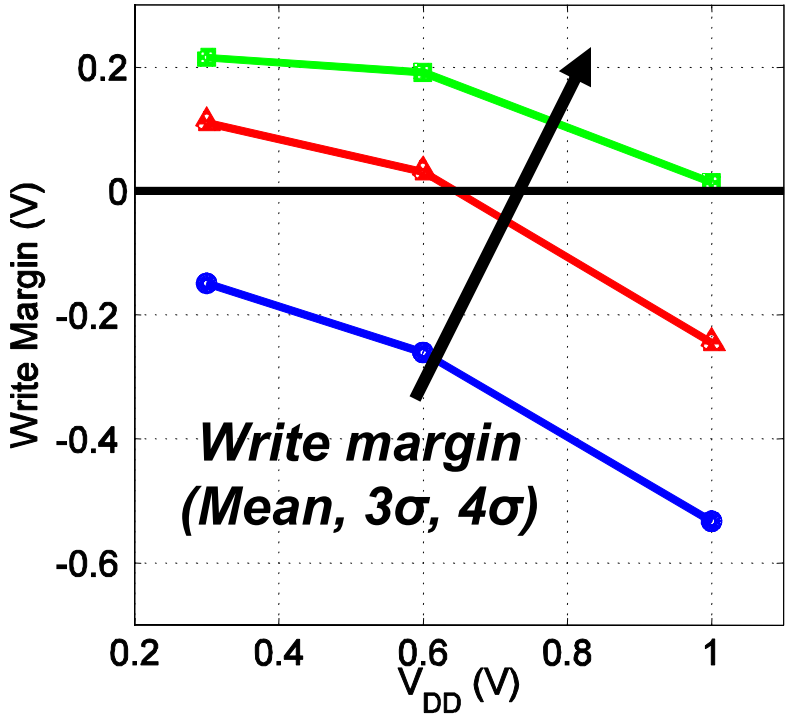
2) I_{ON}/I_{OFF} is severely degraded

6T Low Voltage Failures

Relative device strengths determine readabilty/writeability

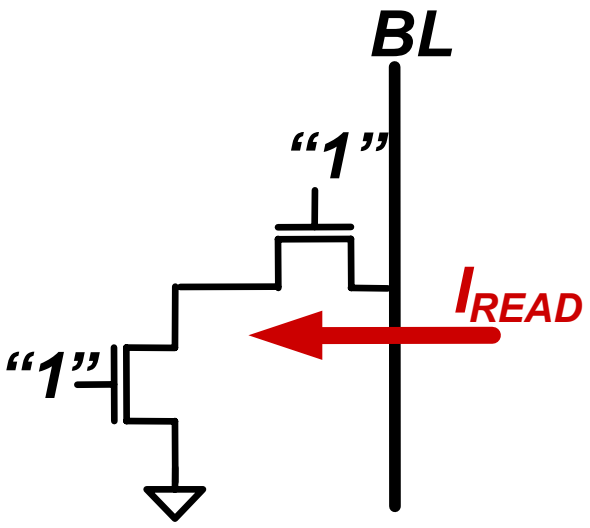


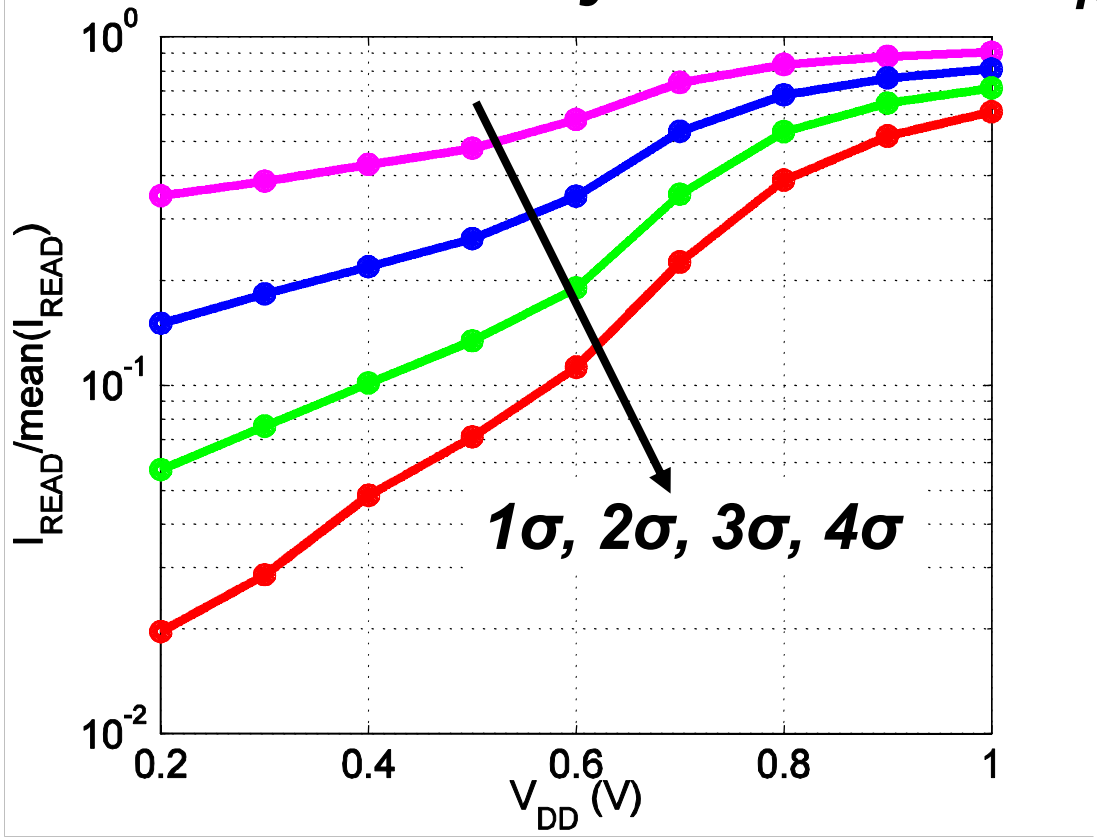




Read Current Distribution

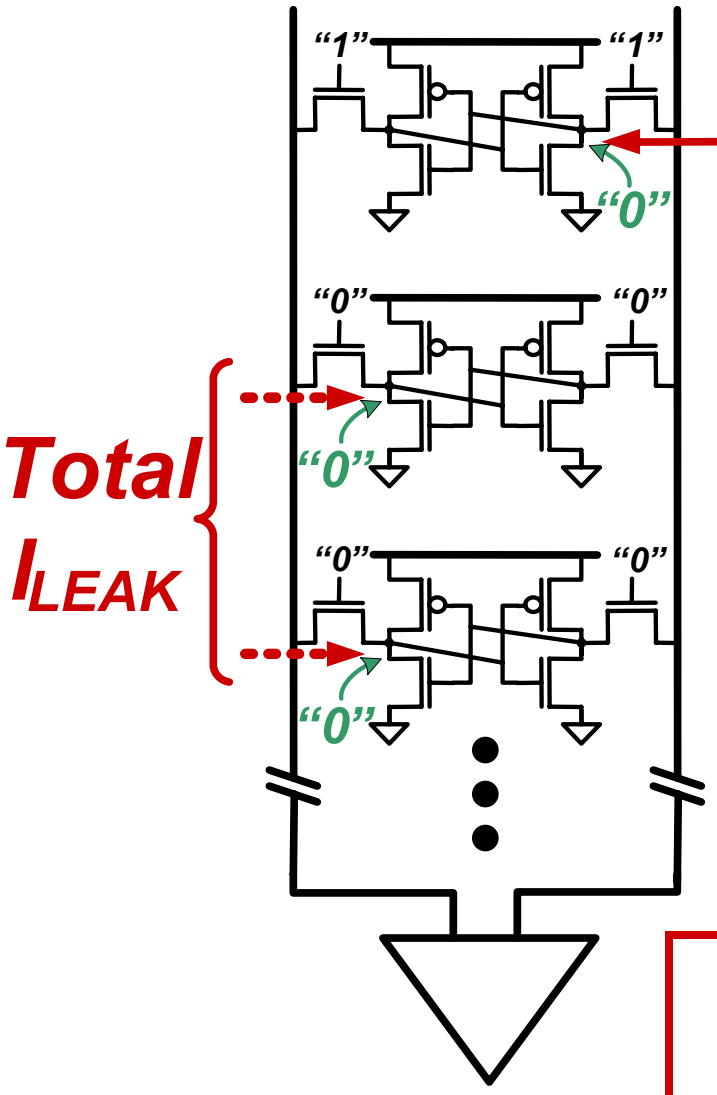
Array performance determined by worst-case I_{READ}

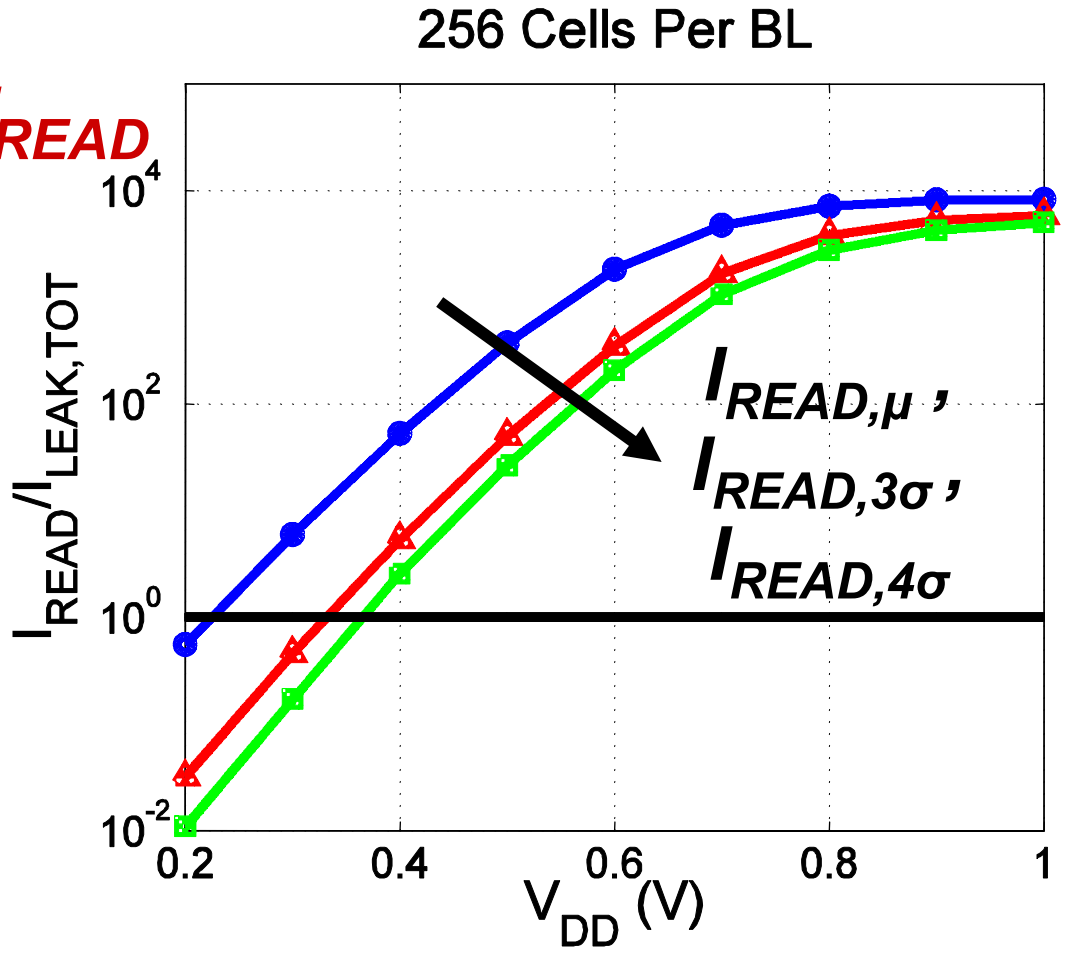




In sub-V_t, reduced overdrive lowers mean I_{READ}, and variation causes larger degradation of tail I_{READ}

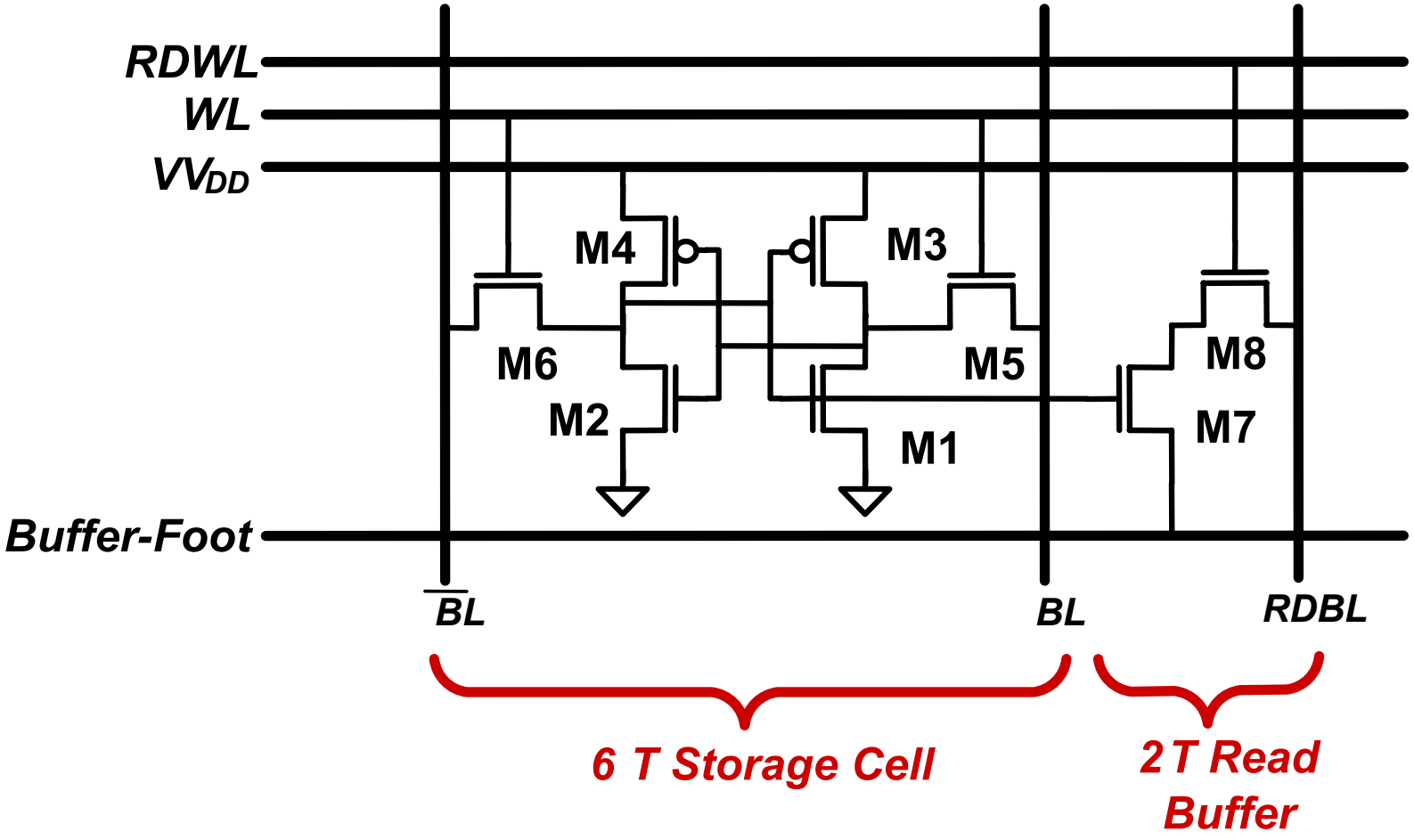
Bit-Line Leakage





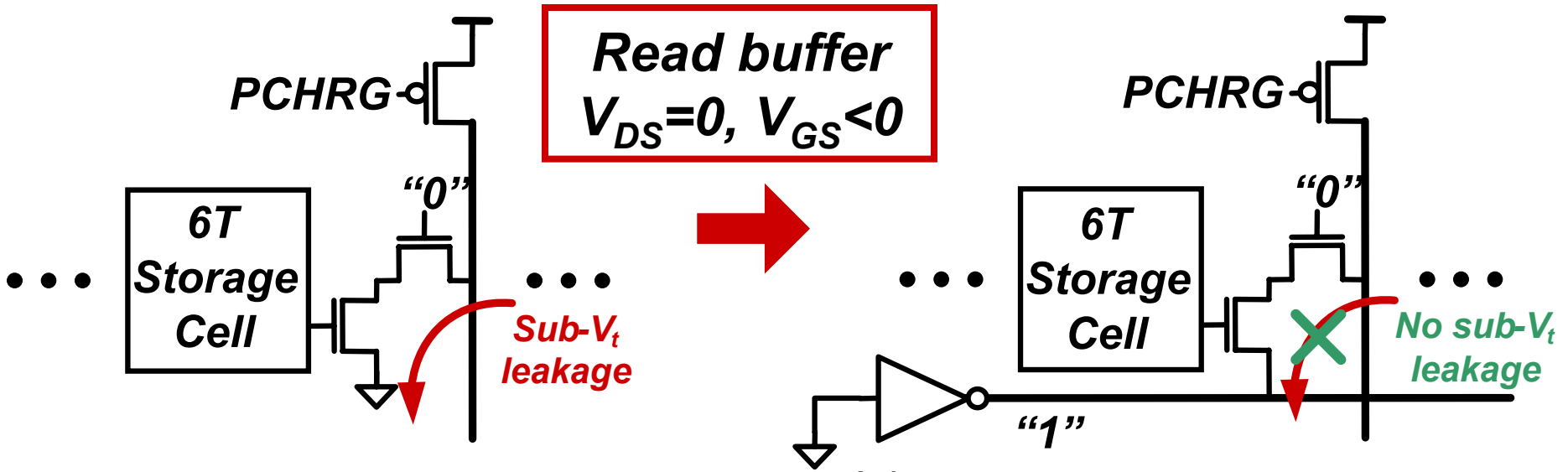
I_{LEAK} depends on stored data and can exceed I_{READ} at low voltages

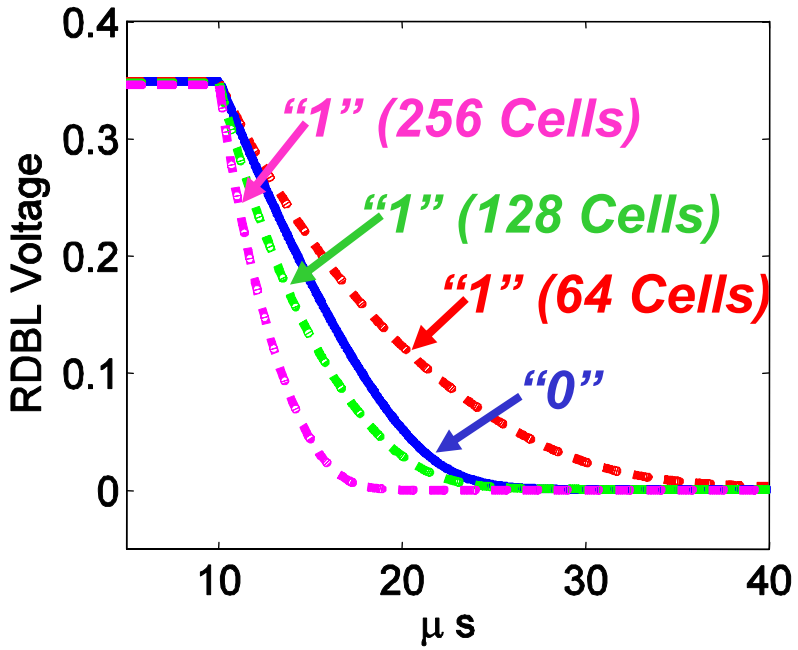
8T Bit-Cell For Sub-V_t SRAM

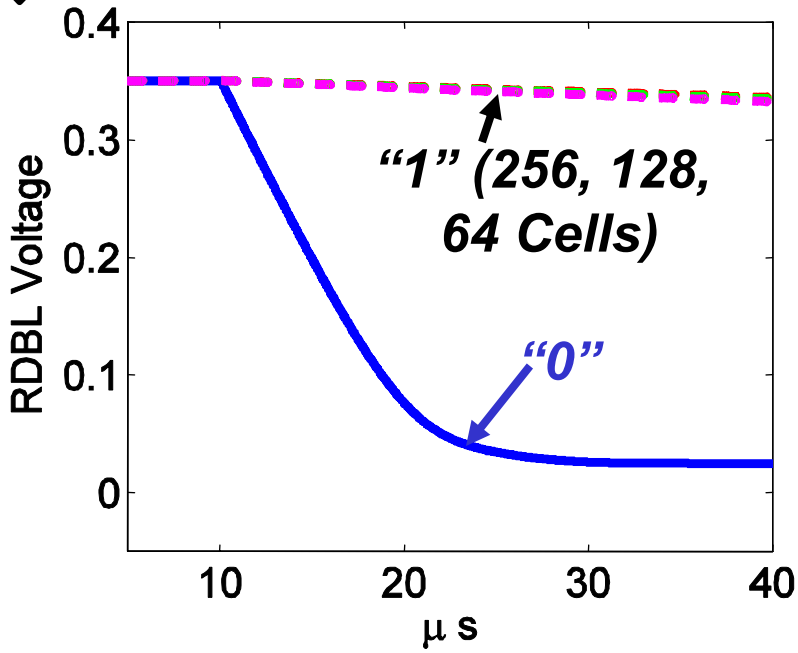


Buffer eliminates read SNM limitation, peripheral assists allow sub-V_t write and sensing

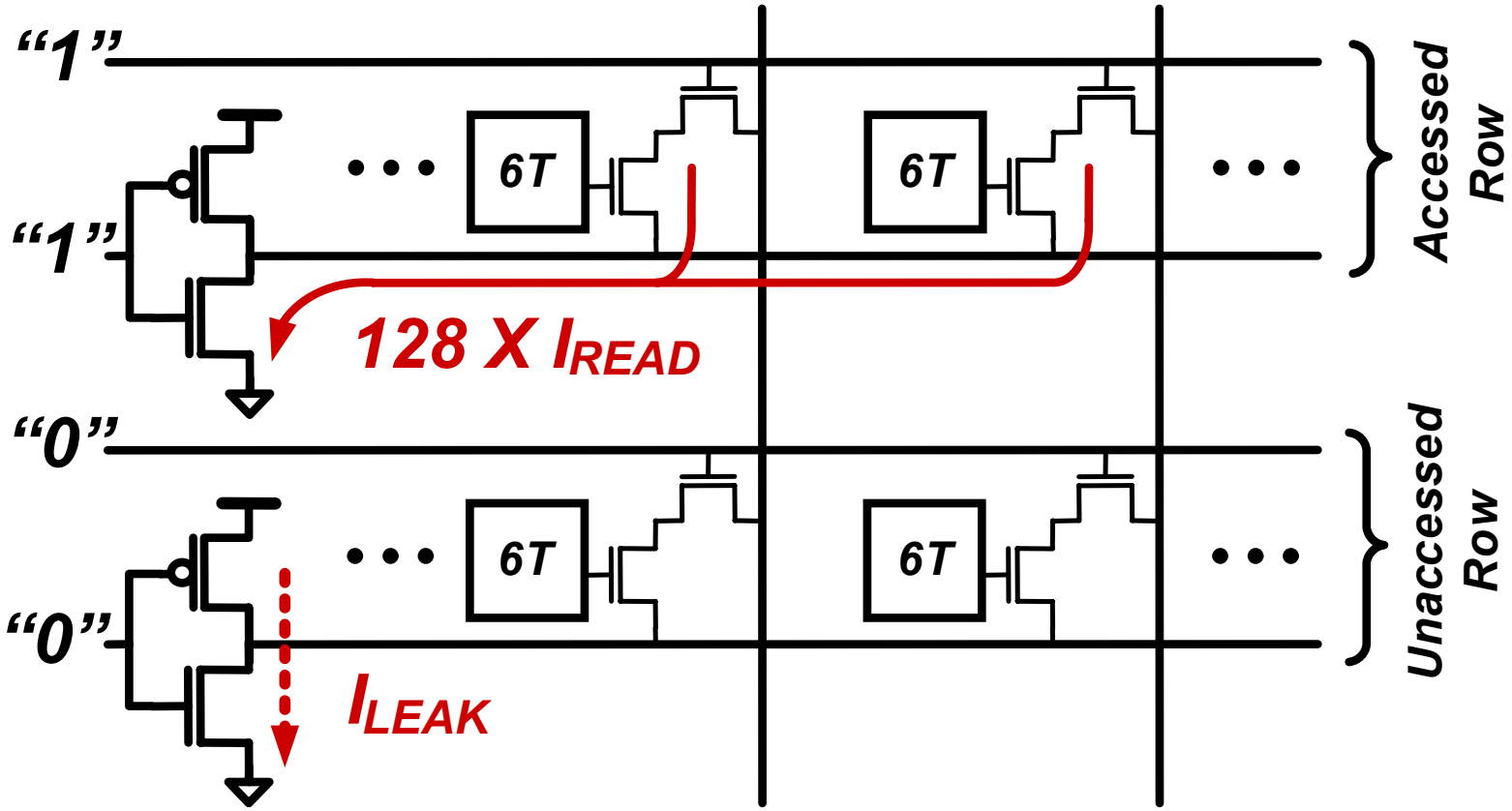
"Zero" Sub-V_t Leakage Read-Buffer





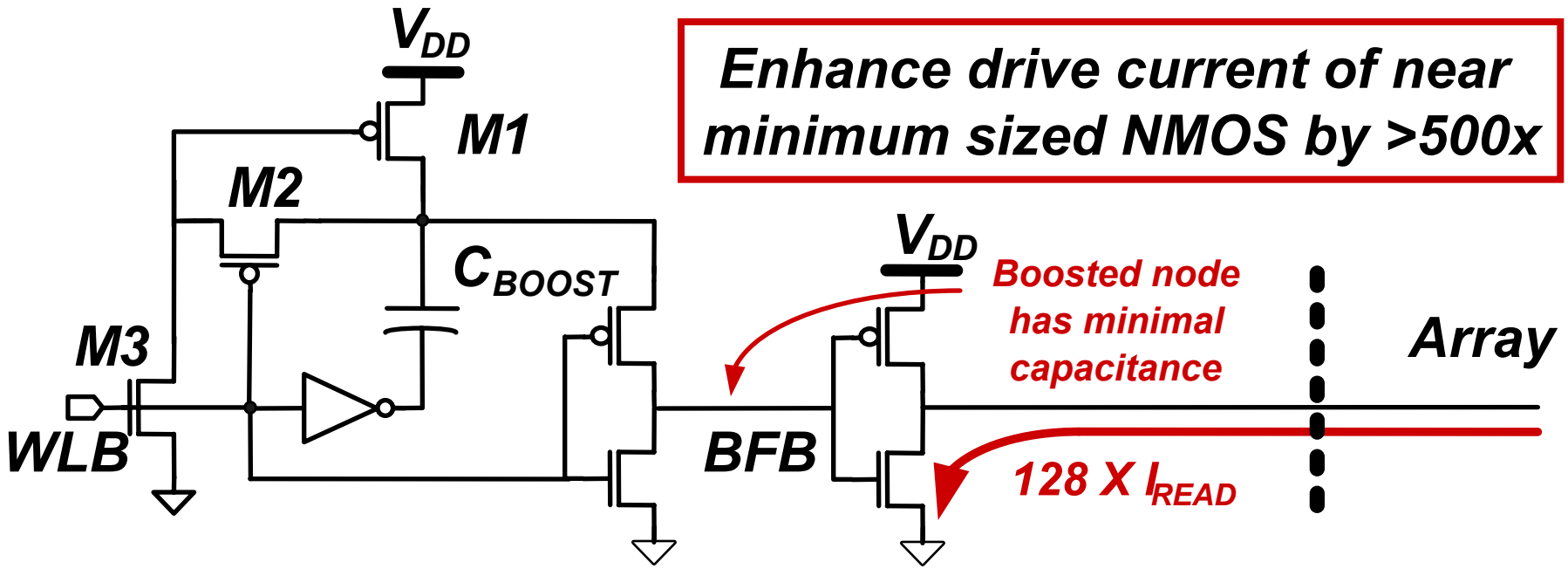


Read-Buffer Foot-Driver Limitation

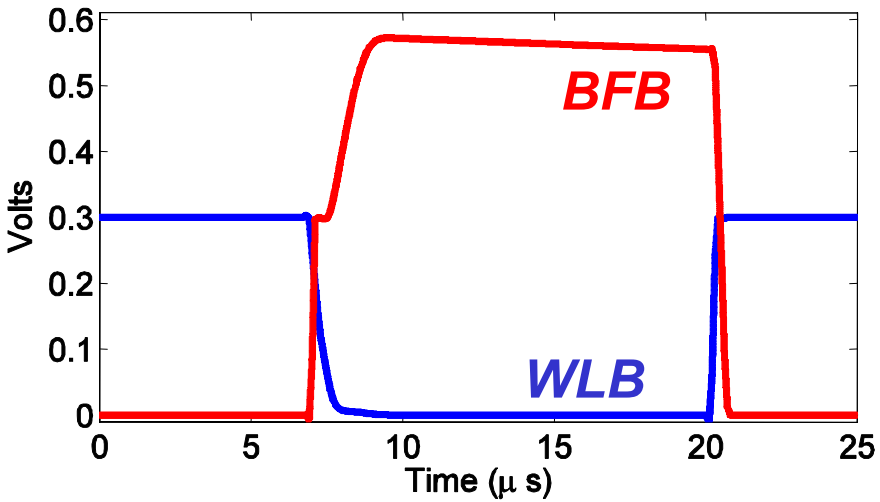


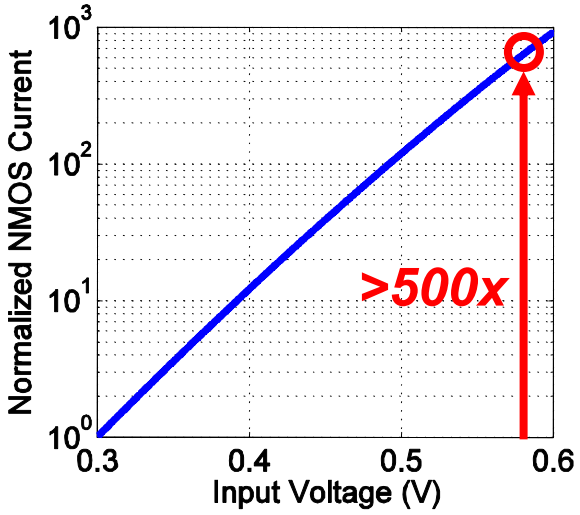
Read-buffer foot-driver must have strong drive current but consume minimal leakage power and area

Gate-Boosted Foot-Driver



Enhance drive current of near minimum sized NMOS by >500x

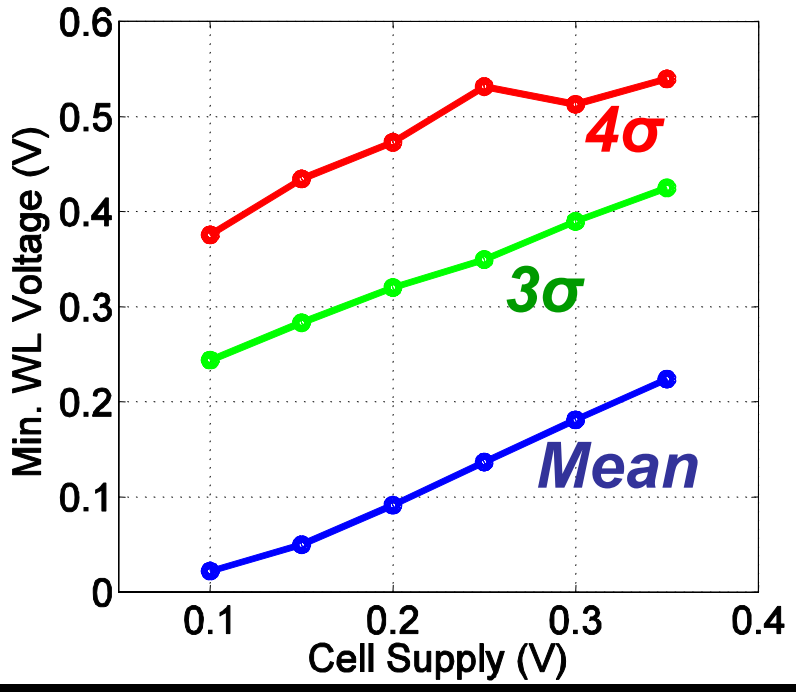




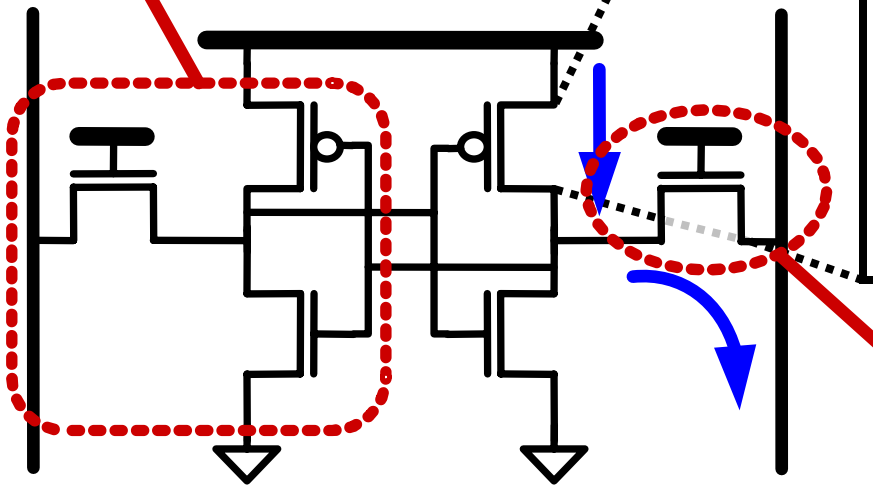
Sub-V_t Write

To ensure write, boost WL 50mV and reduce cell supply

Reduce gate drive



Adjust trip voltage

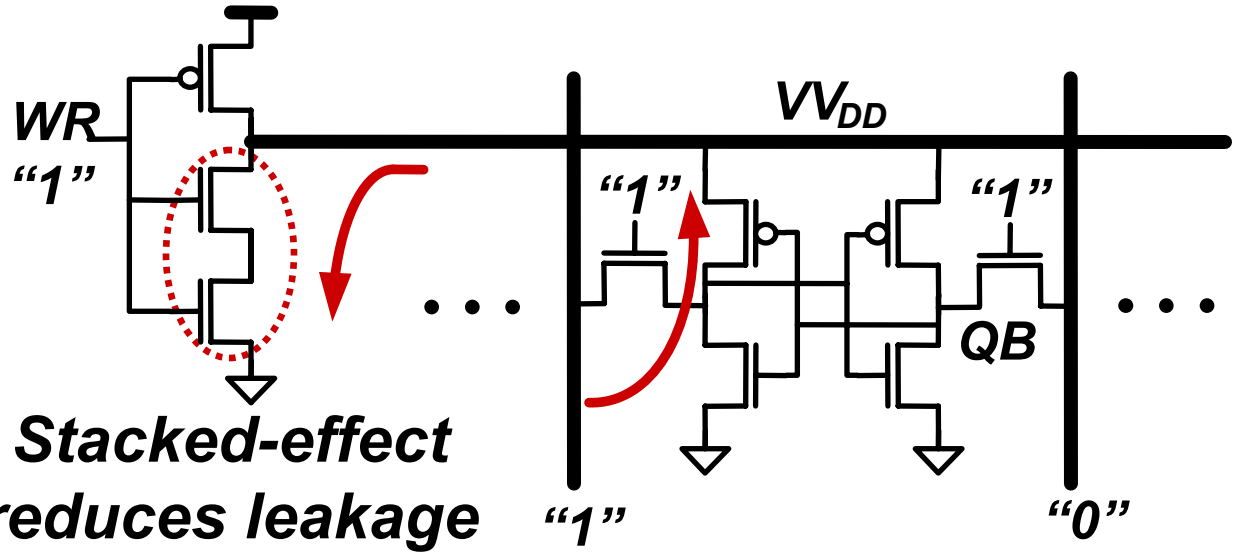


Increase gate drive

"1"

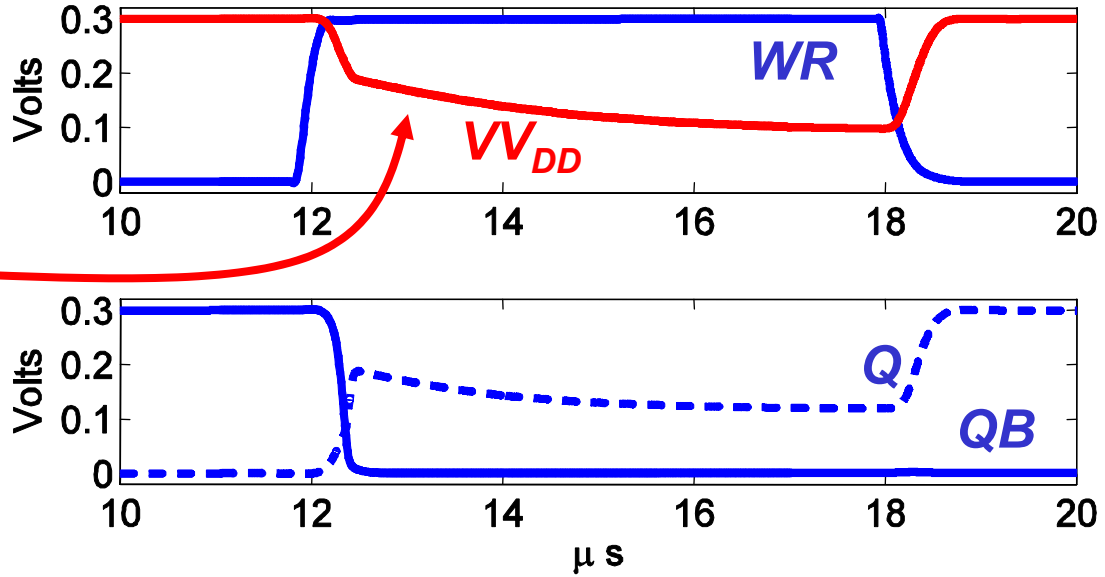
"0"

Virtual Cell Supply



Stacked-effect reduces leakage during hold

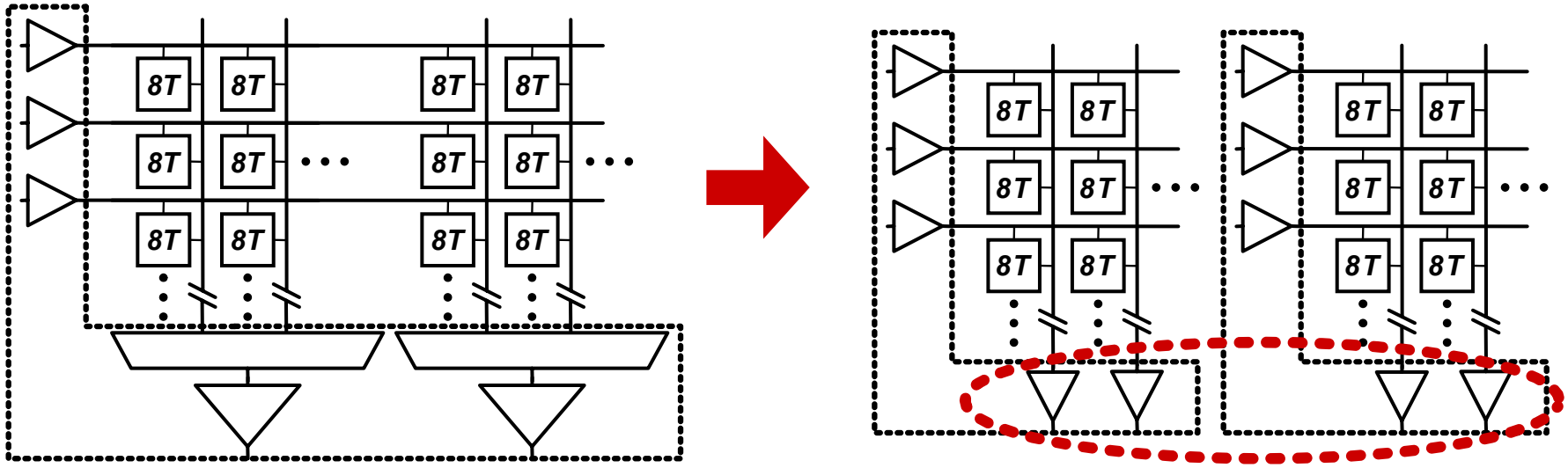
Access devices and supply-driver interact to accurately set VV_{DD}



VV_{DD} settles to low intermediate voltage

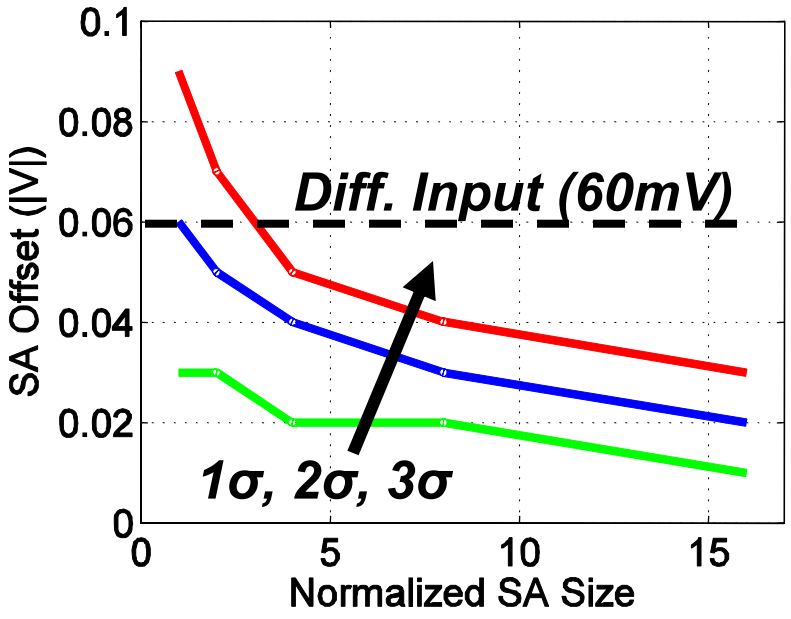
Sense-Amp Area Limitation

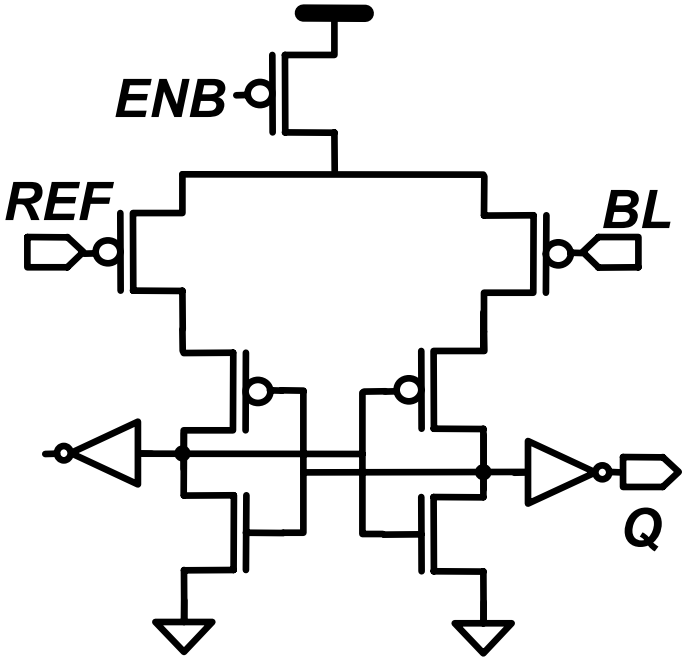
Separate VV_{DD} in non-interleaved layout for minimum voltage and reduced WL load



Sense-amplifier limits yield due to increased number and reduced area

Sense-Amplifier Offset

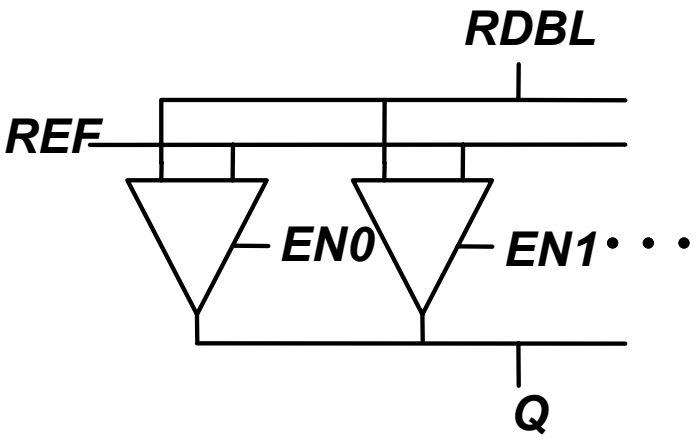




1) <u>Global variation</u> degrades sense-amp accuracy for single-ended read
   - *Pseudo-differential structure eliminates offset*

2) <u>Local variation</u> results in uncorrelated error distribution of sense-amps
   - *Only device up-sizing can reduce offset deviation*

Sense-Amplifier Redundancy

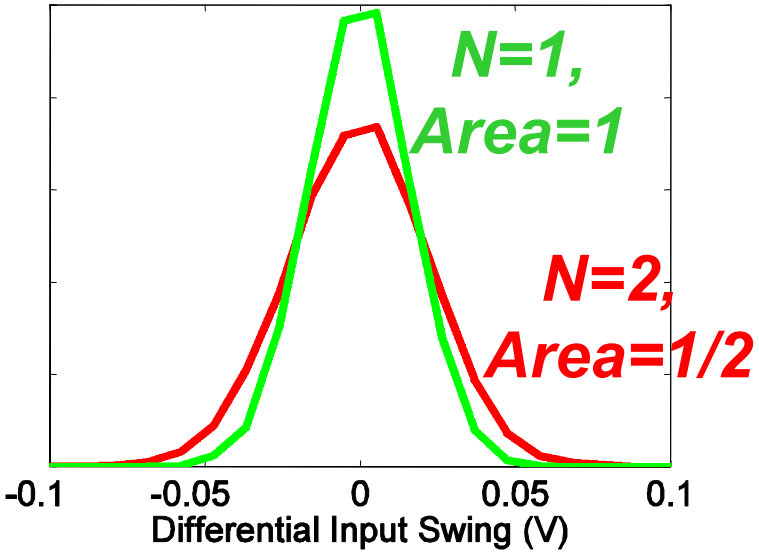


1) Enable only one of N sense-amps for each RDBL

similarly applied to flash A-D [Flynn, TCAS'03]

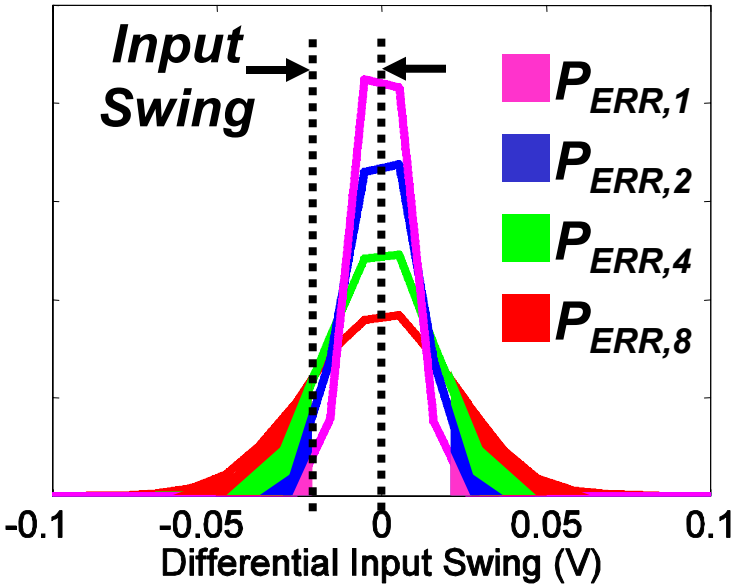
2) Sense-amp offsets are from local variation only (<u>uncorrelated</u>)

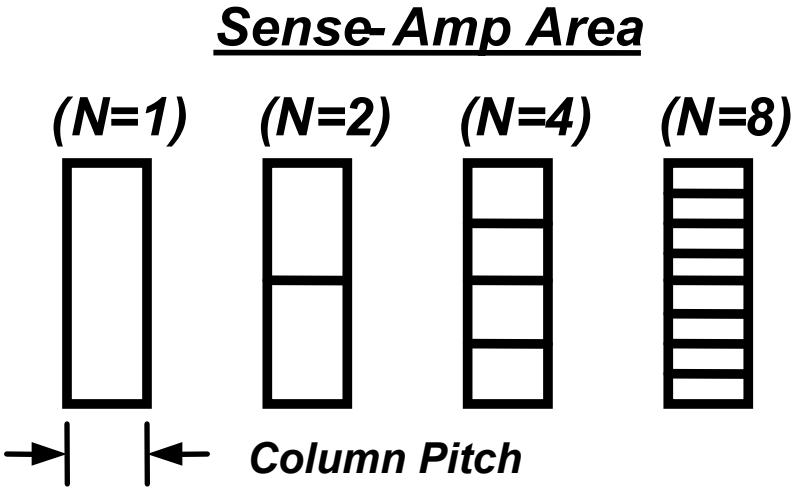
Total area is constrained; each sense-amp must be smaller



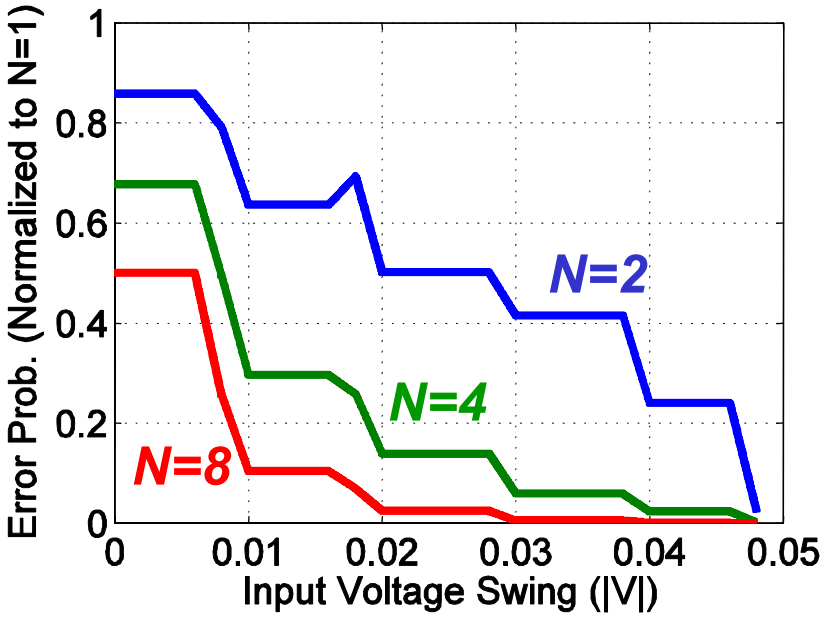
With redundancy, area of each SA must decrease, and <u>its offset goes up.</u>

Sense-Amplifier Redundancy

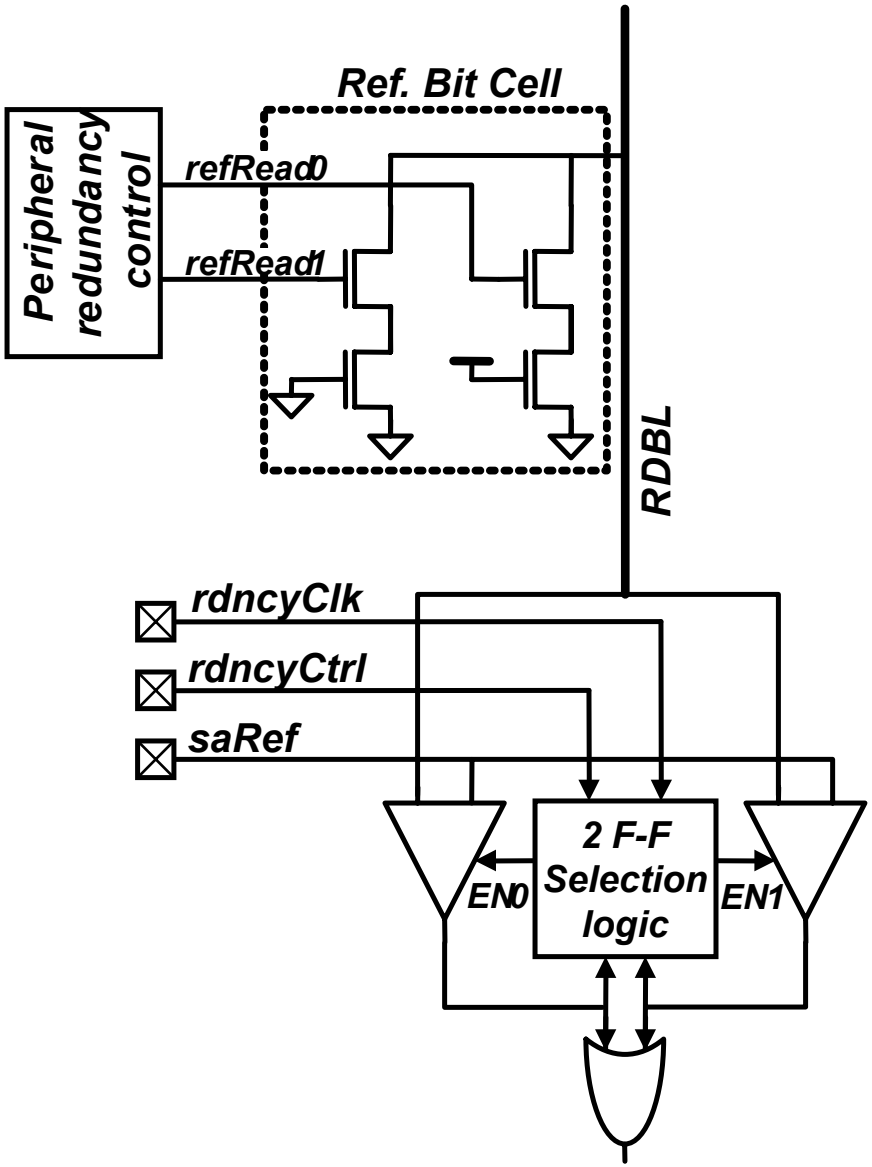




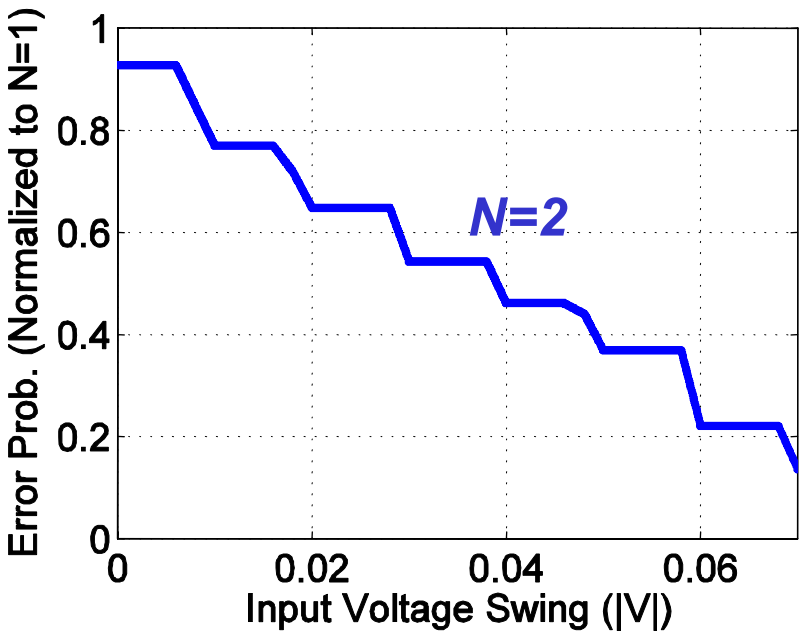
Probability of error depends on joint probability that all sense-amps fail:
$P_{ERR,tot}=(P_{ERR,N})^N$



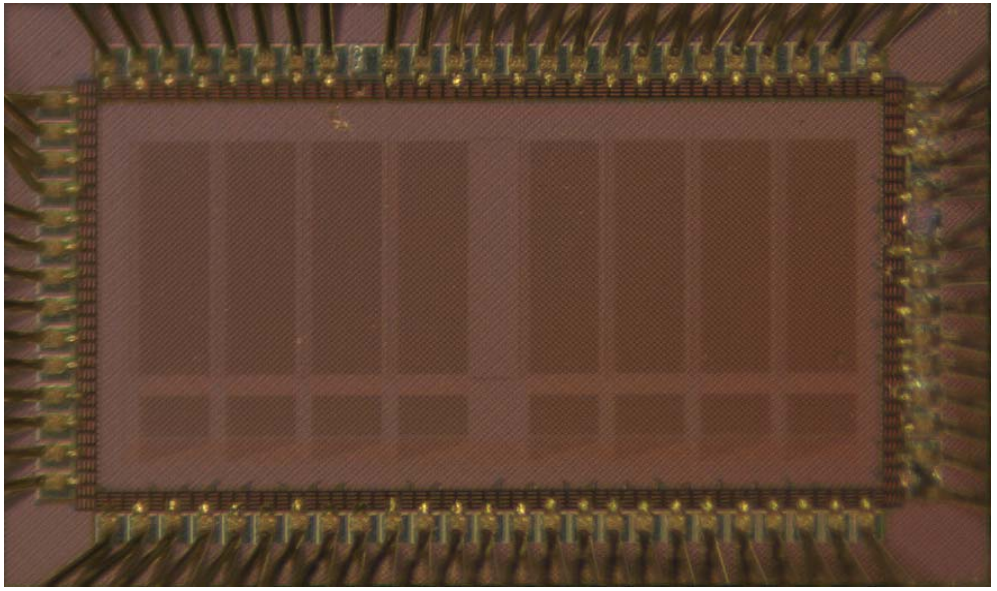
Redundancy Implementation



Start-up loop selects between 2 sense-amps, yielding error improvement of 5x



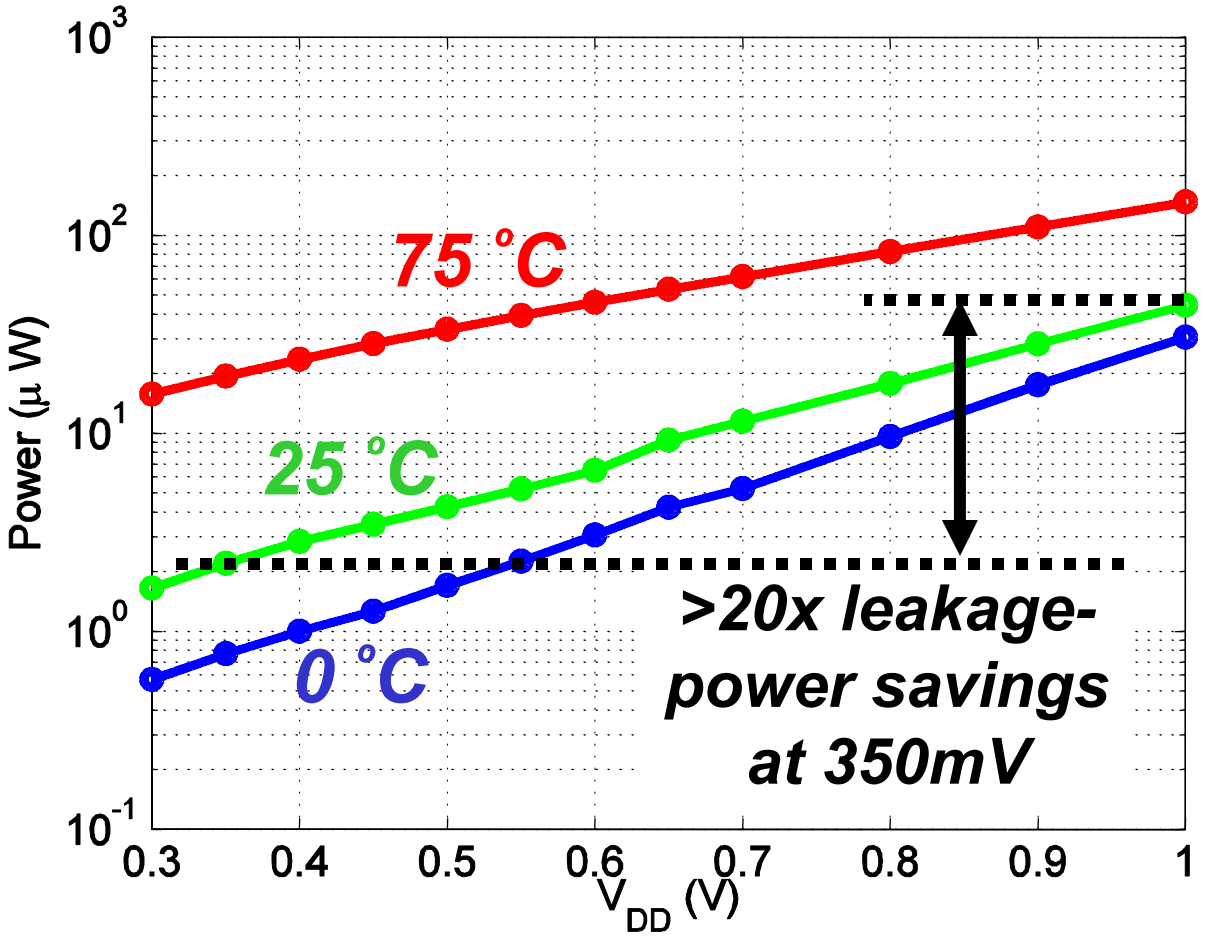
Prototype SRAM



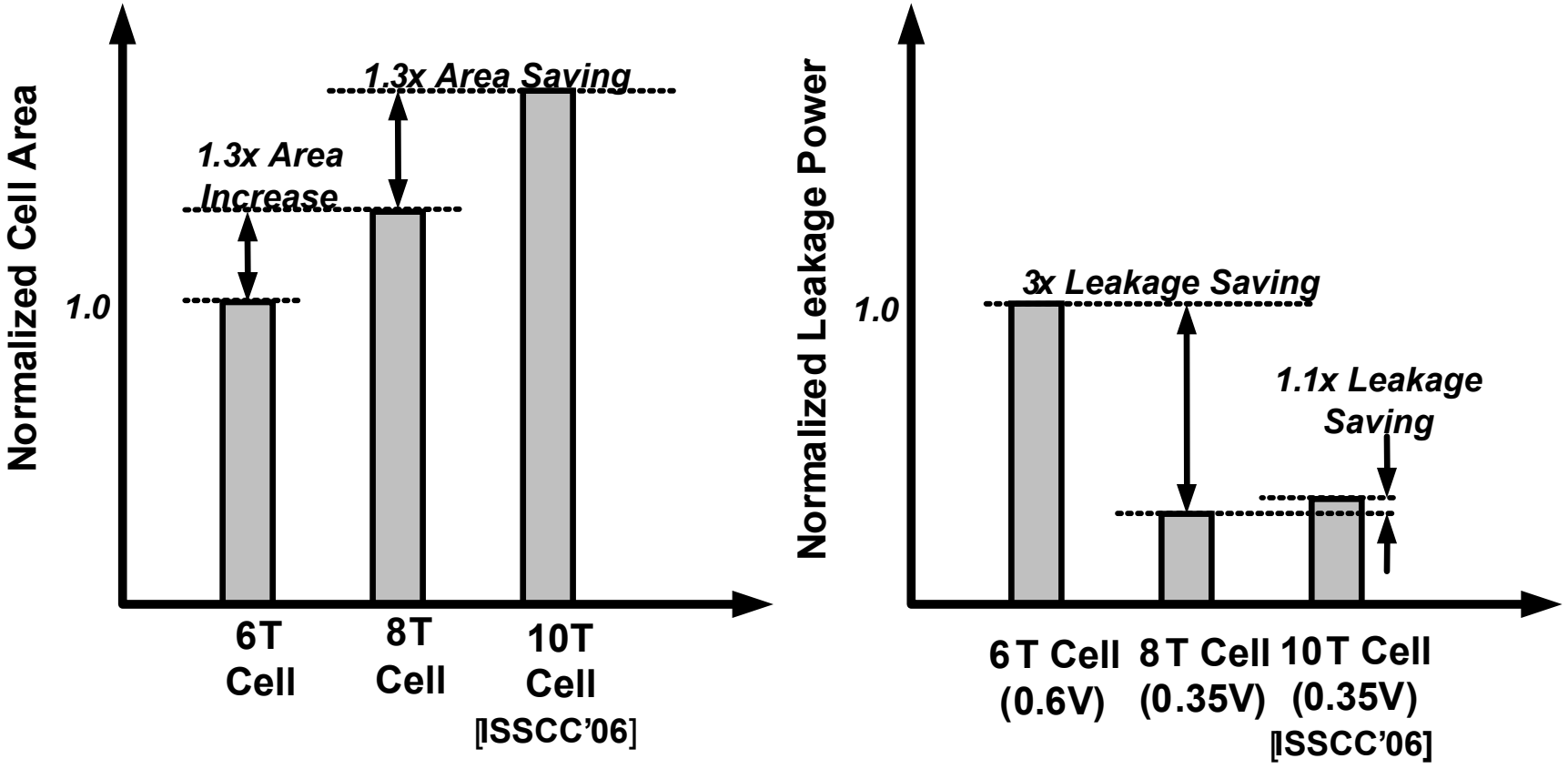
Process	*65nm CMOS*
Architecture	*8 Blocks X 256 Rows X 128 Columns*
Capacity	*256kb*
V_{MIN}	*350mV*

Measured Leakage Power

Data correctly retained at 300mV, P_{LEAK}=1.65µW

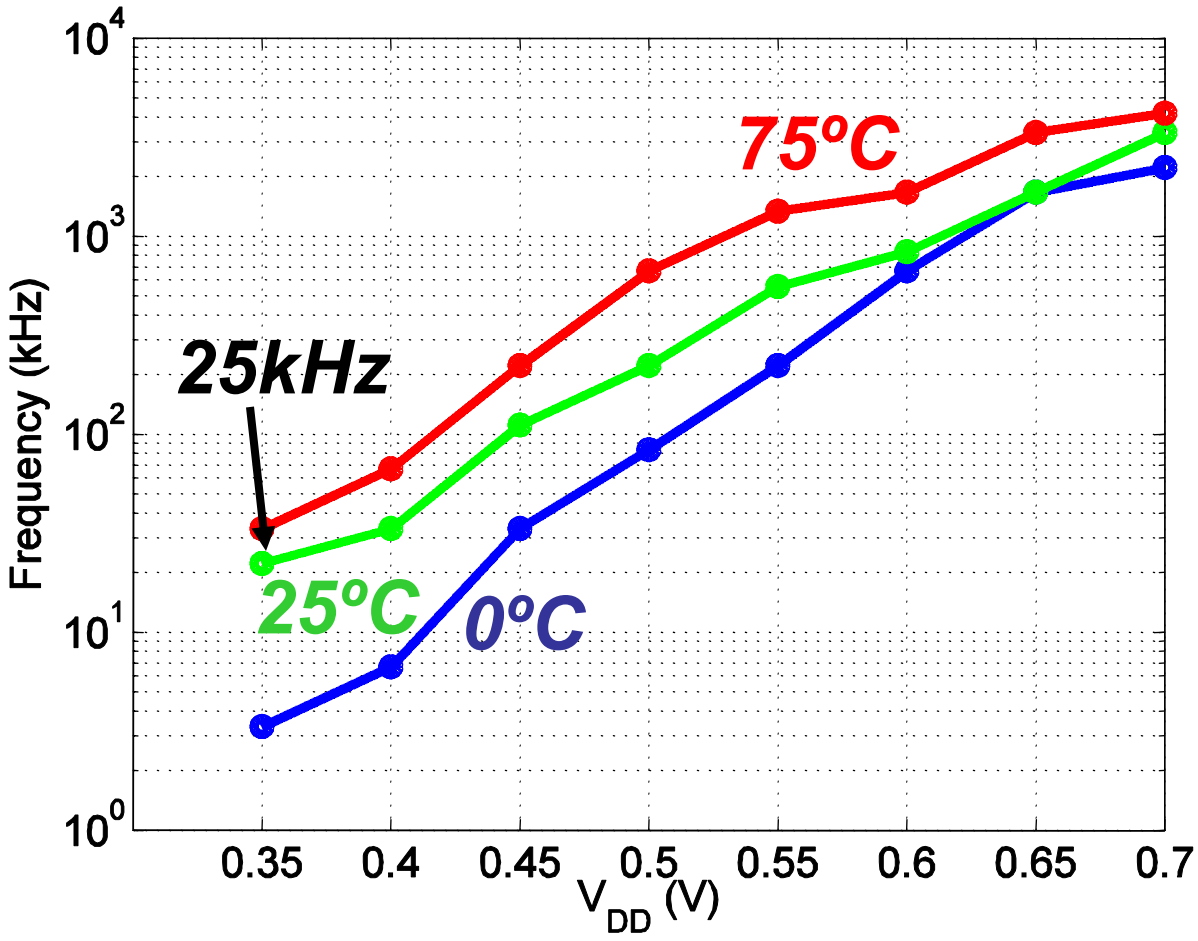


Leakage-Power & Area Comparison



3x leakage power savings and 30% area overhead compared with 6T cell

Active Performance



Conclusions

- **6T cell is ratioed; sub-V_t variation causes read/write failures and long access times**
- **8T cell and peripheral assists eliminate BL leakage, read/write limitations**
- **Sense-amplifier redundancy improves sensing yield by 5x**

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