

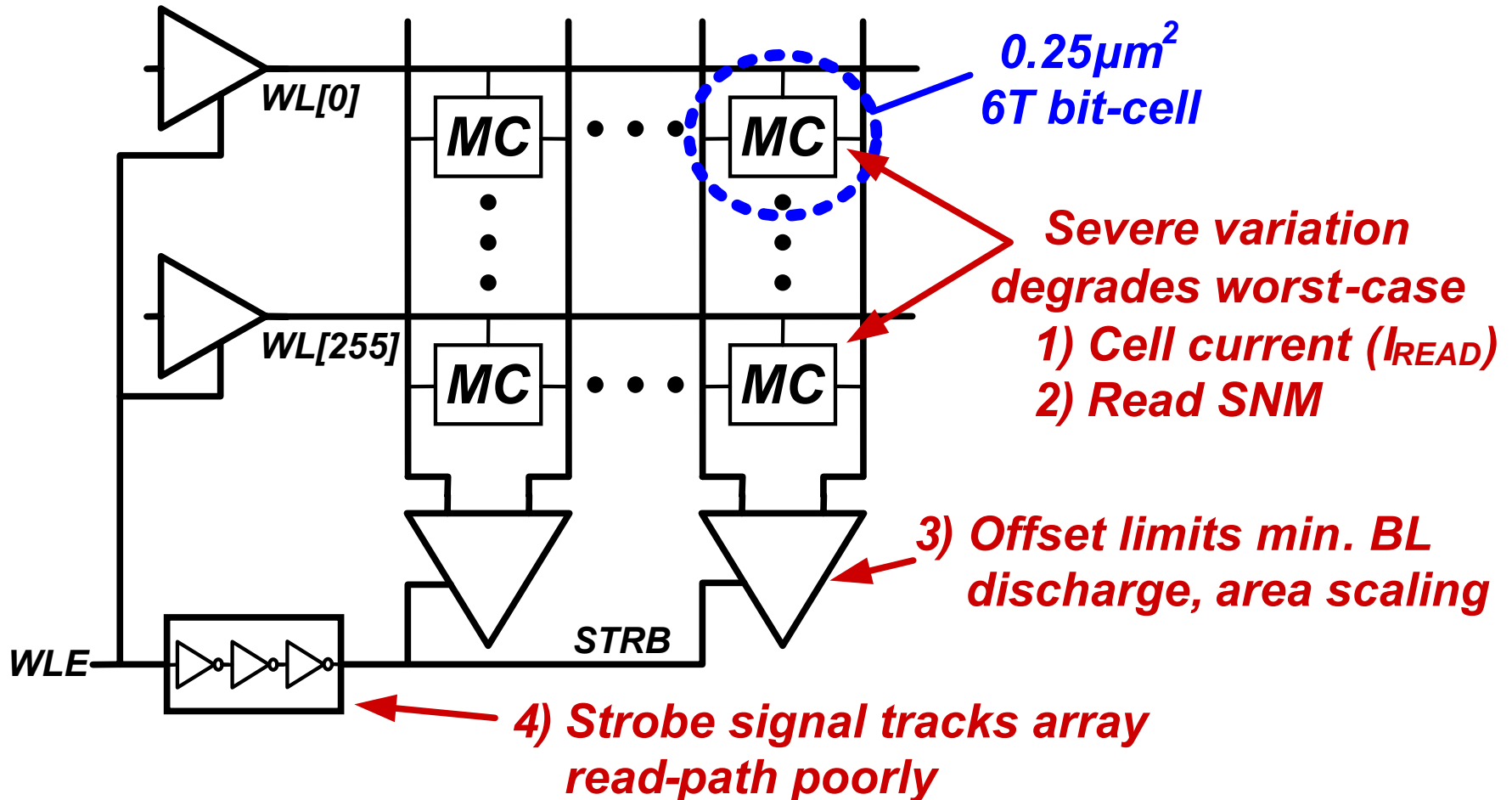
21.3

A High-Density 45nm SRAM Using Small-Signal Non- Strobed Regenerative Sensing

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High-Density SRAM Limiting Factors

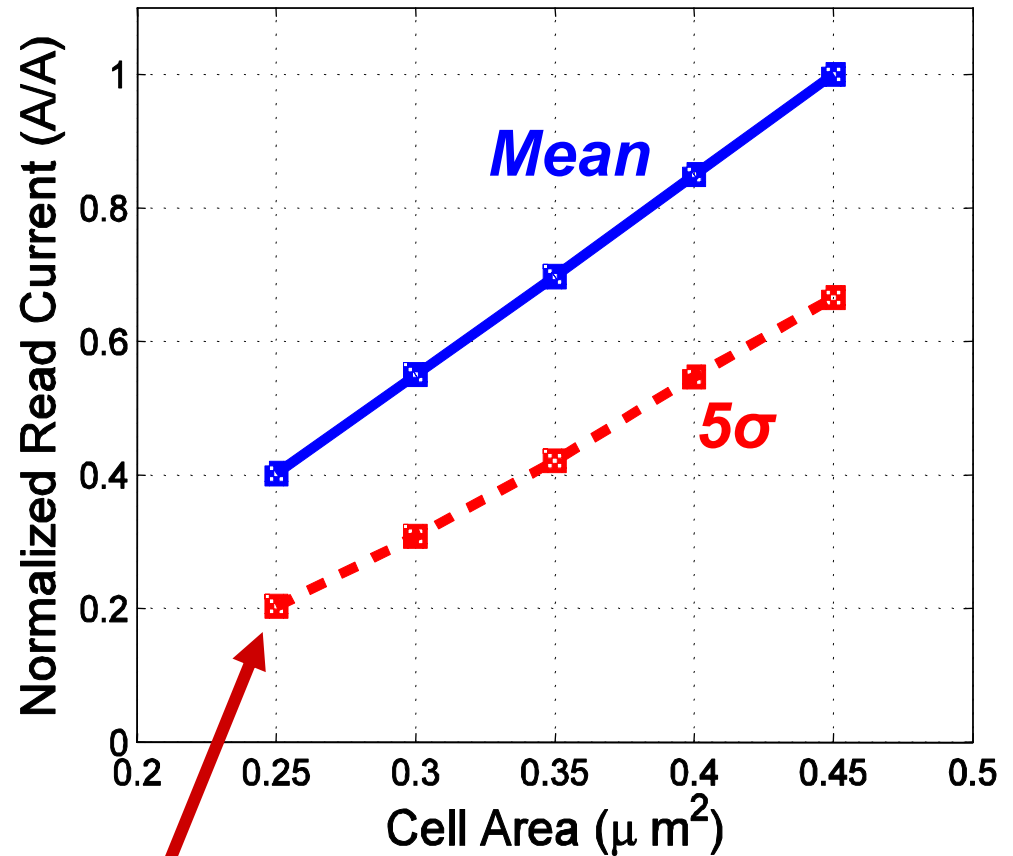
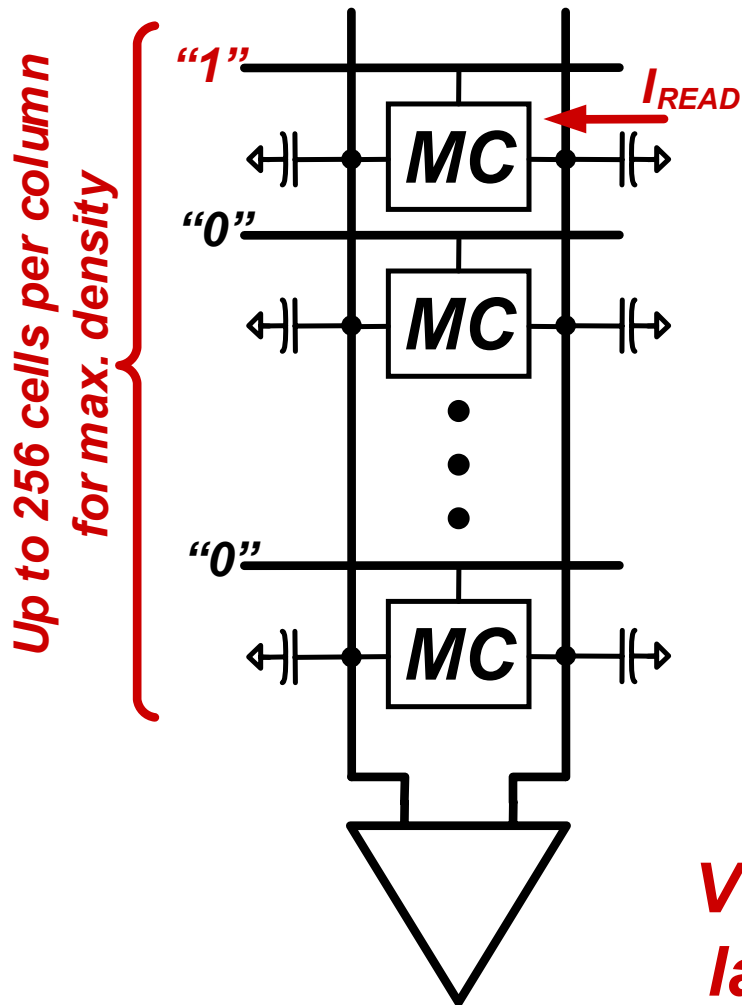


Counter severe variability through sense-amp

Outline

- **High Density 45nm SRAM challenges**
- **Single-ended read architectures**
- **Non-strobed regenerative sense-amp (NSR-SA) operation**
- **Prototype measurements**
- **Conclusions**

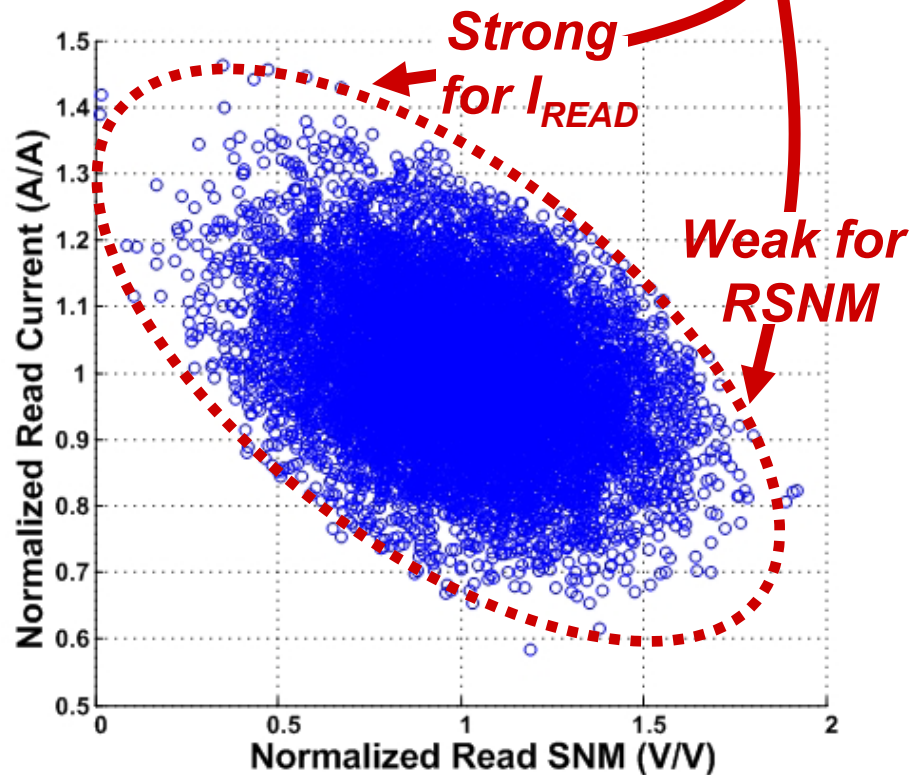
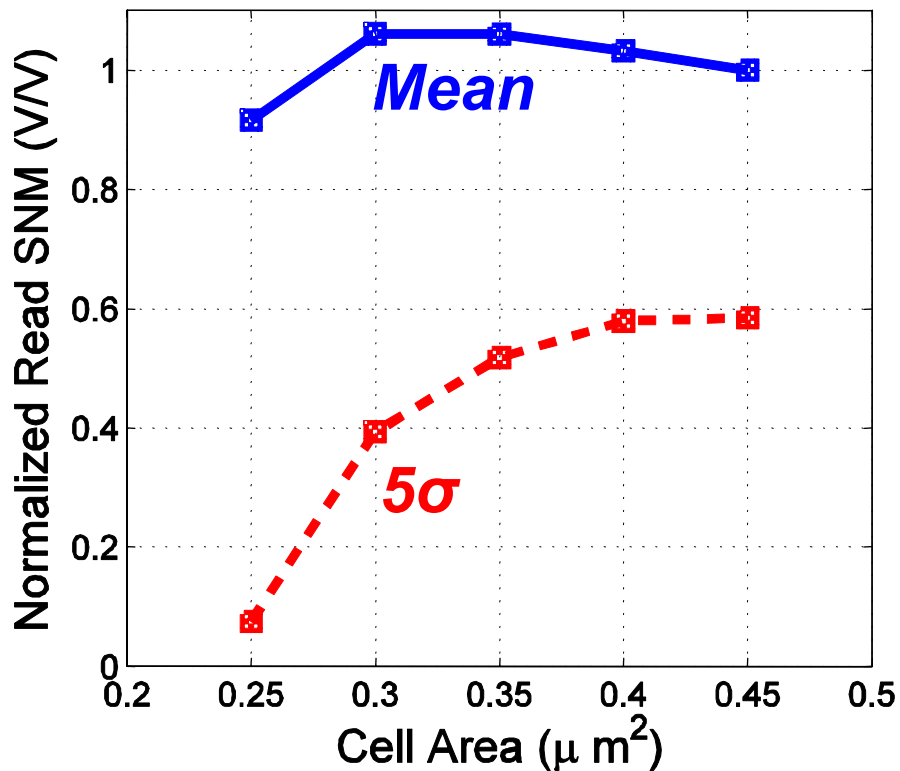
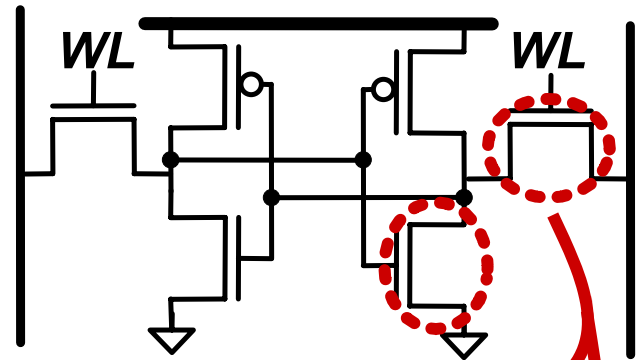
I_{READ} Degradation



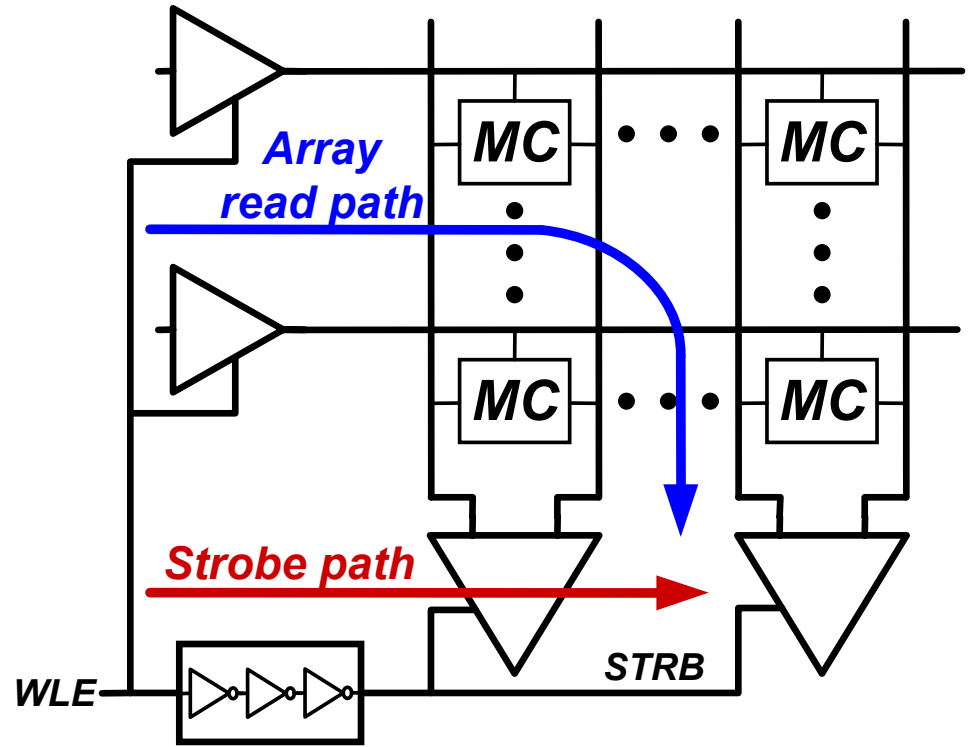
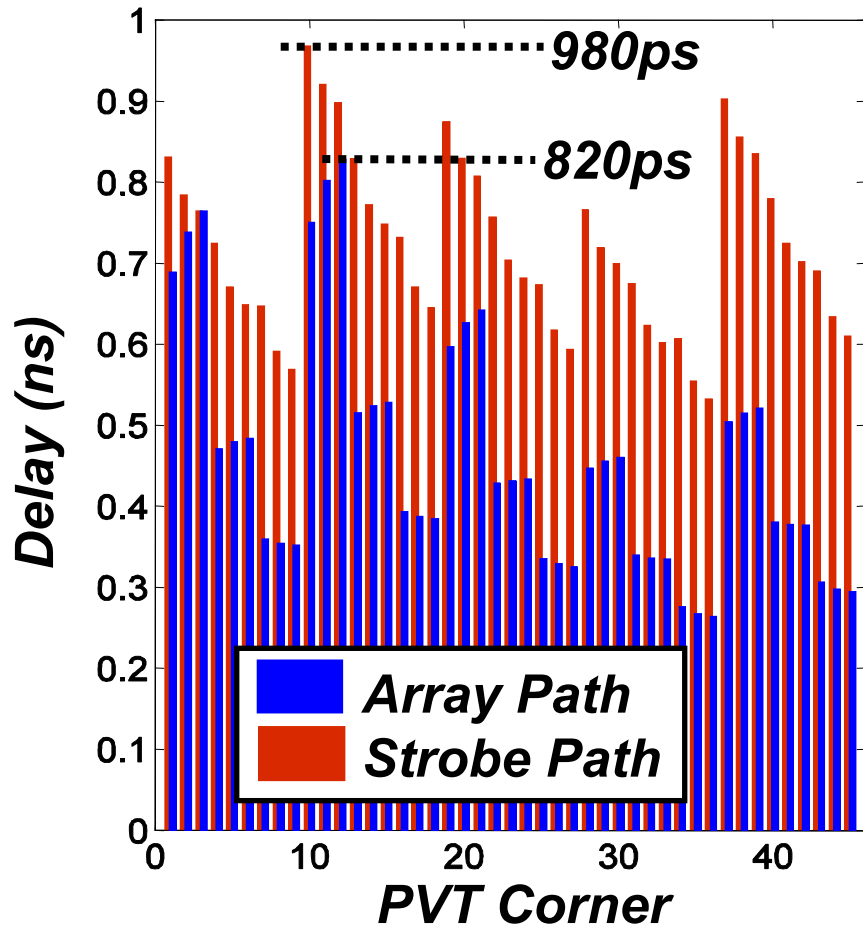
**Variation causes
larger fractional
degradation**

Read SNM- I_{READ} Degradation

Read SNM of $0.25\mu\text{m}^2$ cell is too low and must be improved at the cost of I_{READ}



SA Strobe Timing Uncertainty



Worst-case array delay: 820ps

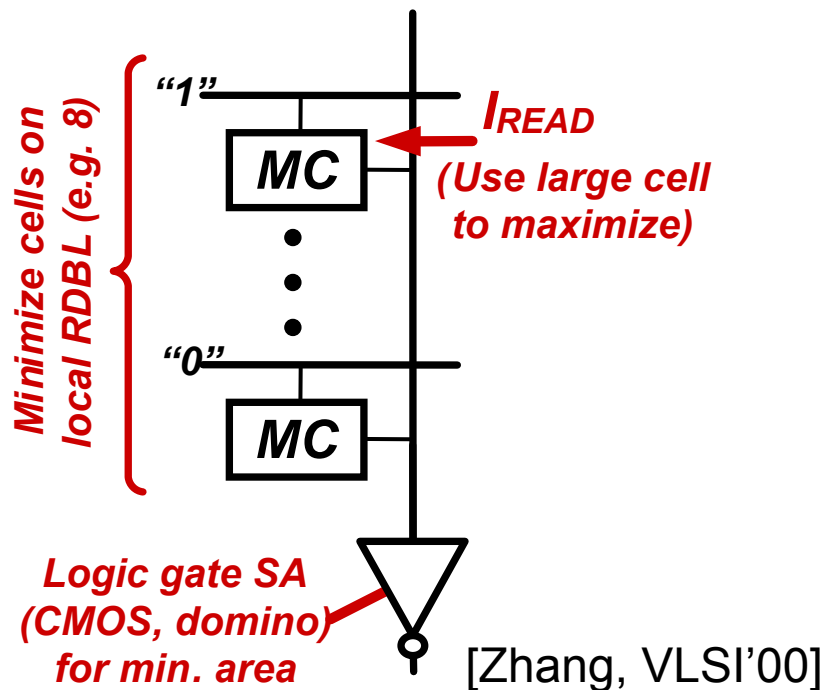
Worst-case strobe delay: 980ps

Array and strobe paths track poorly; required timing margin increases worst-case access time by ~20%

Single-Ended Sensing - Techniques

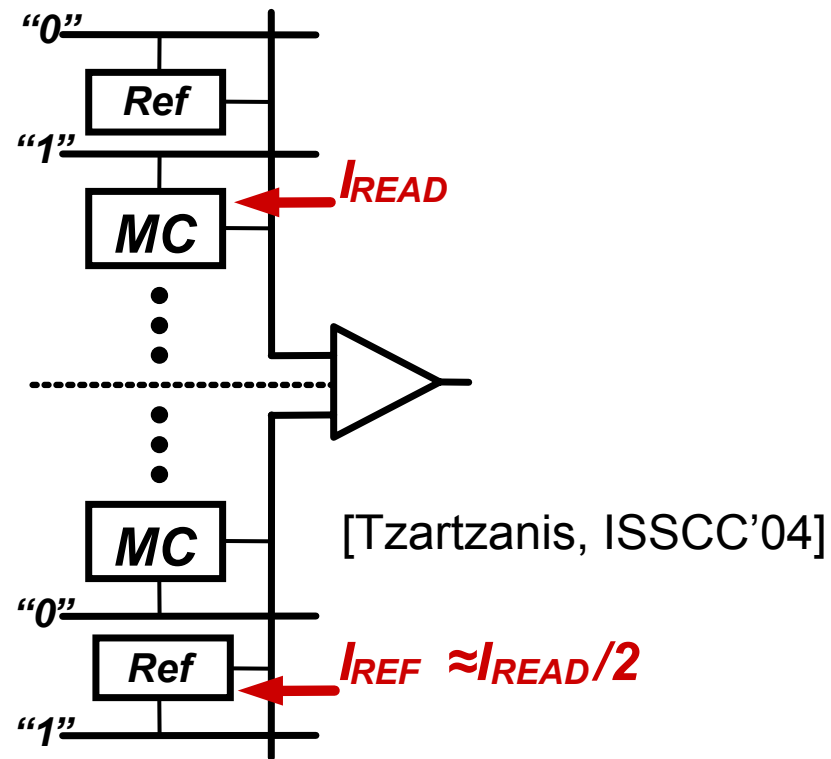
*Asymmetric cells can have wider operating margins
e.g. 8T [Morita, Chang, Joshi, etc. VLSI'07]*

Full-Swing Sensing



- Need to minimize C_{BL}/I_{READ} limits density

Pseudo-Differential Sensing

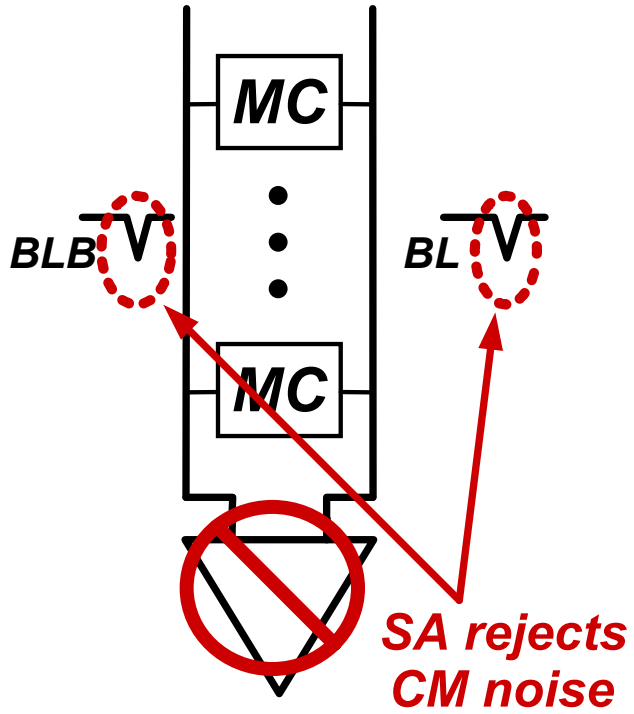


- Need to generate reference that tracks $I_{READ,MIN}$

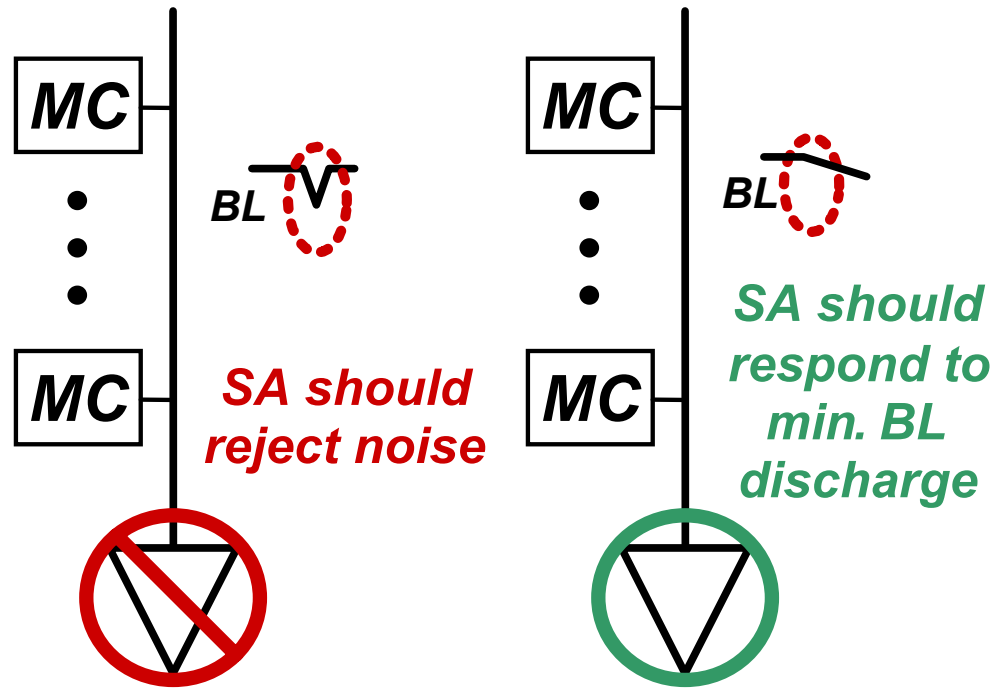
Single-Ended Sensing – Trade-off

Single-ended SA has no common-mode rejection...

Differential SA

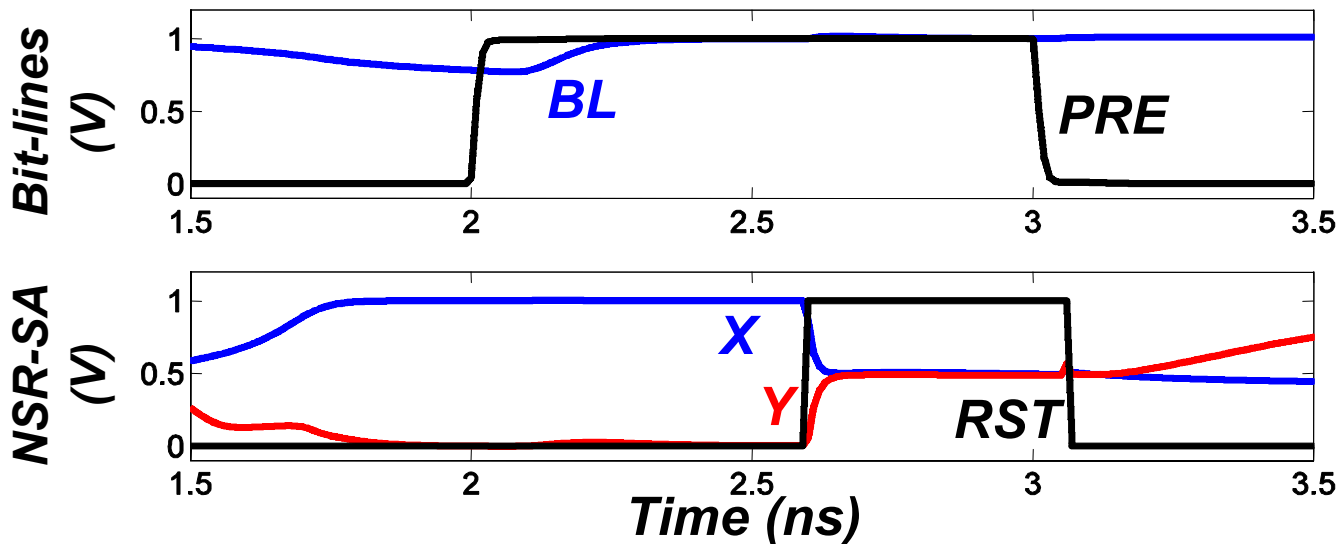
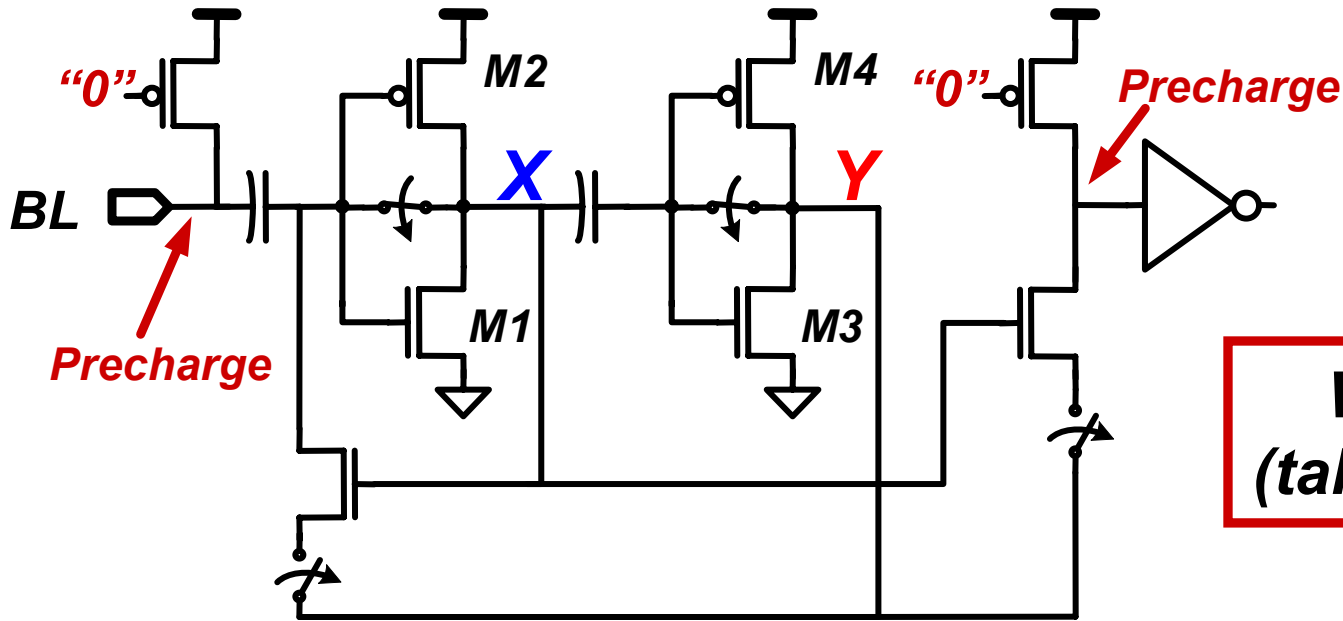


Single-Ended SA

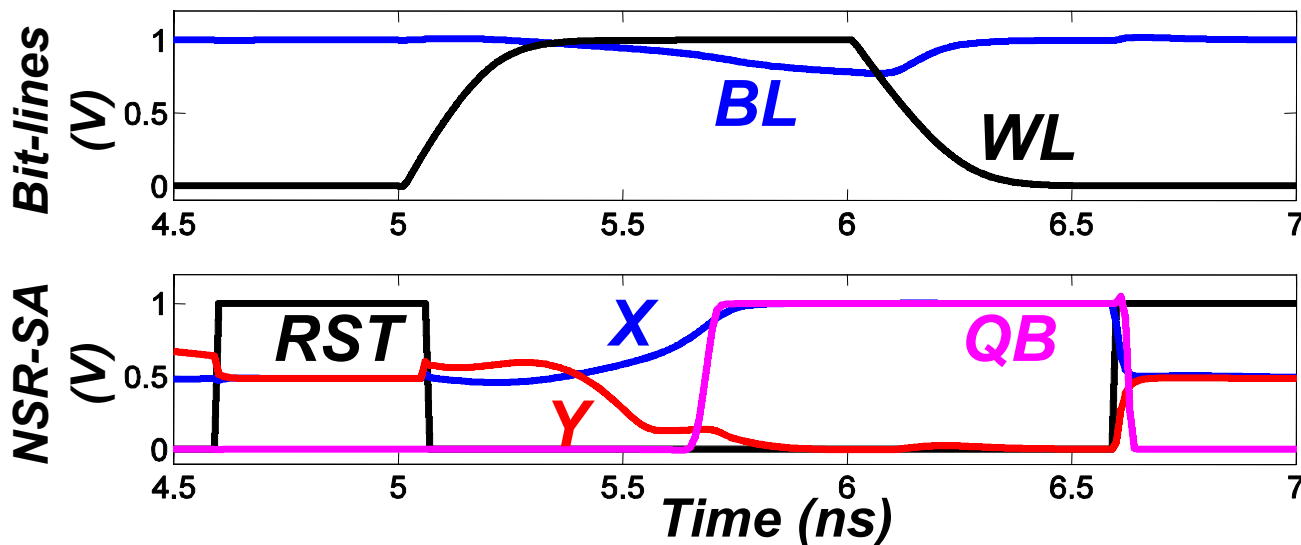
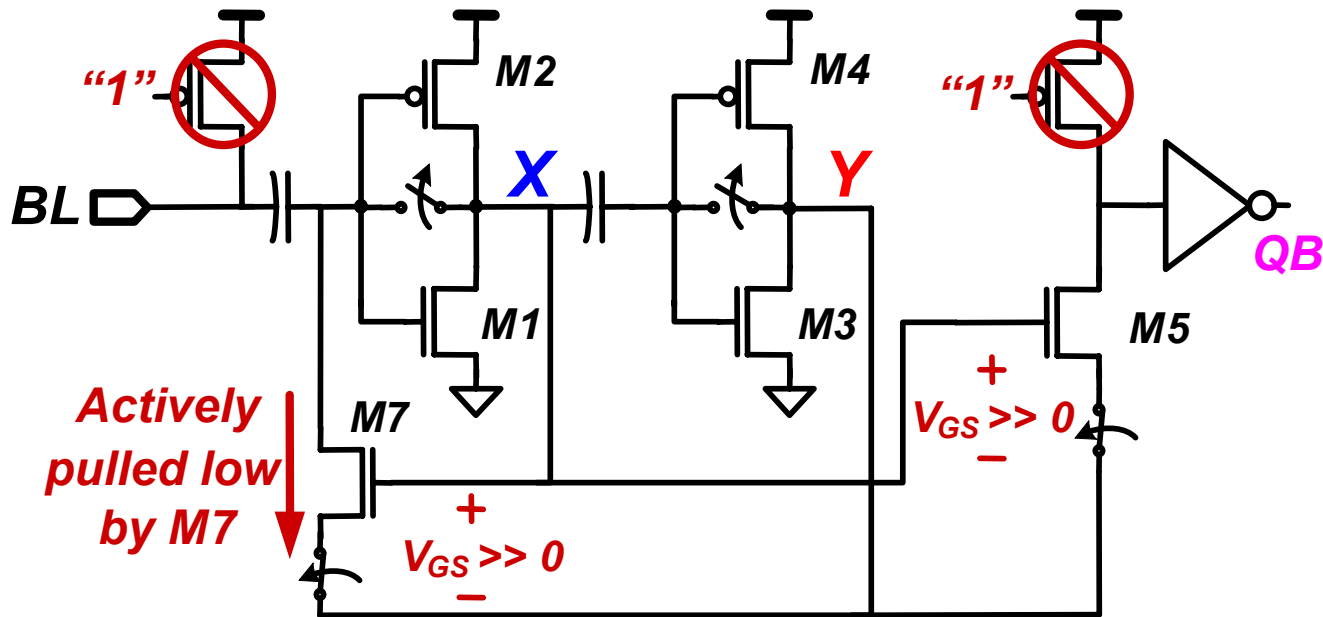


Single-ended sensing introduces trade-off between sensitivity and noise-rejection

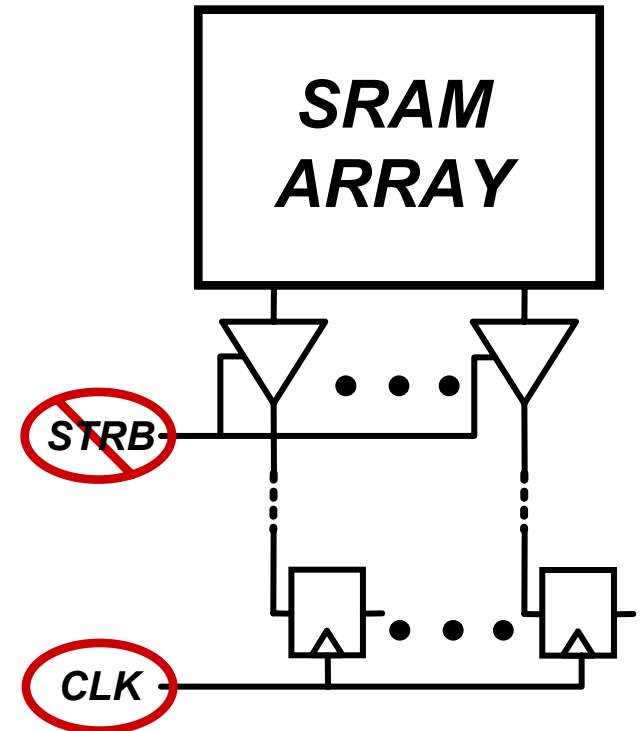
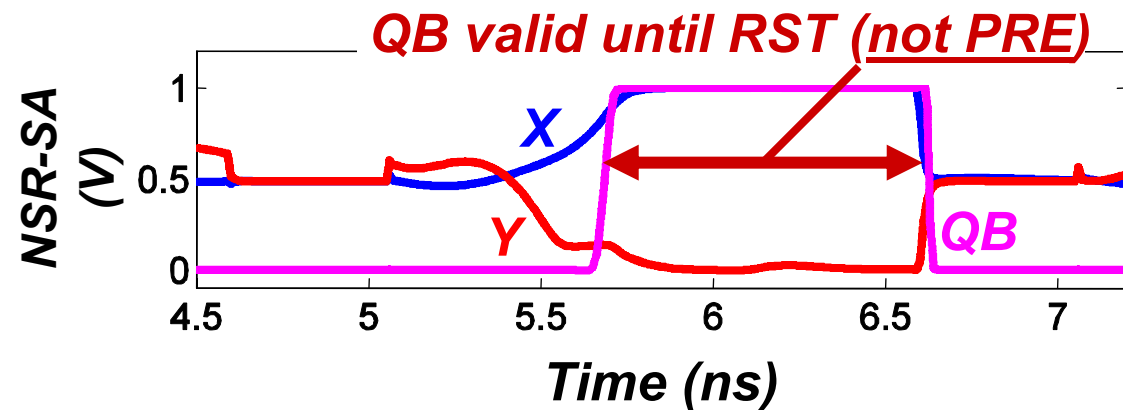
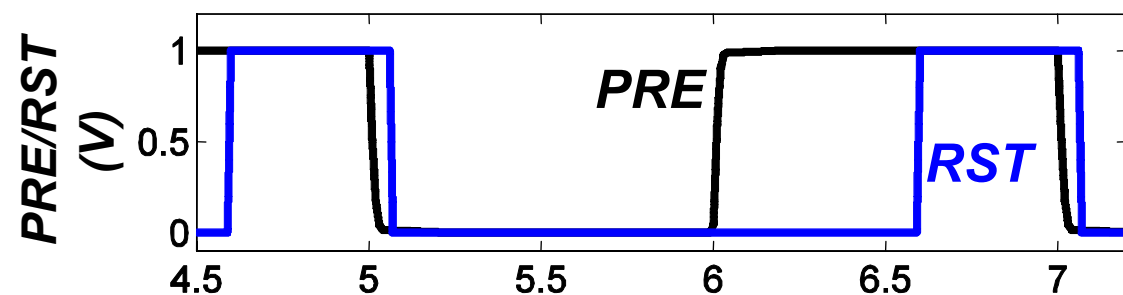
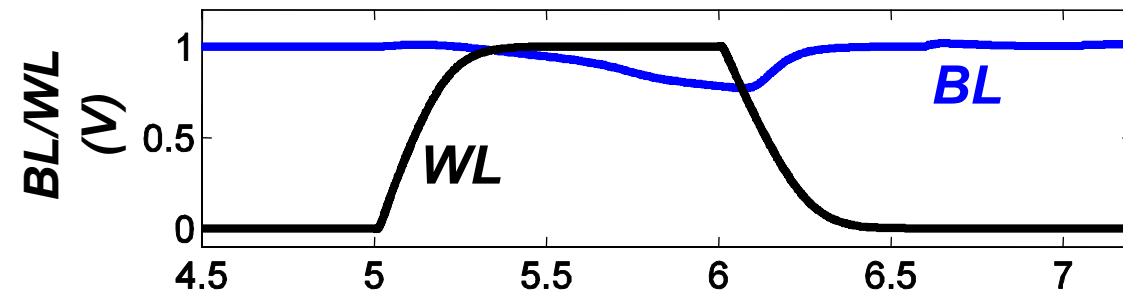
NSR-SA Operation: Reset Phase



NSR-SA Operation: Sense "0"

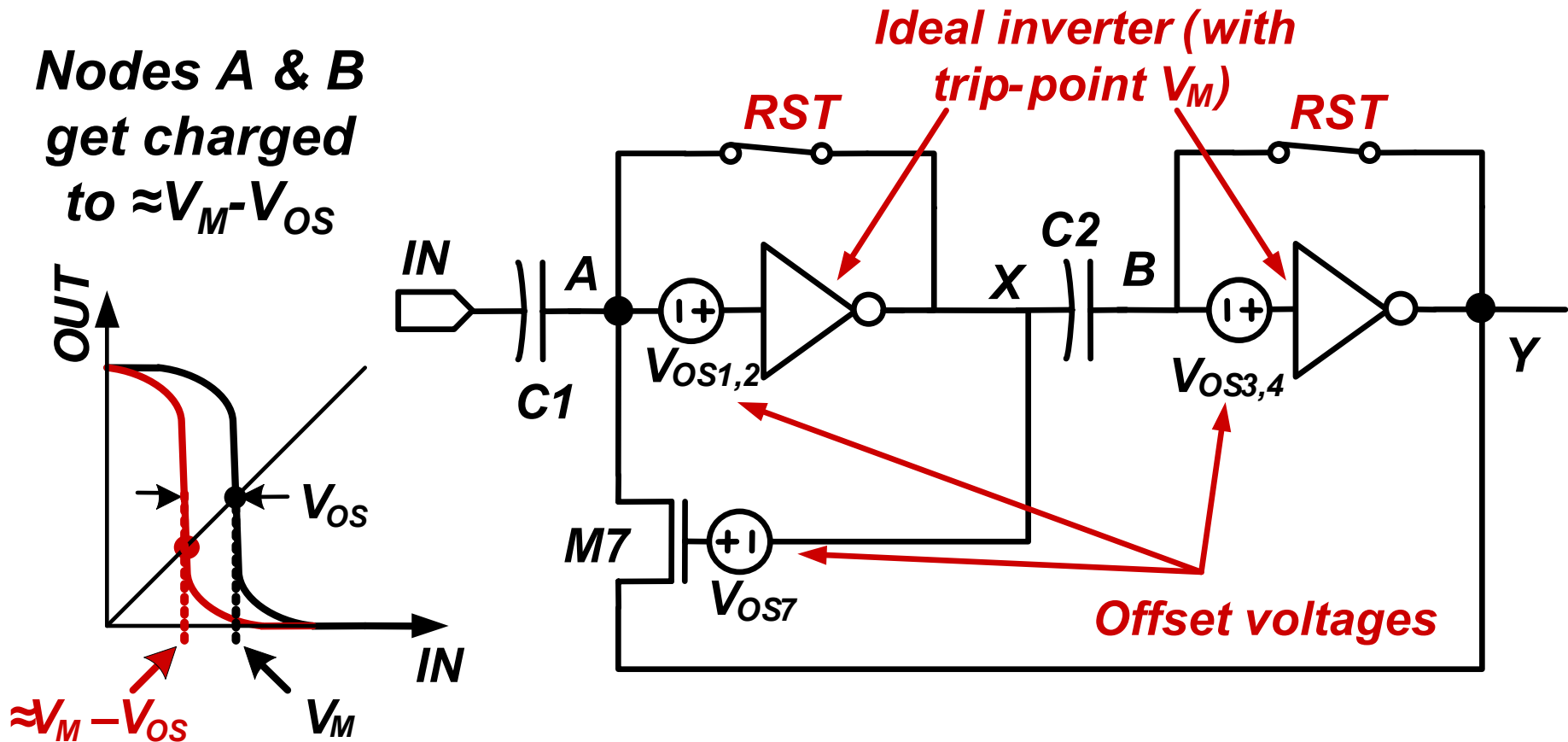


NSR-SA Output Clocking



NSR-SA latches data, so output can be clocked after PRE begins

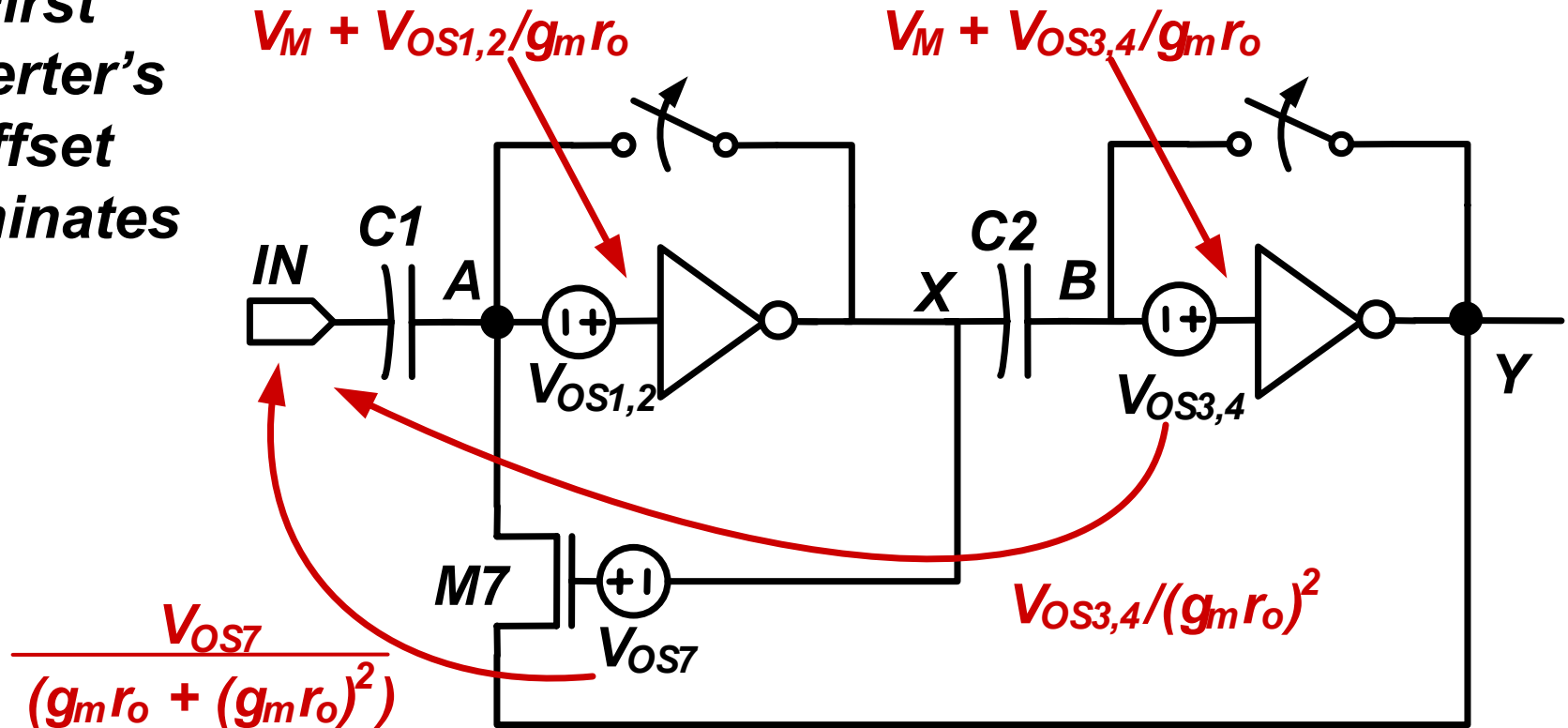
NSR-SA Offset Compensation - I



**Negative of offset voltages are stored on C1/C2;
VTCs from IN-X and X-Y are offset free**

NSR-SA Offset Compensation - II

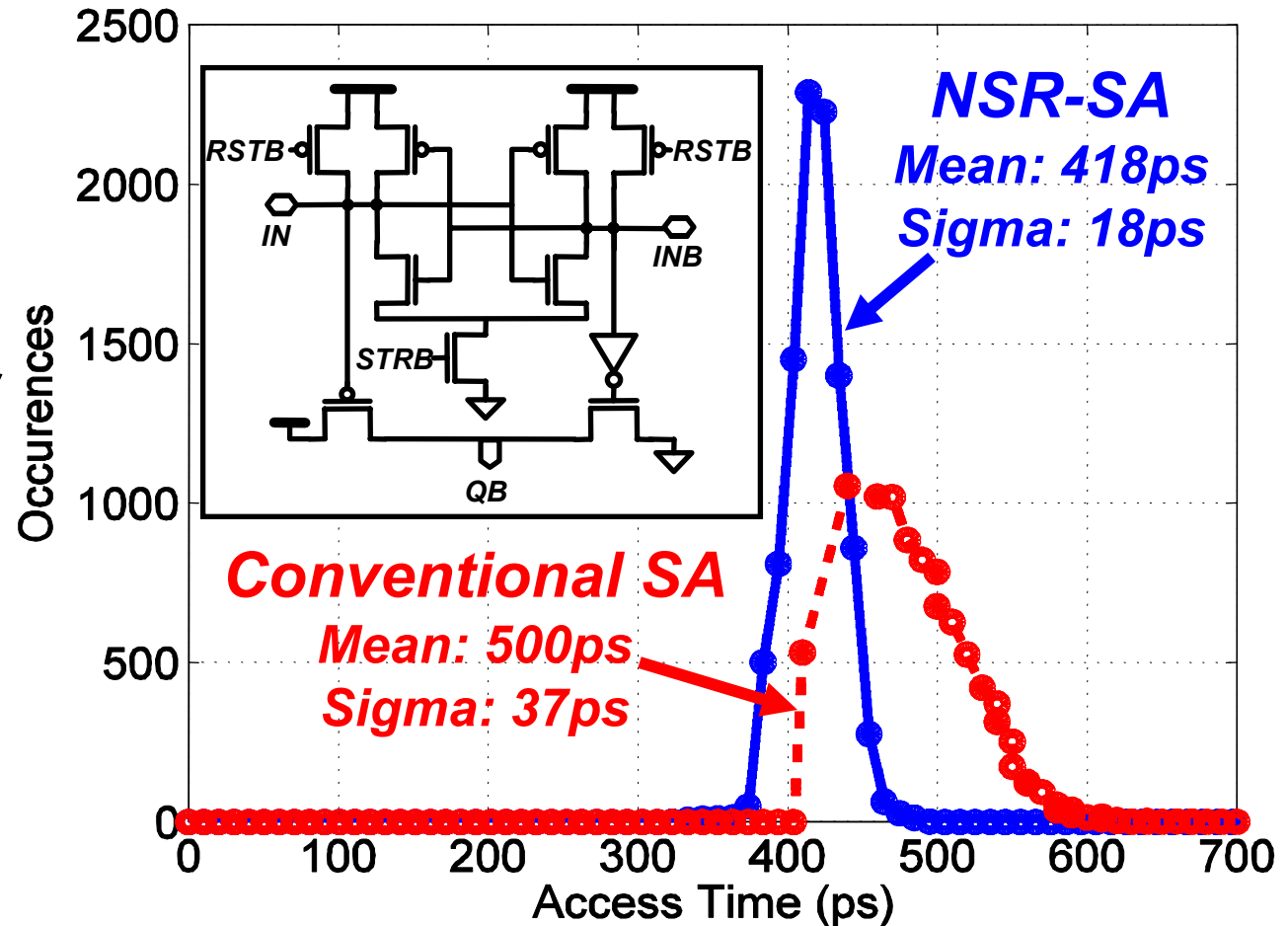
First inverter's offset dominates



All offsets are diminished by at least $g_m r_o$ (i.e. inverter gain) when input referred

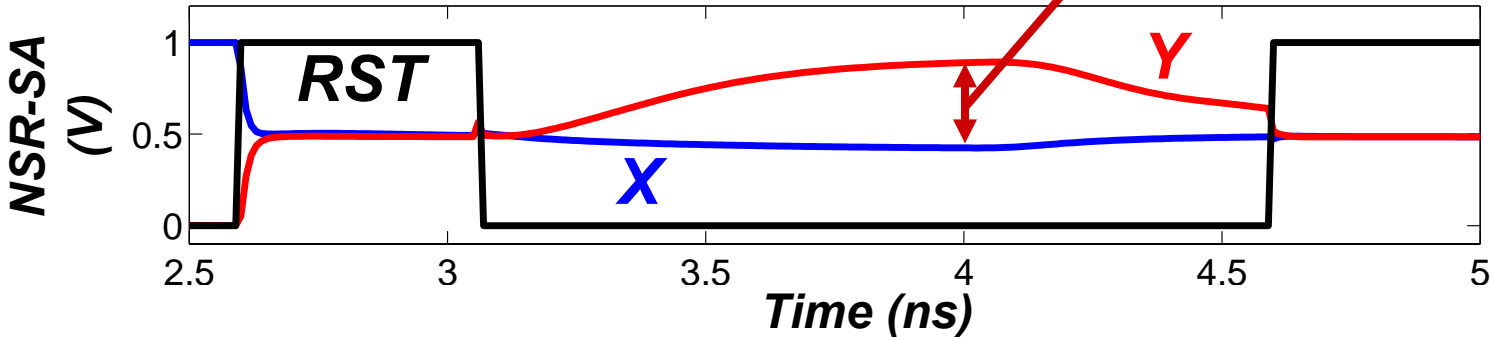
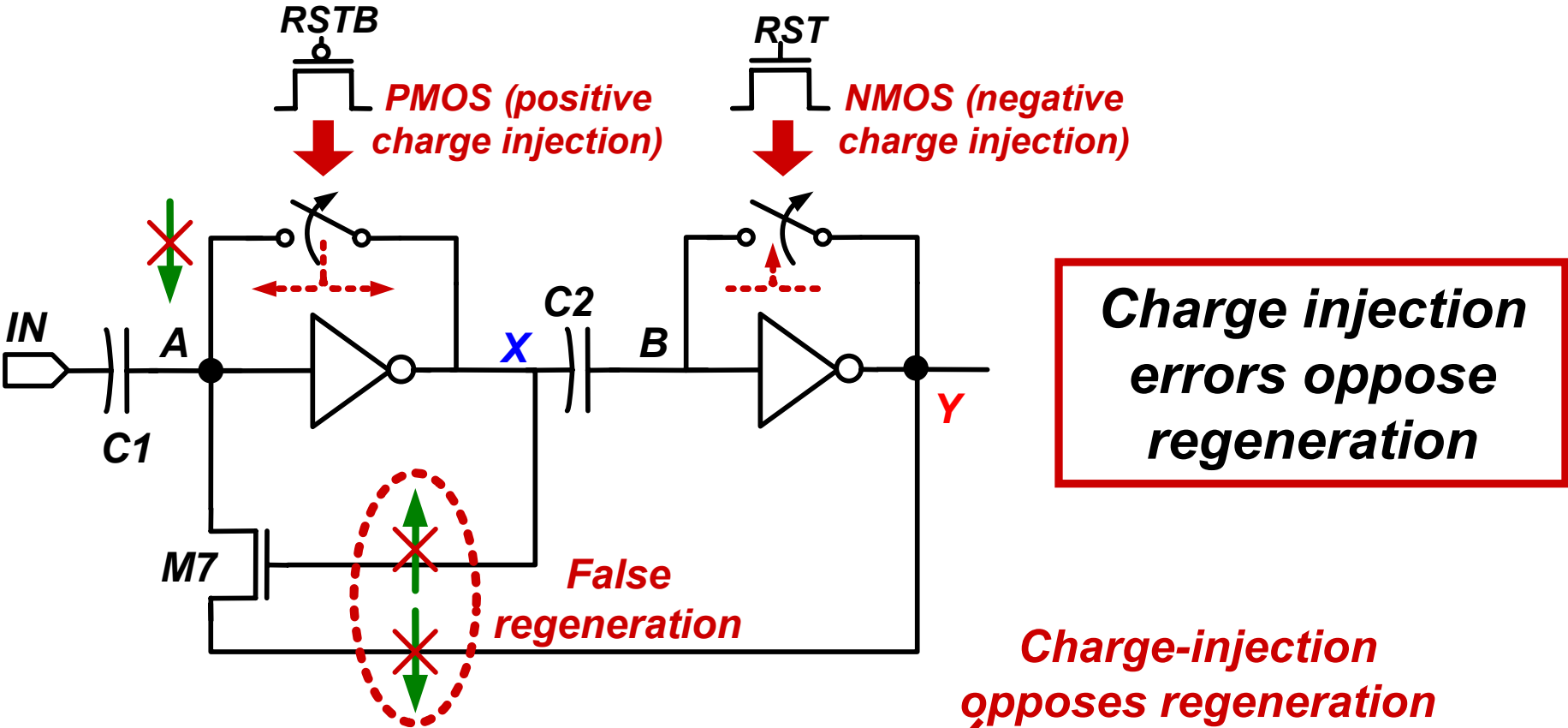
SA Access Time Distribution

- *Mean bit-cell*
- *Nominal process corner*
- *Variation applied to all SA devices*

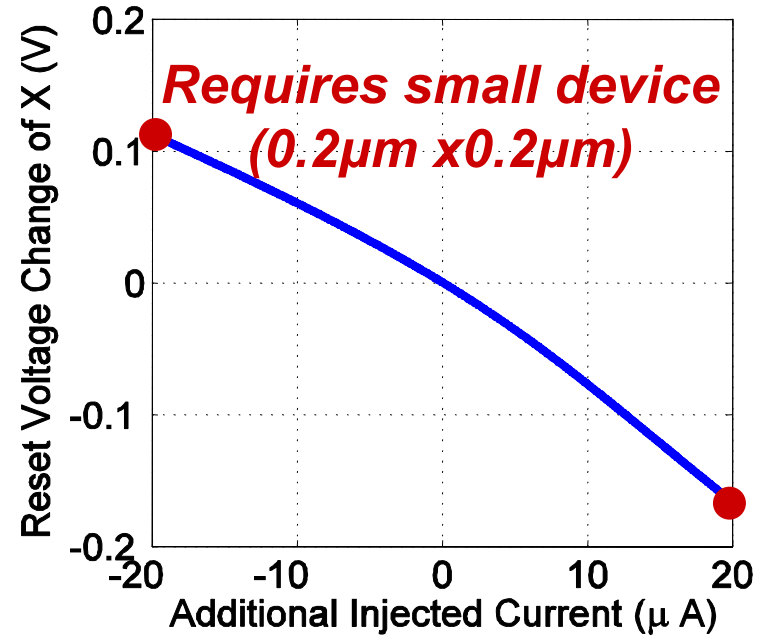
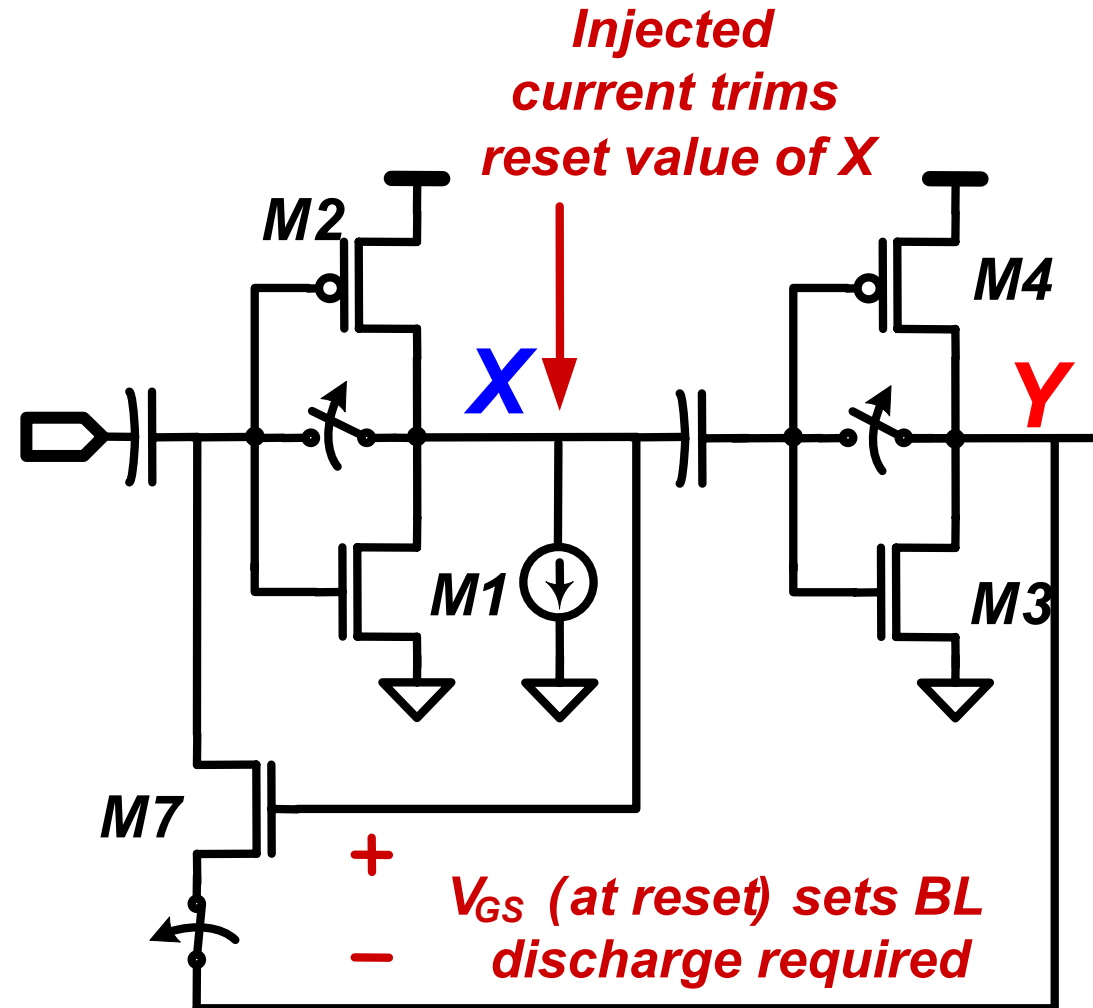


NSR-SA offset compensation yields superior sigma

Charge Injection Error Immunity



Regeneration Trip Point

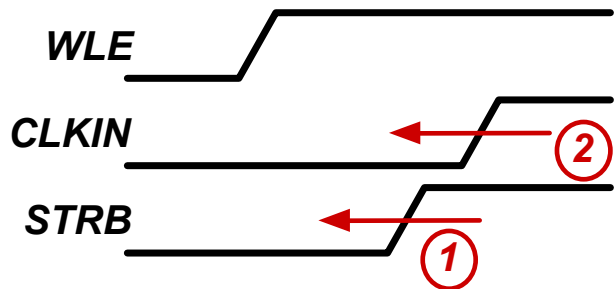


Adjust reset value of X & Y to set desired BL discharge required for regeneration

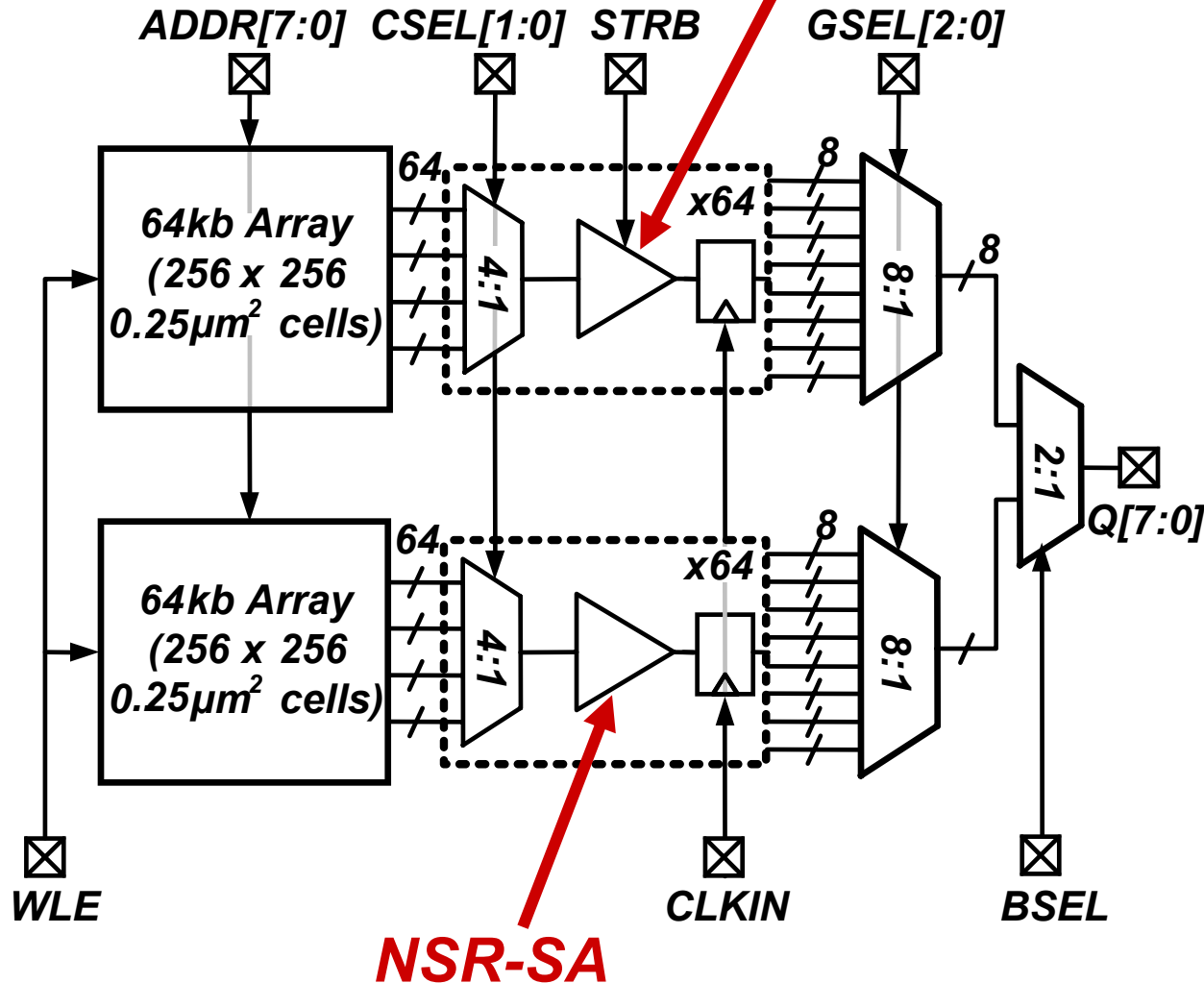
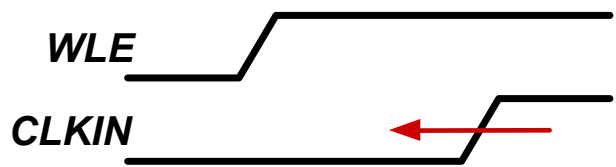
Test-Chip Architecture

Conventional SA

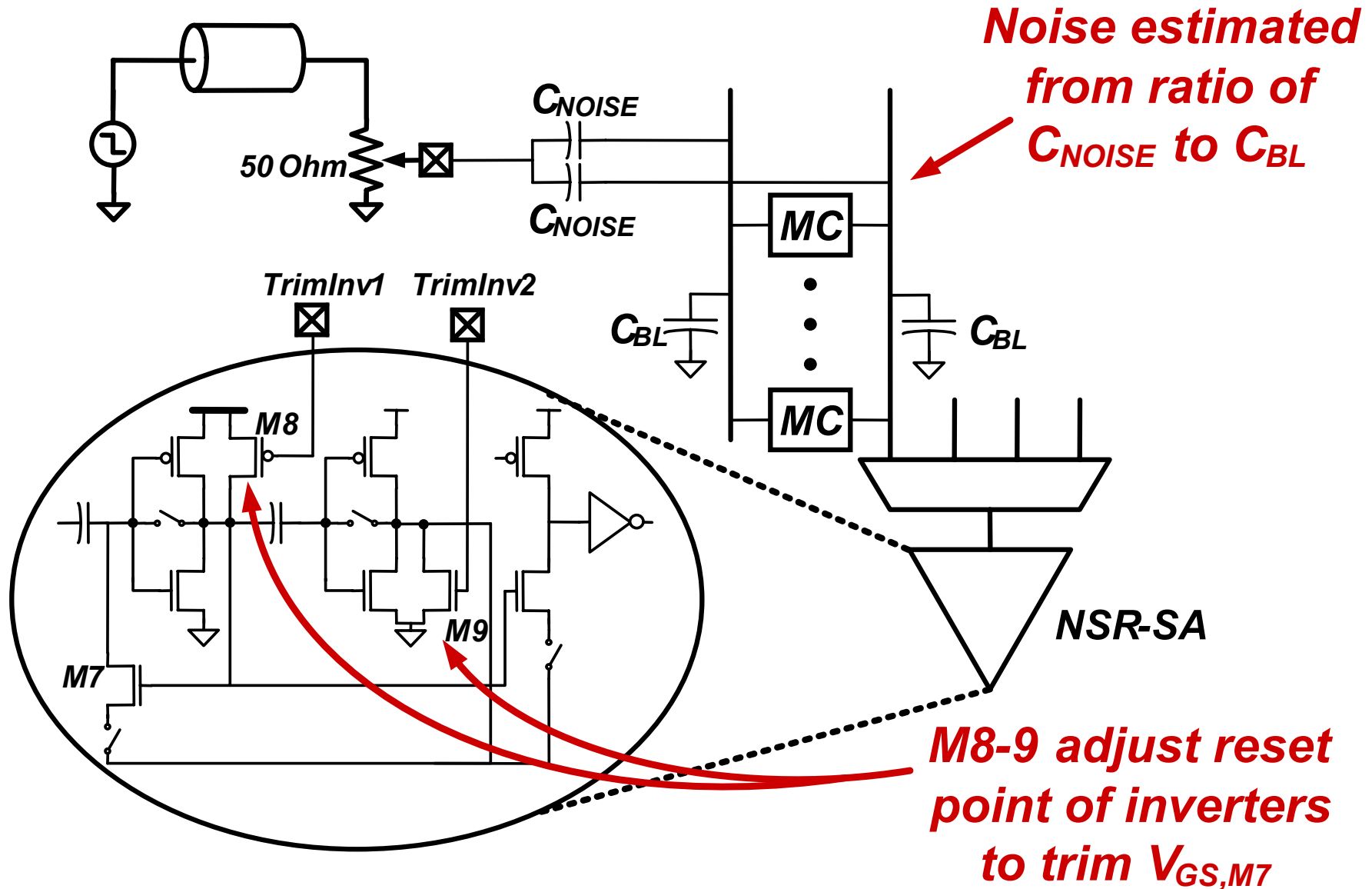
Conventional SA



NSR-SA

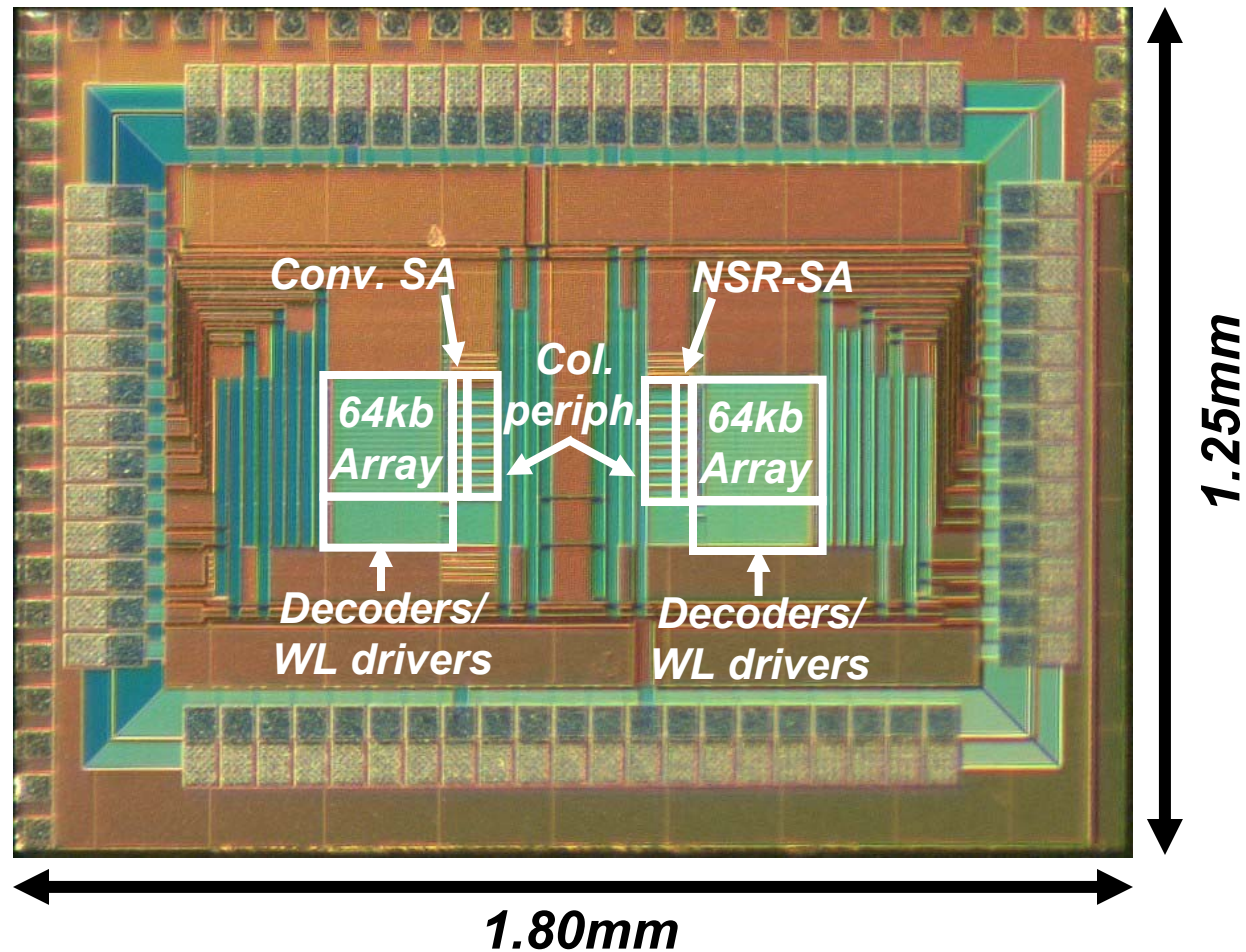


Noise Injection Circuit

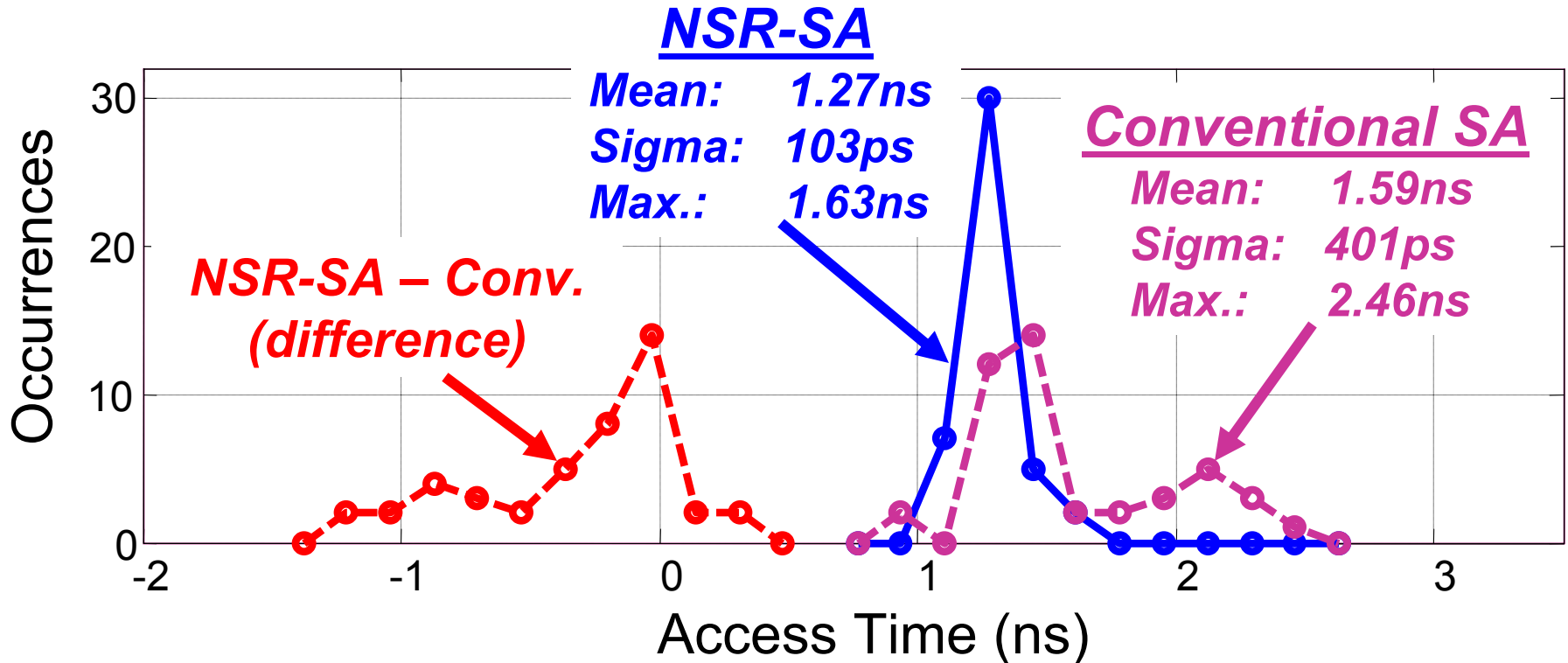


Prototype SRAM

- **45nm low-power CMOS**
- **2, 256x256 arrays (compare SA performance)**
- **0.25 μm^2 bit-cells**

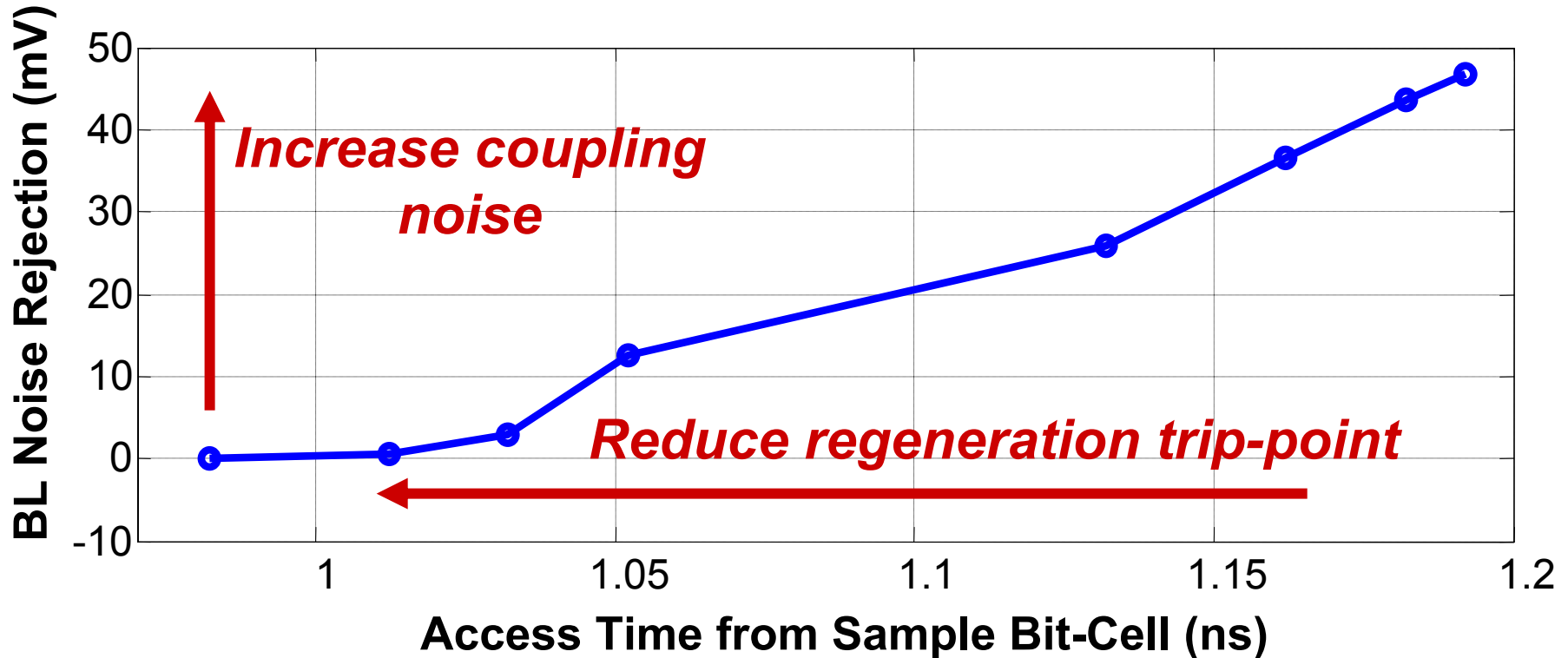


Measured Access Times



**Measured 53 chips;
NSR-SA gives 34% speed-up in worst-case
access-time**

Noise Rejection



50mV of bit-line noise margin can be reduced for up to 20% performance increase

Performance Summary

	Conventional SA	NSR-SA
Technology	<i>45nm low-power CMOS</i>	
Cell size	<i>0.25μm^2</i>	
Array configuration	<i>256 x 256</i>	
Capacity	<i>64kb</i>	
Area	<i>12μm^2</i>	<i>19μm^2 *</i>
Power in reset	<i>-</i>	<i>23μW</i>
% of array power (at 100MHz)	<i>2%</i>	<i>7%</i>
Mean access-time	<i>1.59ns</i>	<i>1.27ns</i>
Max. access-time	<i>2.46ns</i>	<i>1.67ns</i>
Access-time sigma	<i>401ps</i>	<i>103ps</i>

**NSR-SA includes testability features*

Conclusions

- **Bit-cell design for high-density SRAM is highly constrained, leading to low I_{READ}**
- **NSR-SA improves sensing stability with offset compensation and overcomes strobe uncertainty, enhancing speed up to 34%**
- **Single-ended small-signal sensing improves trade-offs for asymmetric bit-cells**

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