Ultra-Low-Power UWB for Sensor Network Applications

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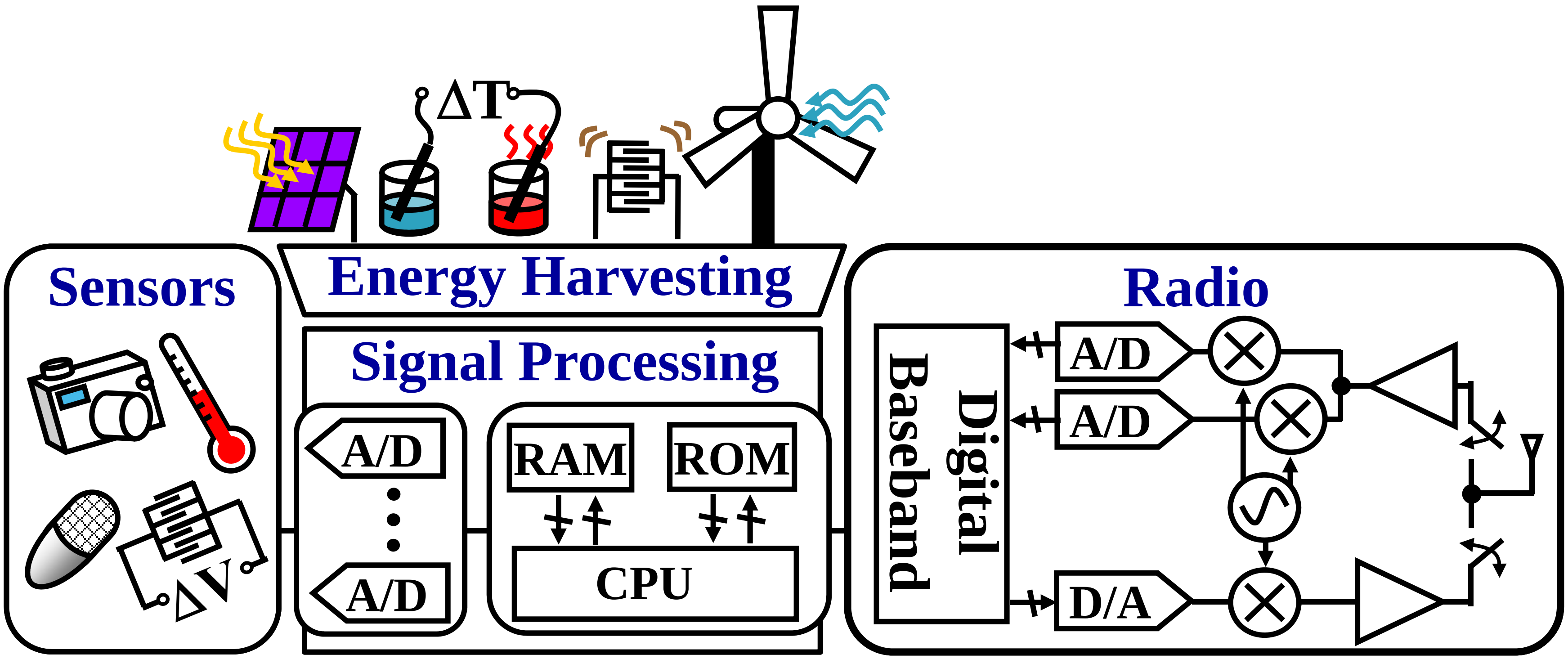
Outline

- Motivation
- Energy Detecting UWB Receiver
- All-Digital UWB Transmitter
- Maximizing Communication Distance
- Conclusions

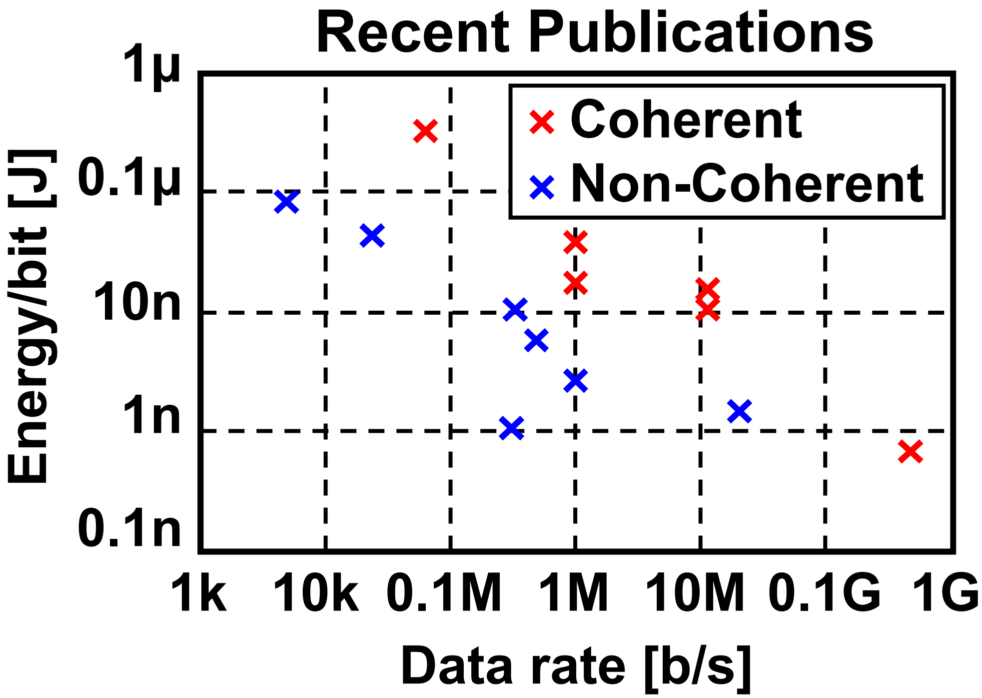
Wireless Sensor Networks



- Key requirements:
  - Long battery life
  - Small form factor
  - 1-to-100m range

Low Data Rate
Simple Architecture
Low Power Radio

Architectural Considerations

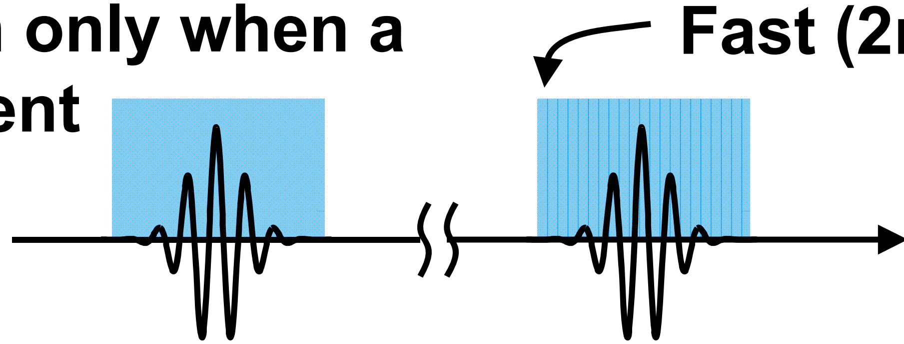


Receiver Trends:
- Data rate ▼, energy/bit ▲
- Non-coherent 10x lower energy

- Pulsed-UWB signaling inherently duty-cycled

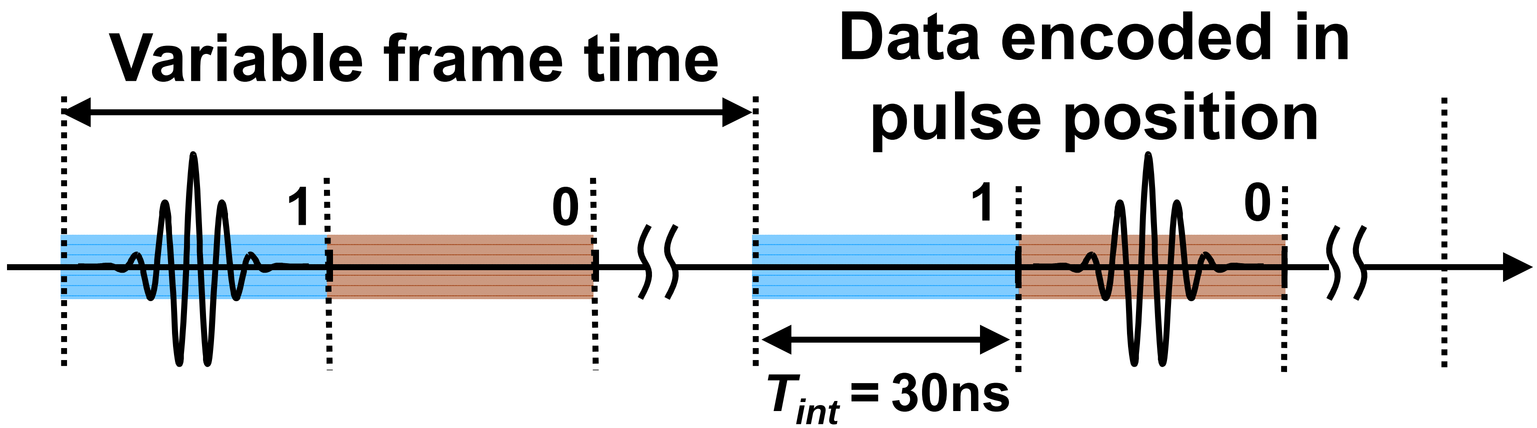
TX and RX on only when a pulse is present

Fast (2ns) turn-on time

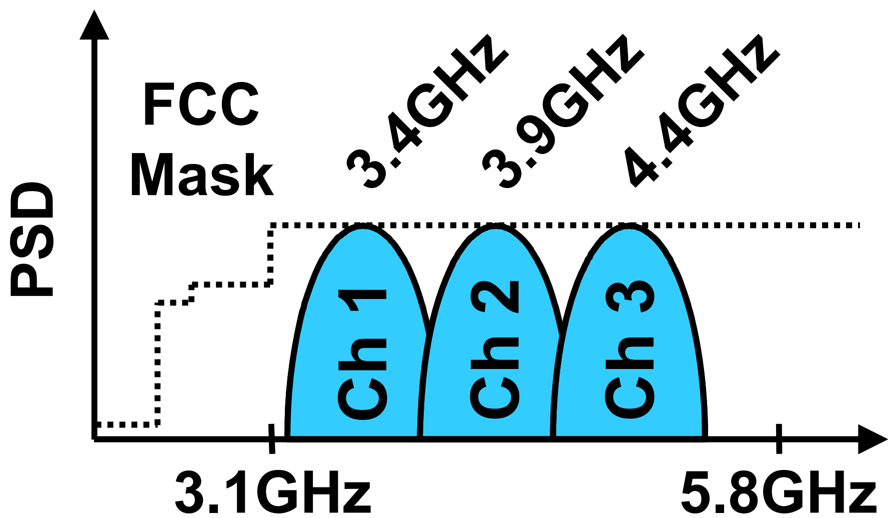


Scalable Signaling

- PPM signaling with non-coherent receiver

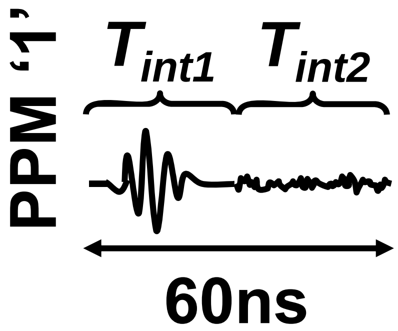


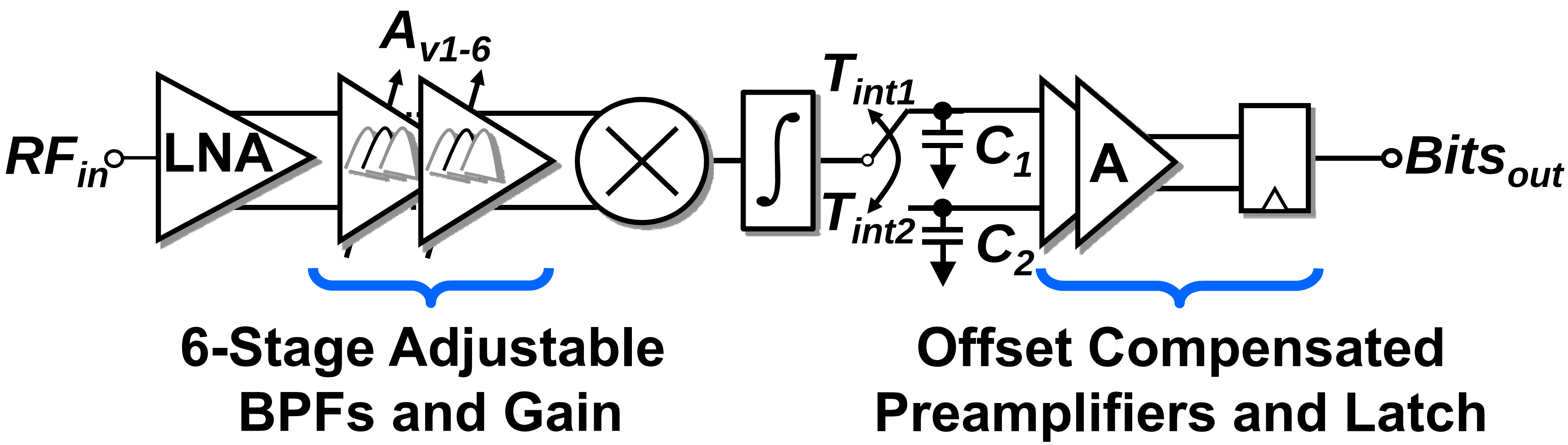
- Three channel frequency plan



- ❑ T_{int} set to maximum channel spreading
- ❑ Multiple channels for narrowband robustness

Receiver Architecture

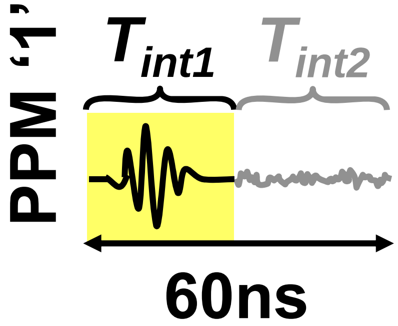


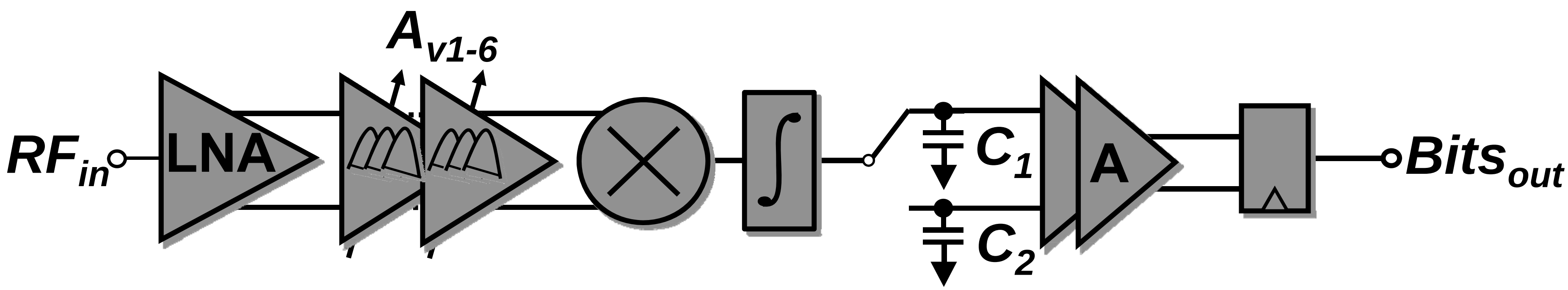


- Energy detection receiver
- All circuits on/off time ~2ns
- No RF PLL; only 30MHz clock

→ **Low Complexity Receiver**

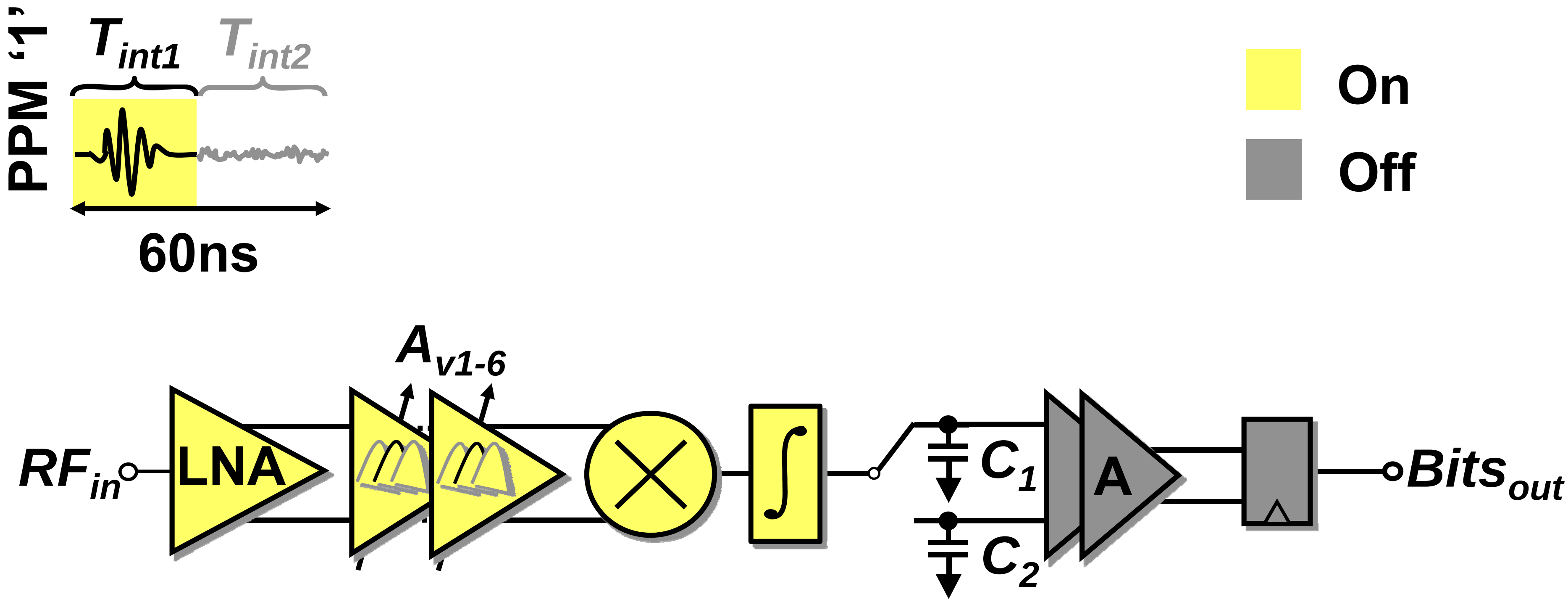
Receiver Operation



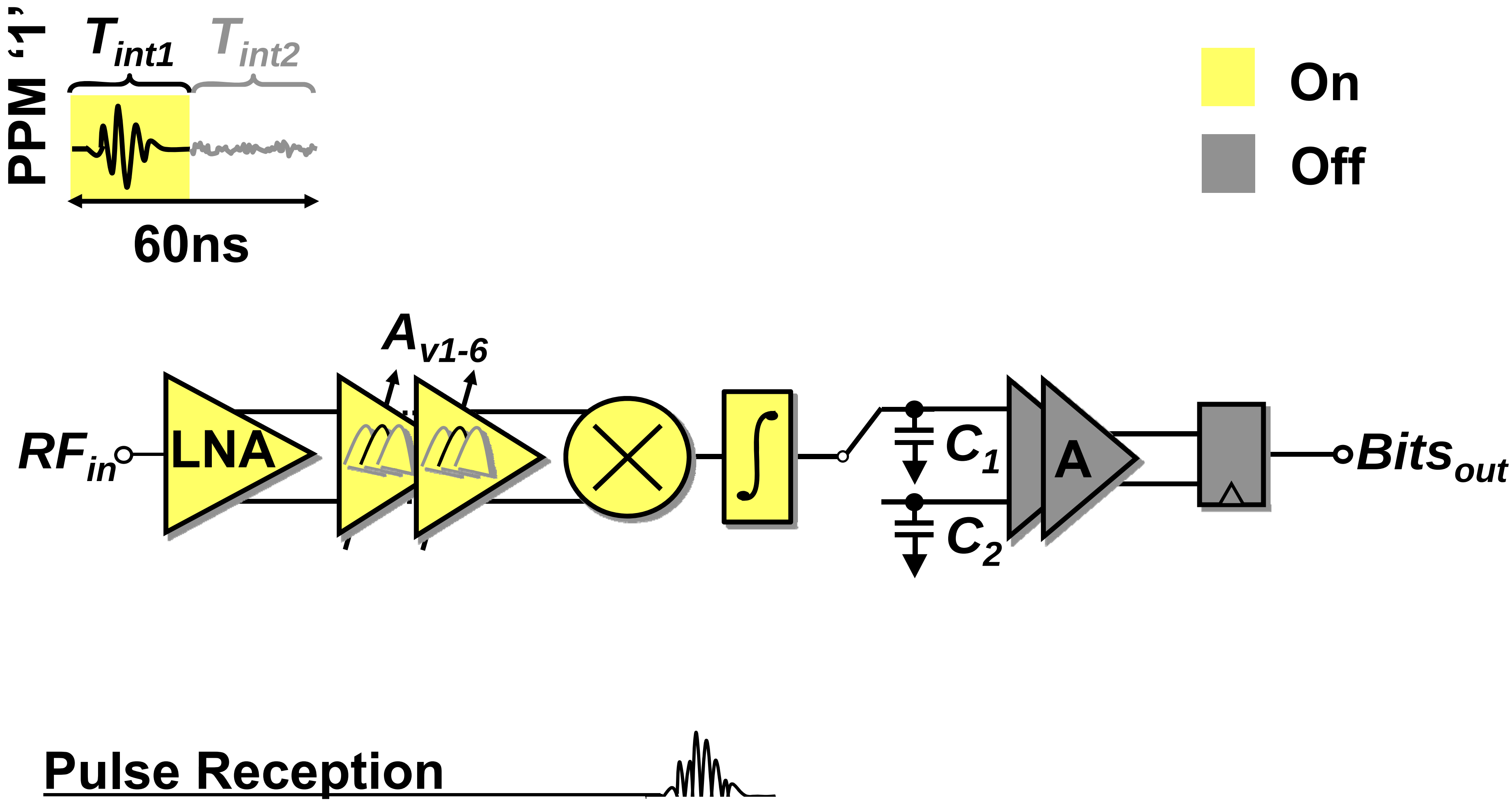


Receiving a '1'

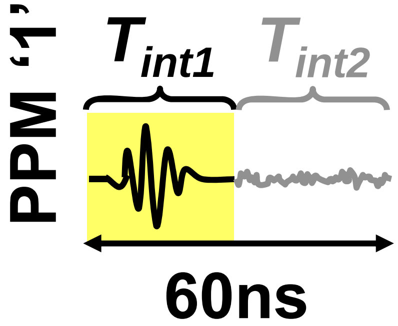
Receiver Operation

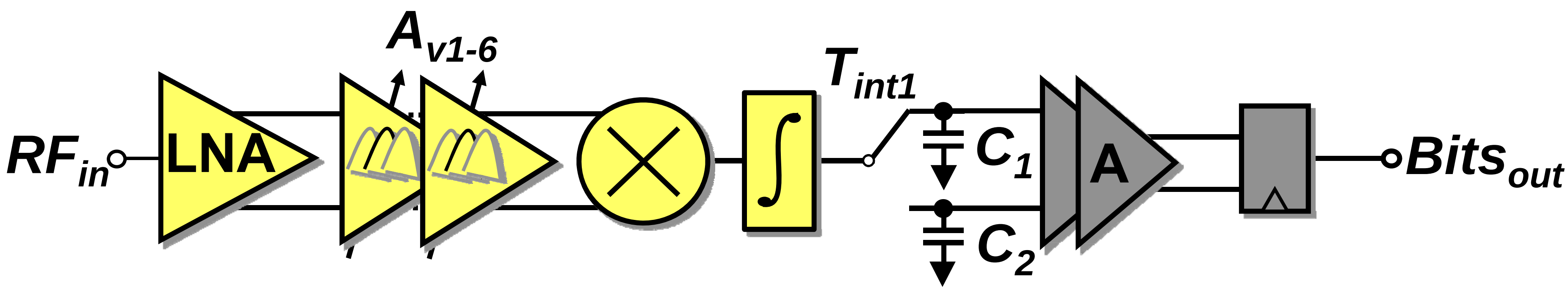


Receiver Operation

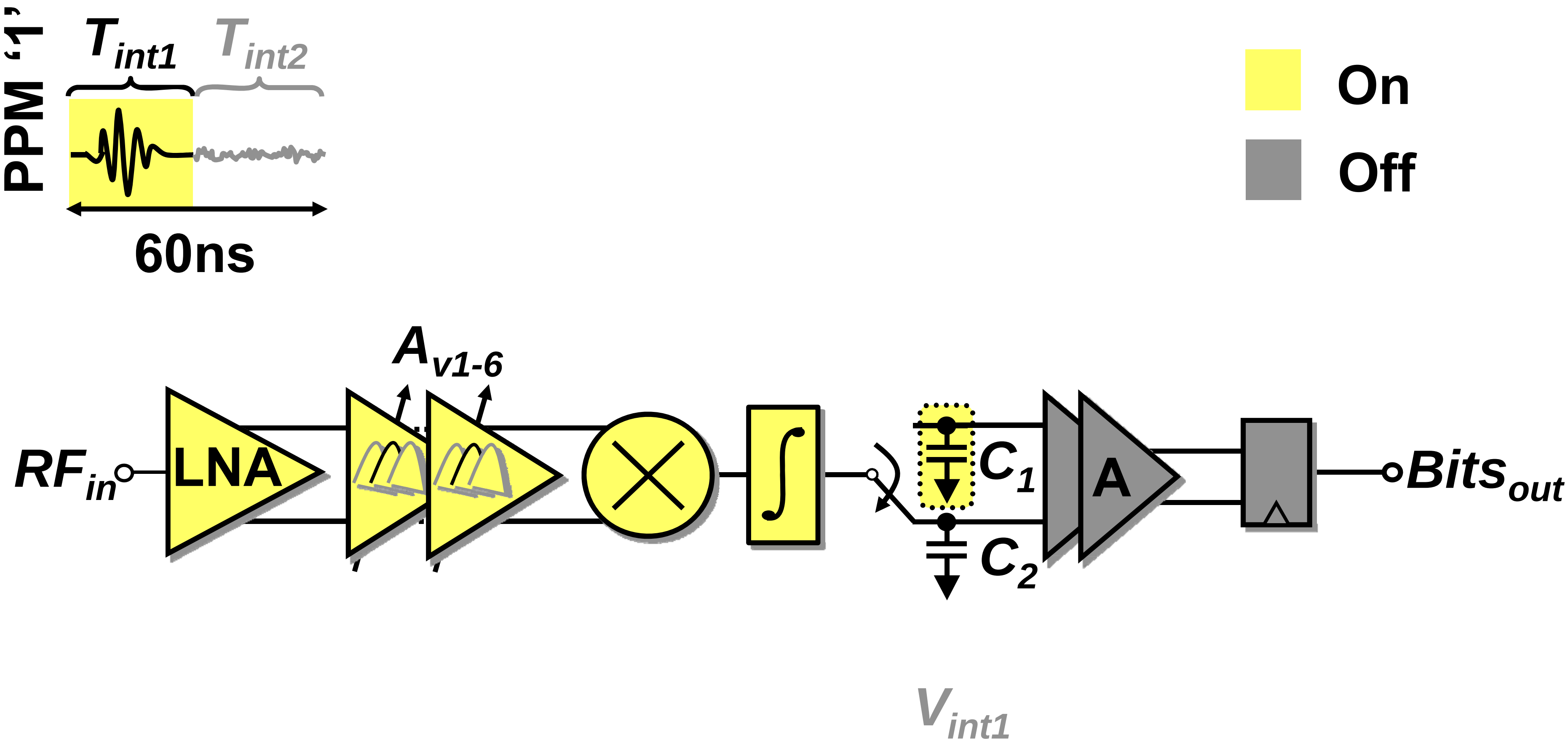


Receiver Operation



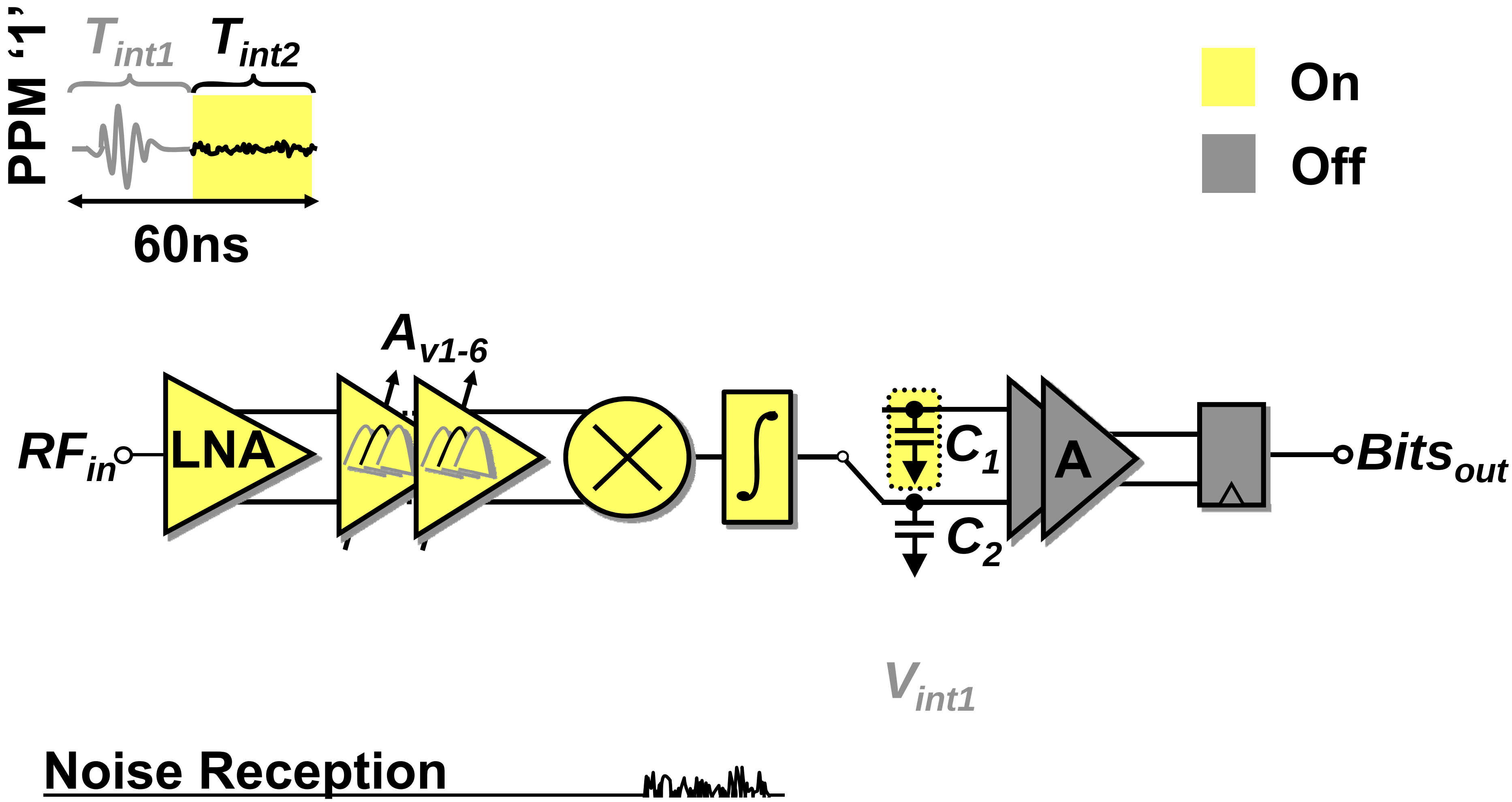


Receiver Operation



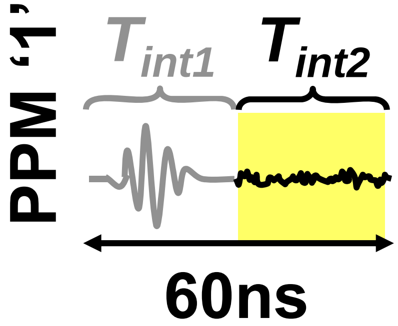
Pulse Storage

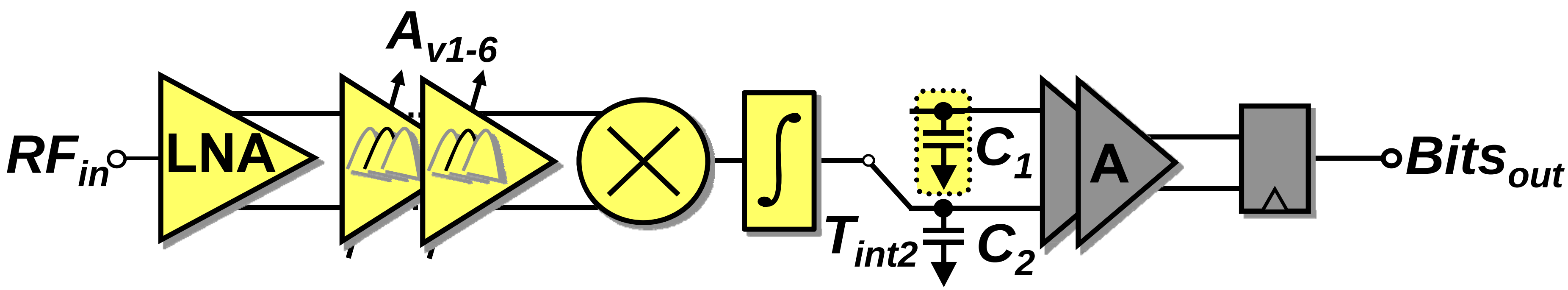
Receiver Operation



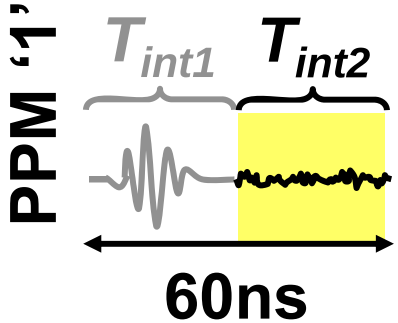
Noise Reception

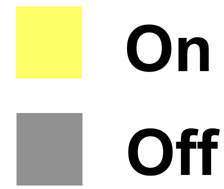
Receiver Operation

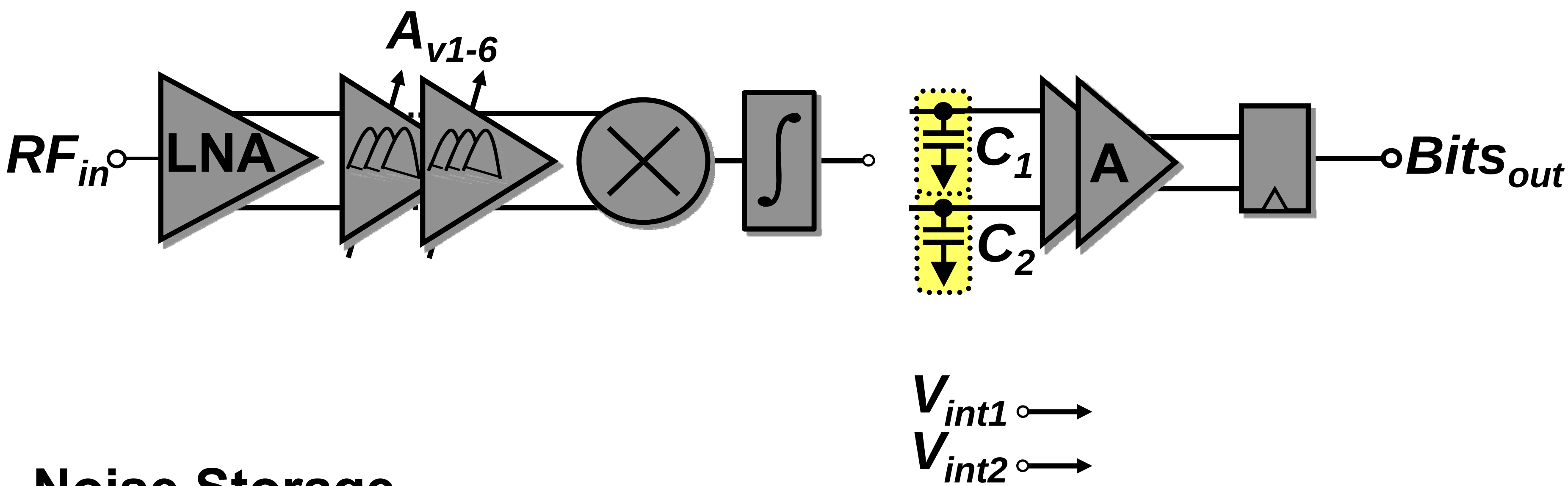




Receiver Operation

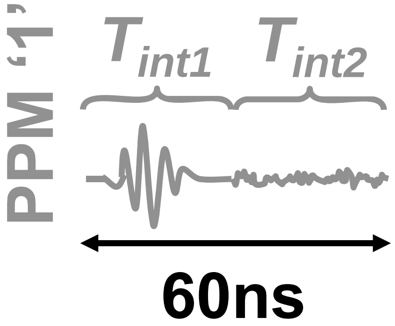






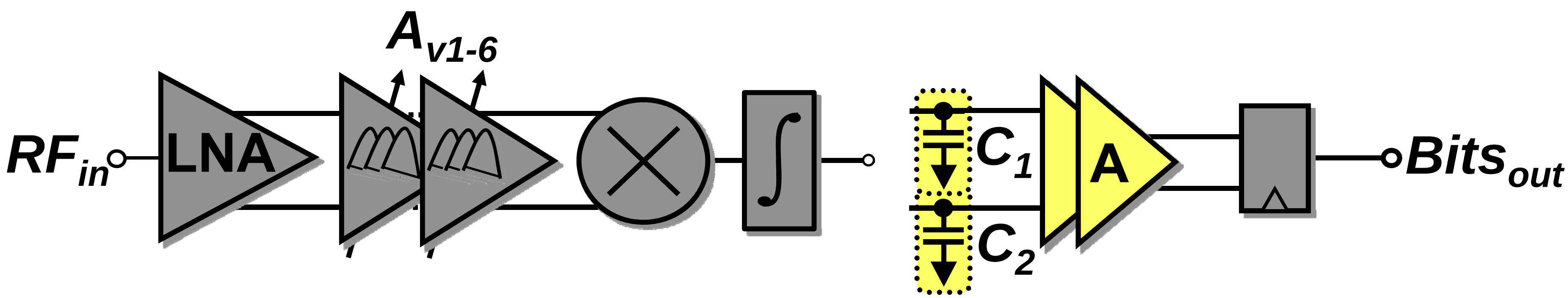
Noise Storage

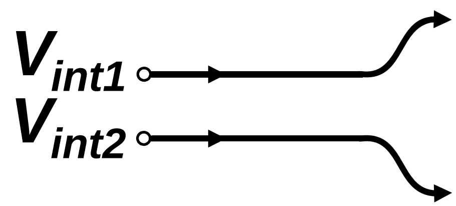
Receiver Operation



On

Off

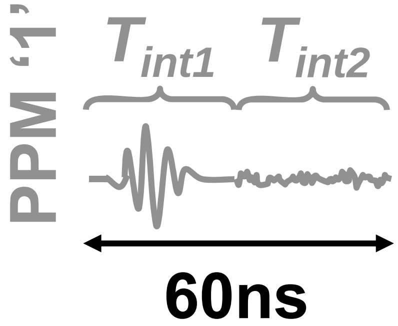


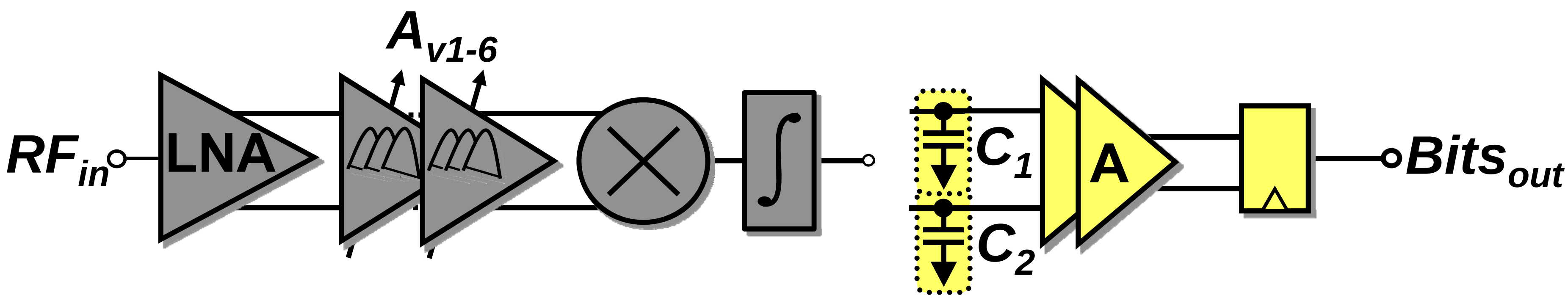


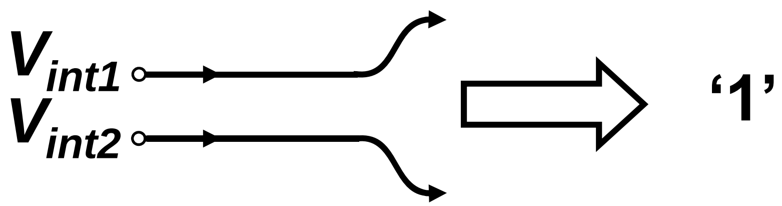
Relative Compare

(DC offsets and path non-idealities automatically normalized)

Receiver Operation

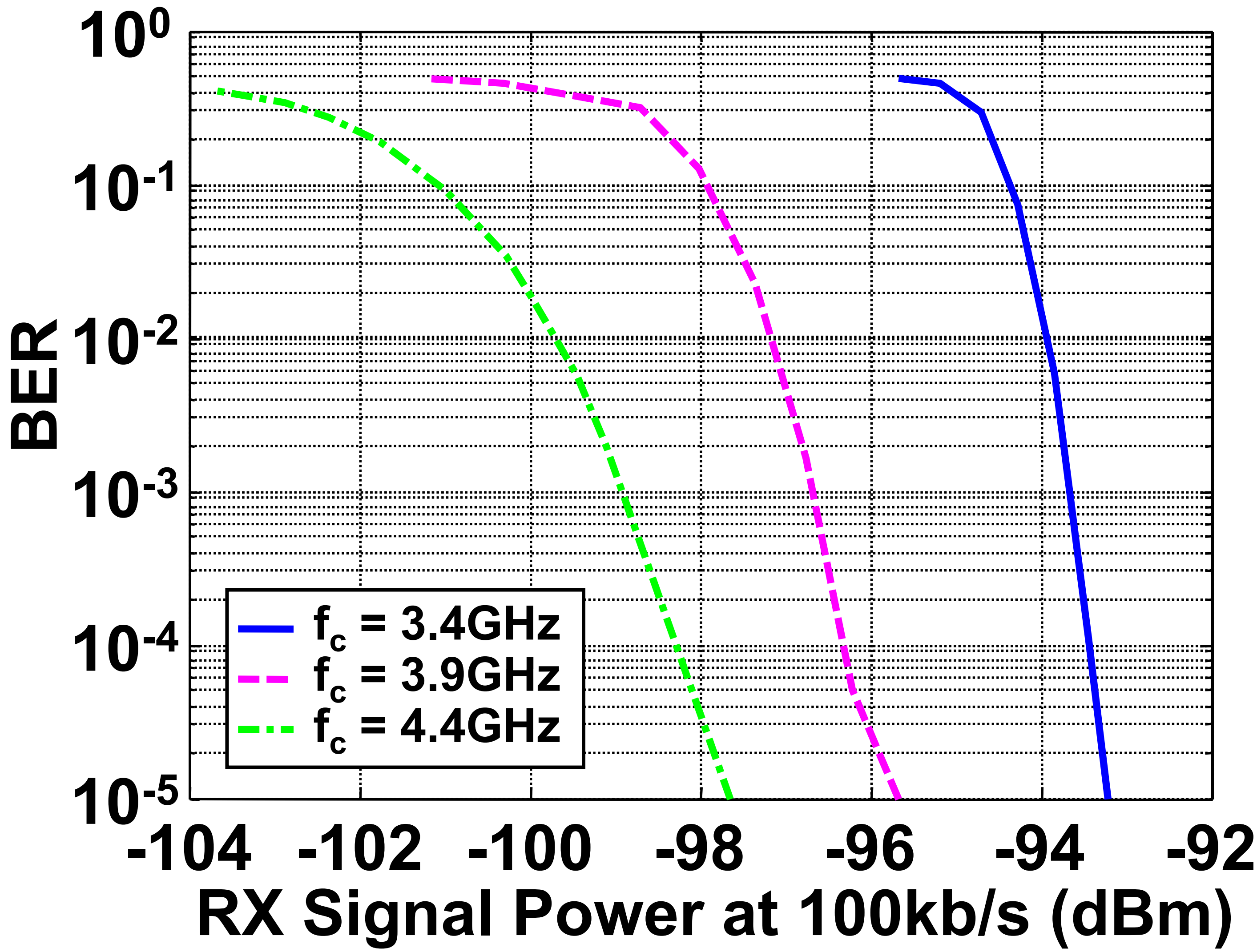






Bit Evaluation

Bit Error Rate

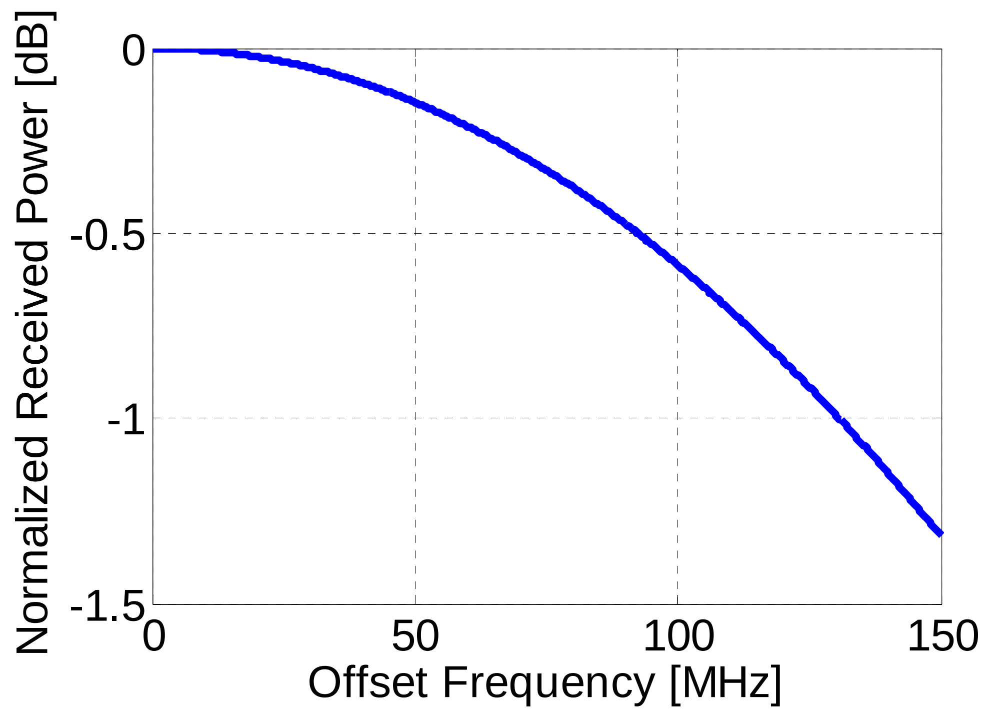


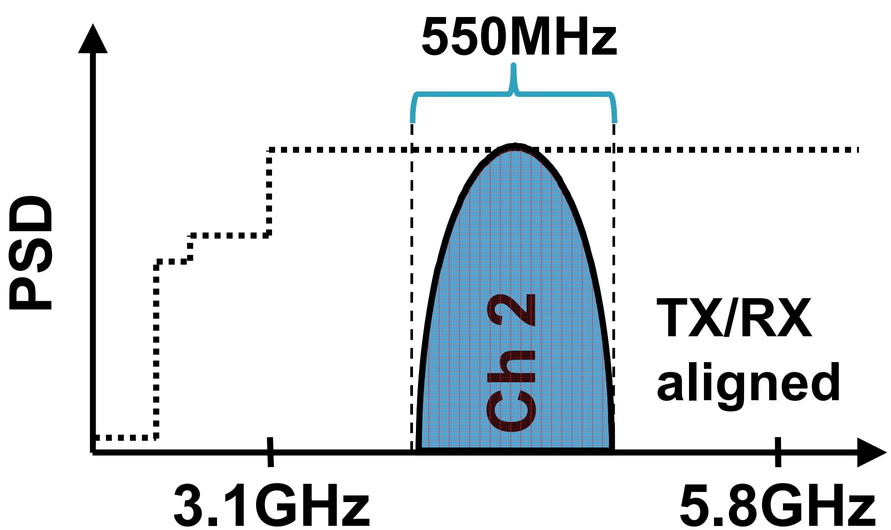
-99dBm Sensitivity for 10^{-3} BER in 4.4GHz Band

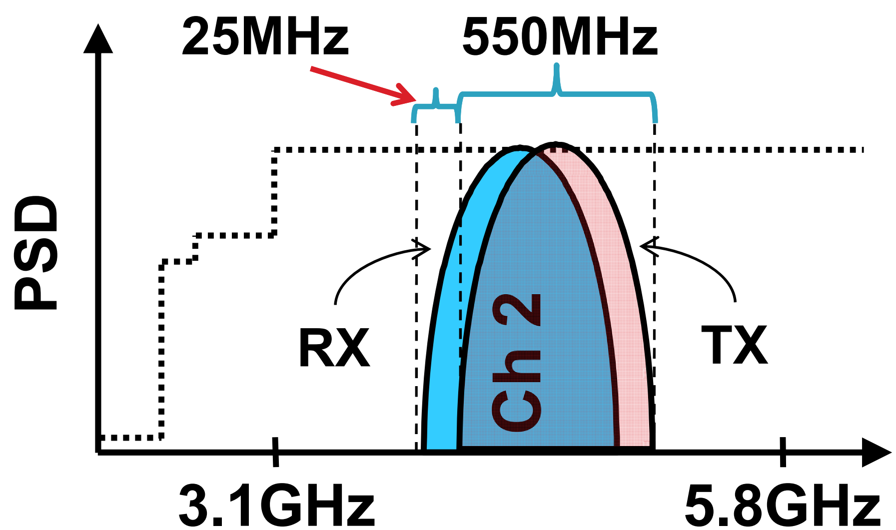
Frequency Tolerances

- **Wideband, non-coherent signaling relaxes frequency tolerances**
- **E.g. At 6000ppm TX accuracy (25MHz), we lose only 0.04dB of received power**

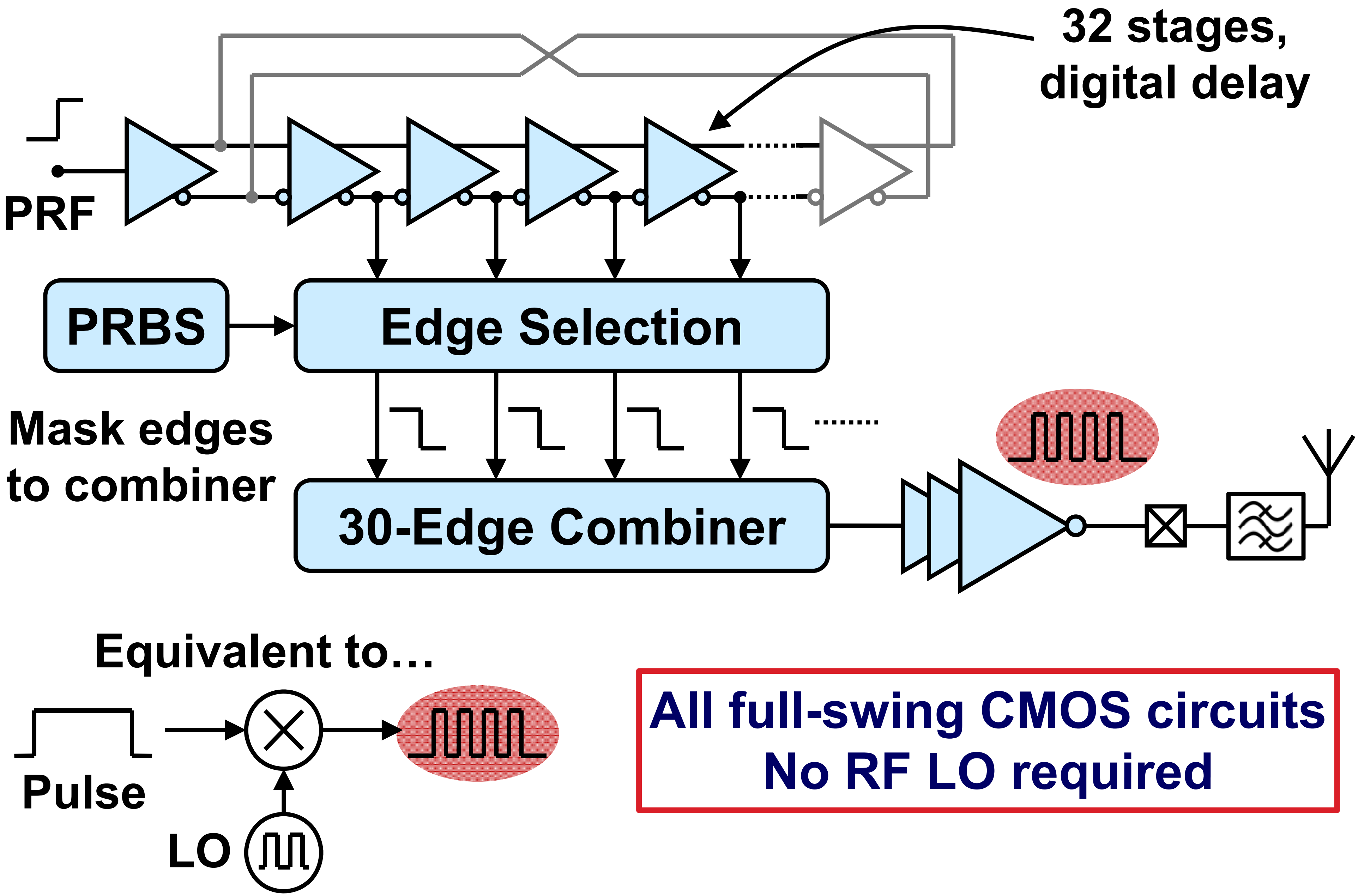
Use simple, low-power frequency generation







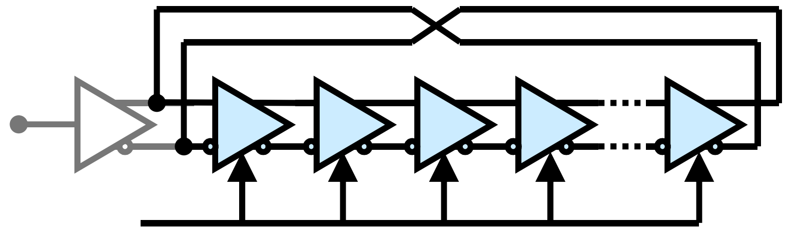
Transmitter Block Diagram



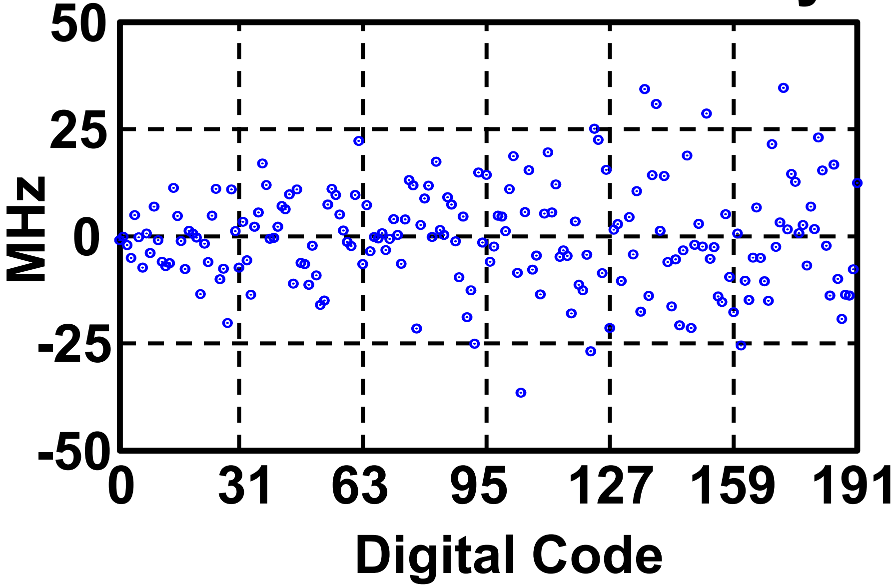
All full-swing CMOS circuits
No RF LO required

RF Calibration

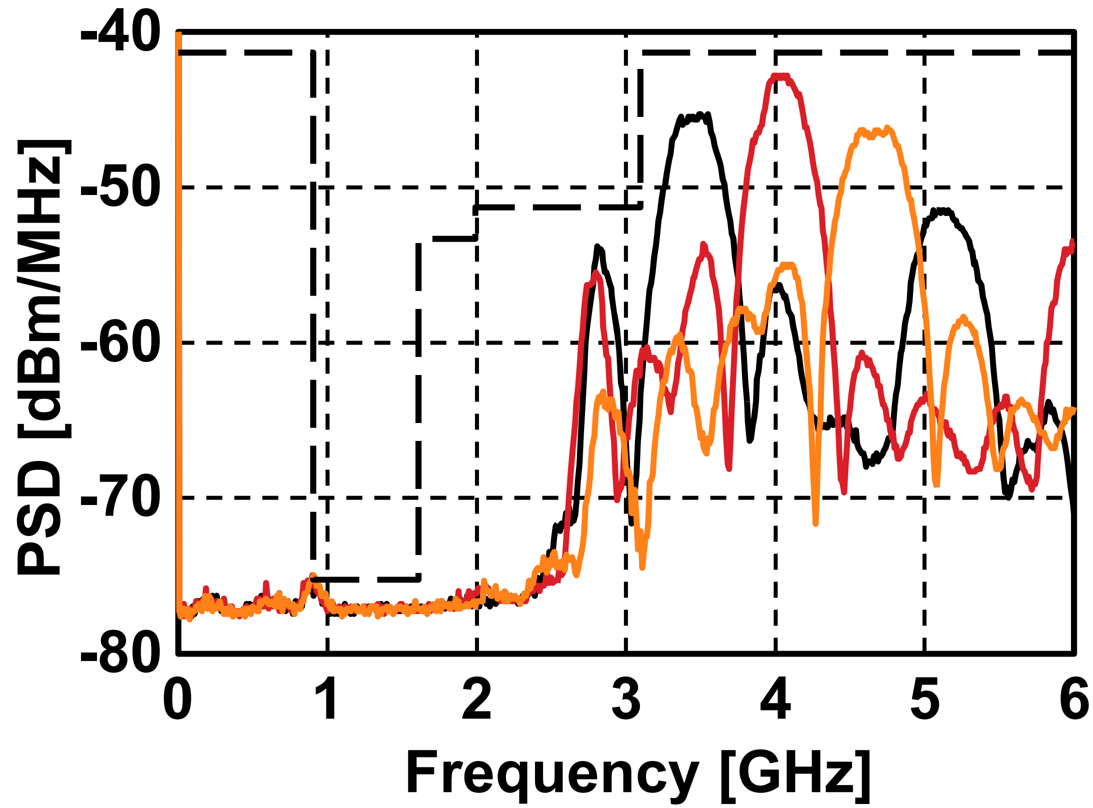
Calibrate delay in ring



Calibration Accuracy



3-Channel Spectrum



Digital calibration algorithm sets RF center frequency to within 6000ppm

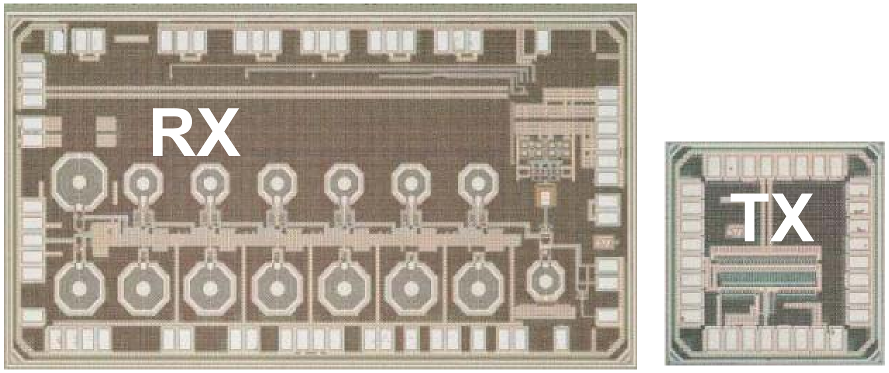
Chip Results

	Transmitter	Receiver
Die area	$0.2x0.4mm^2$	$1.0x2.2mm^2$
V_{DD}	1.0V	0.5-0.65V
Leakage	96μW	3.5μW
Power	0.72mW	41.8mW
Energy/bit (16.7Mb/s)	43pJ/bit	2.5nJ/bit

90nm CMOS

1mm

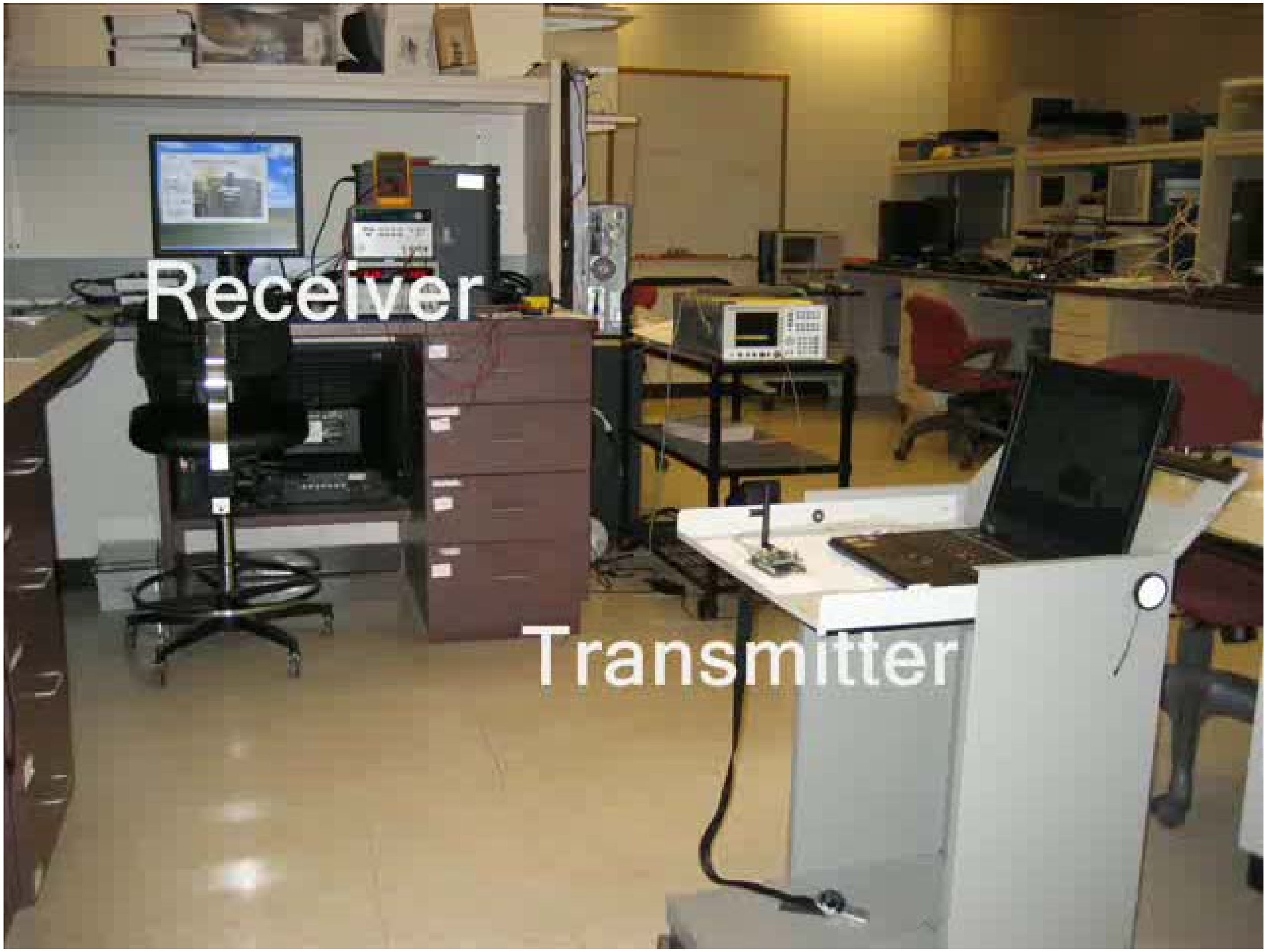
[F. Lee, ISSCC2007]



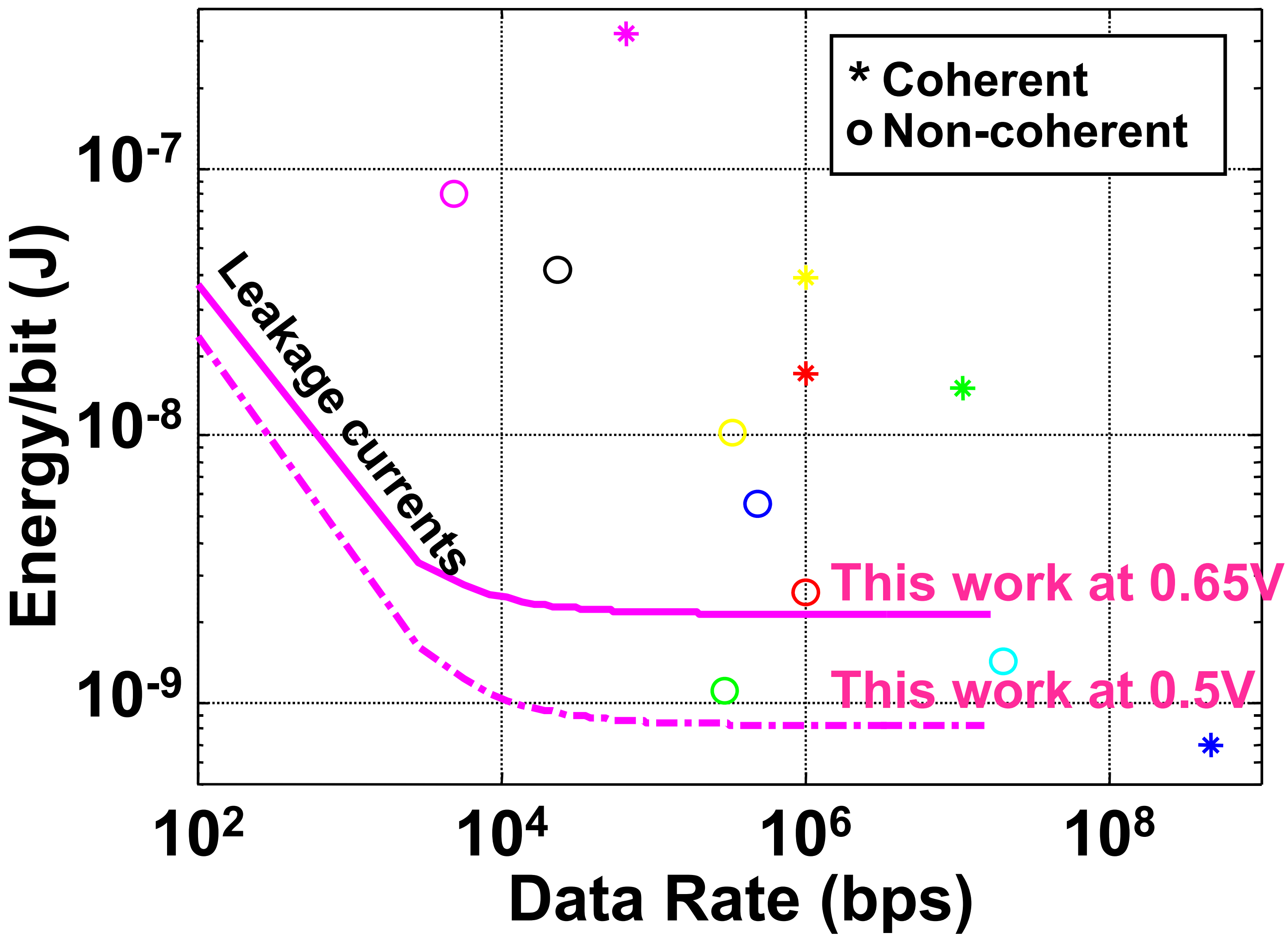
[D. Wentzloff, ISSCC2007]

- **Digital TX, non-coherent RX ► no RF oscillators**
- **Receiver actually dominates energy budget**

Wireless Demonstration



Receiver Figure of Merit



Can operate efficiently down to low data rates

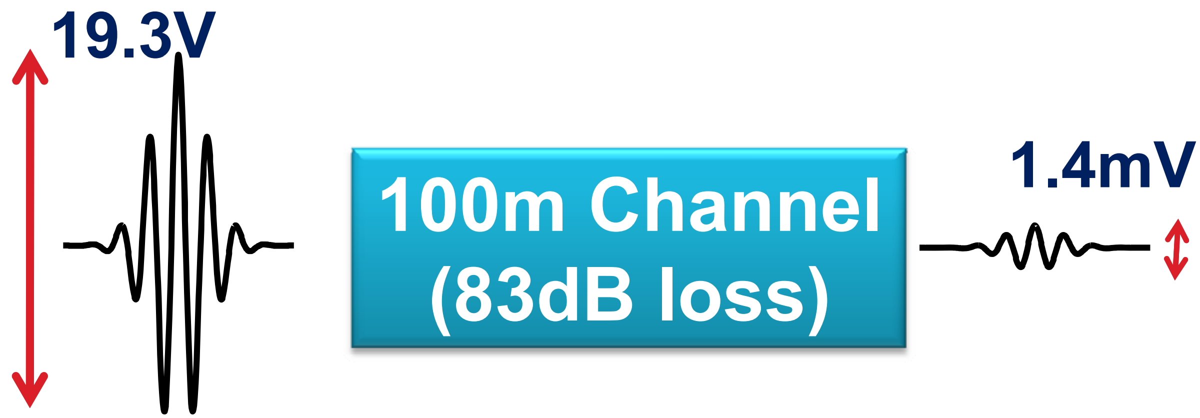
Maximizing Range of Low-Rate Systems

- **Low-data rate systems are peak-power limited**
  E.g. 10kbps system:

<u>1st Goal: Maximize average power:</u>

P_{avg} = -41.3dBm/Mhz
P_{pk} ≈ 16dBm/50MHz

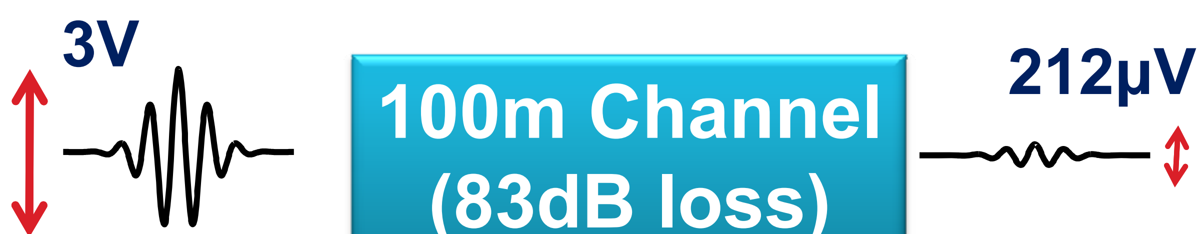
peak power violation!



<u>2nd Goal: Maximize peak power:</u>

P_{avg} = -57.4dBm/Mhz
P_{pk} ≈ 0dBm/50MHz

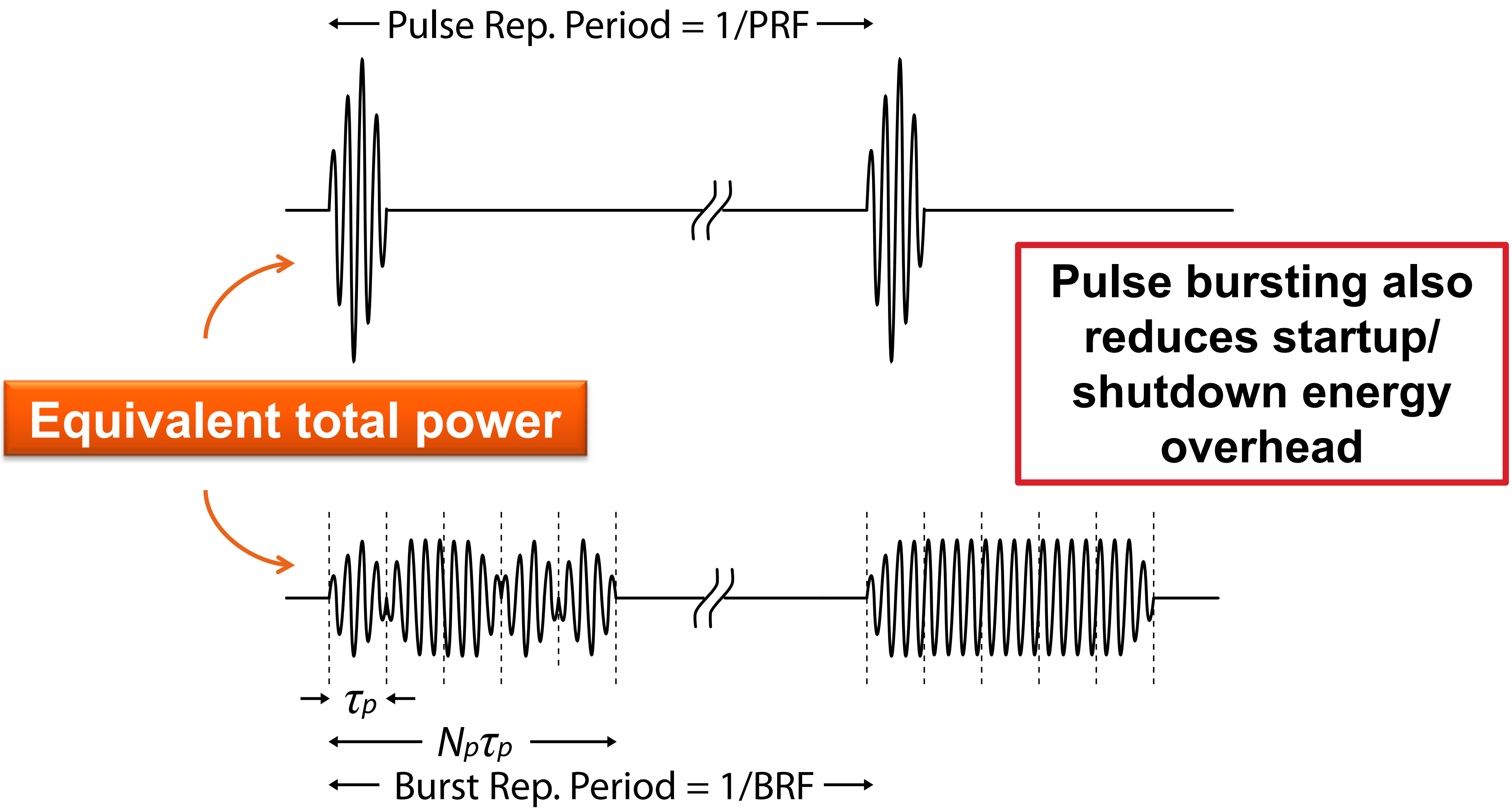
16dB less total
power at receiver!



$3V_{pk\text{-}pk}$ difficult to achieve in 1V CMOS

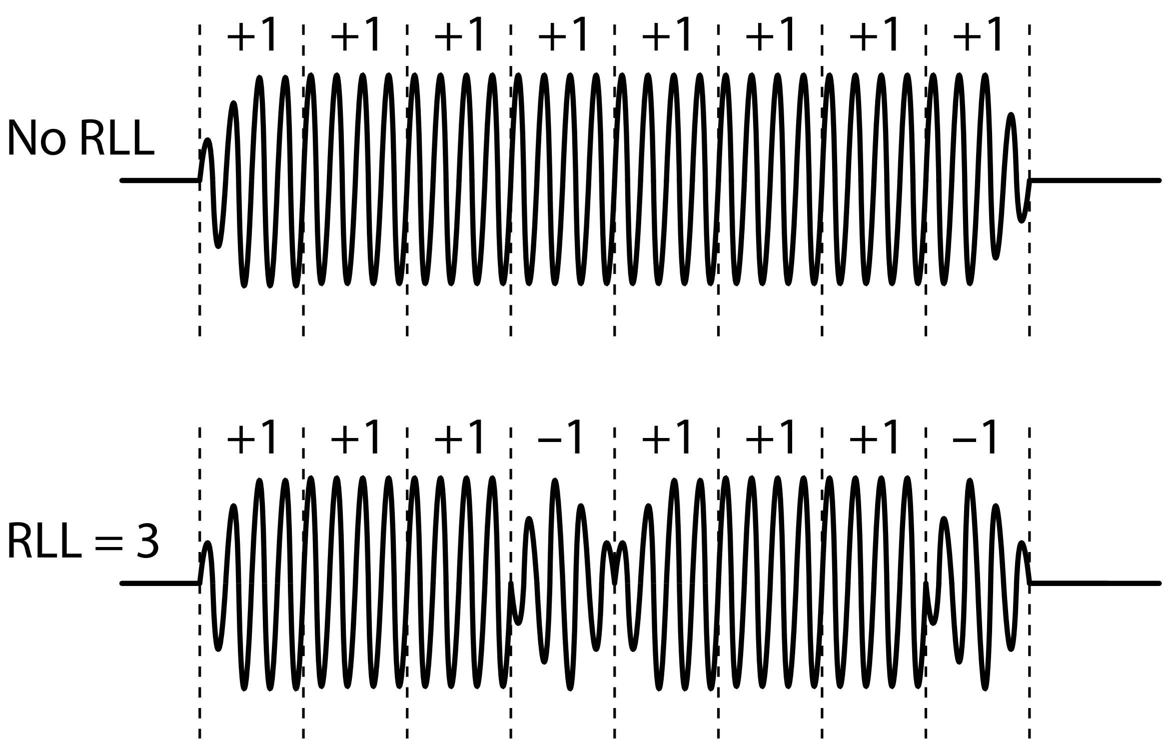
Maximizing Range of Low-Rate Systems

- **Instead, maximize voltage swings under process and FCC limits and increase the *spreading factor* (multiple pulses per bit)**



Increasing Range Under FCC Limits

- **Pulse bursts must be BPSK-scrambled to retain average PSD properties**
  - **Long runs with no phase inversions produces large peak-power content when spectrum analyzer is in peak-hold mode**

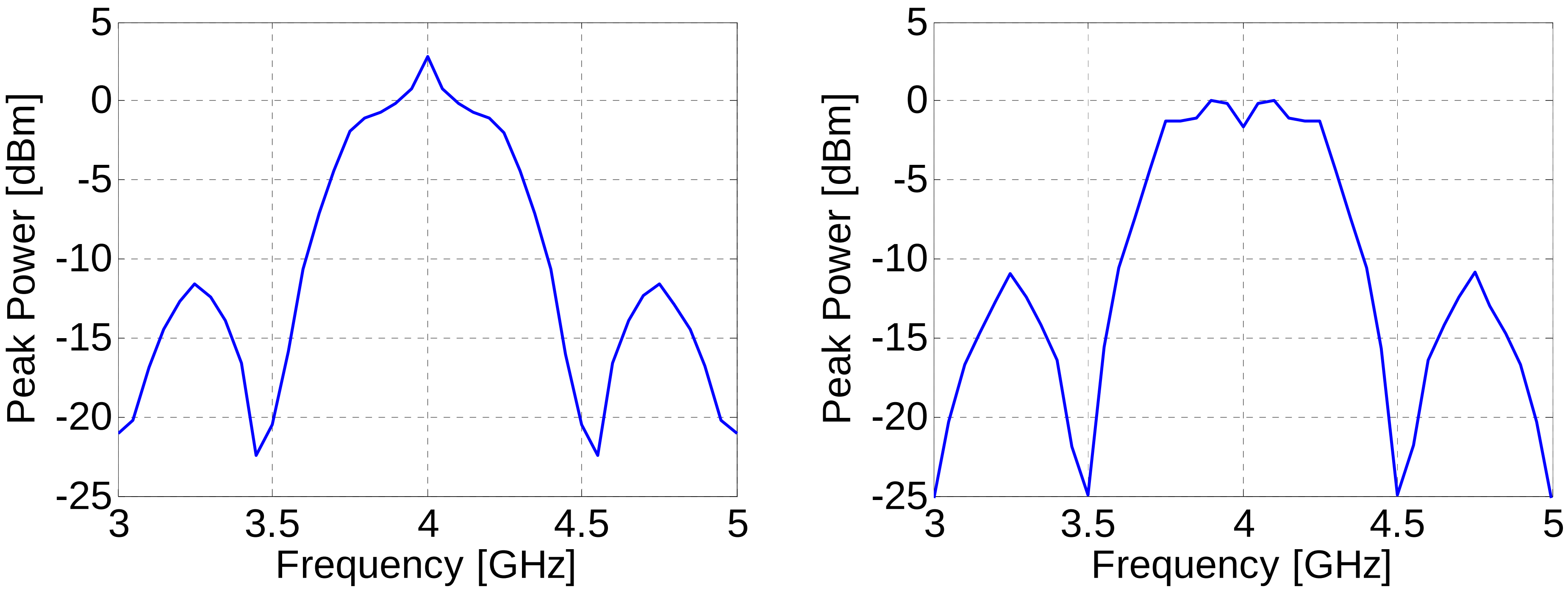


Run-length limits can reduce peak-power by up to 3dB for bursts with 4 or more pulses

Run Length Limiting

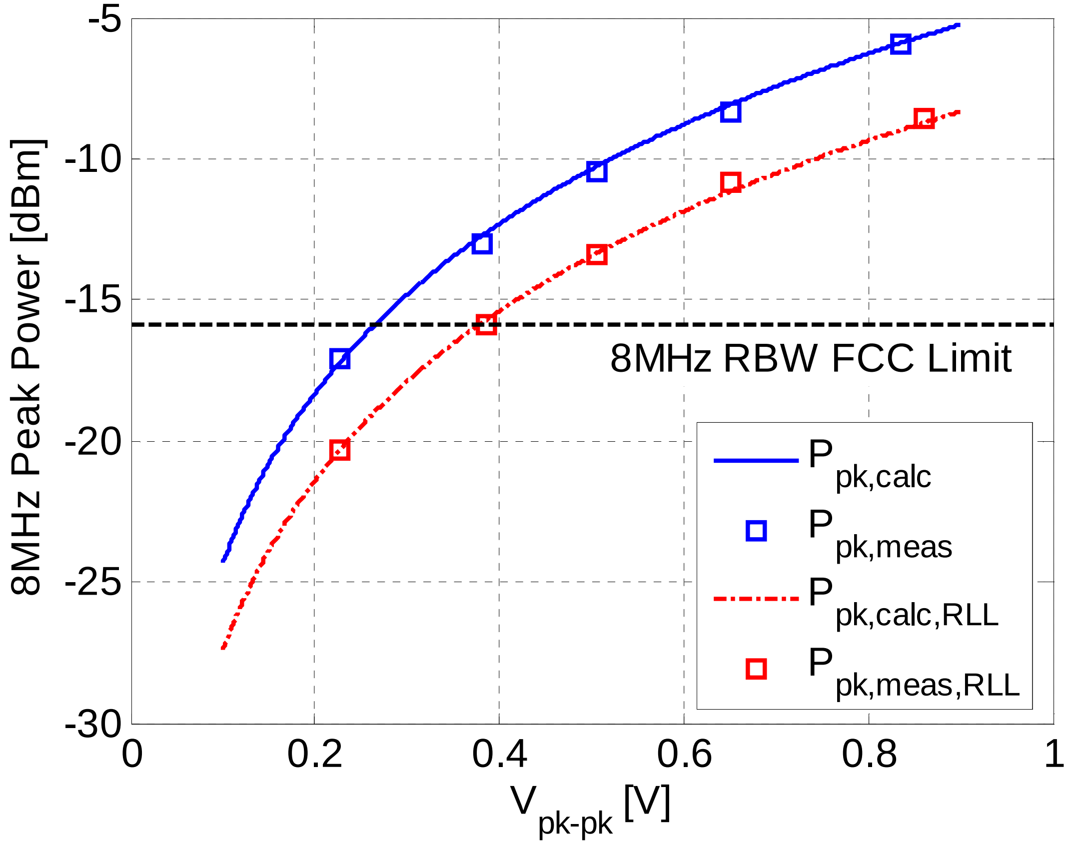
- Simple to add state logic to output of an LFSR
- Ideally doesn't affect *average* PSD
- E.g. simulations of spectrum analyzer in peak-hold mode:

Peak power reduced by 3dB



Results

- **Adding RLL can increase voltage swings by 3dB**



- **2x reduction in spreading factor and <u>receiver observations</u>**
- **E.g. maximizing both peak and average power at 10kbps:**

	No RLL	With RLL
$V_{pk\text{-}pk}$	260 mV	370 mV
BRF	3.3 MHz	1.7 MHz
Spread Factor	5280 pulses/bit	2720 pulses/bit

RLL decreases system energy consumption by 1.9x

Conclusions

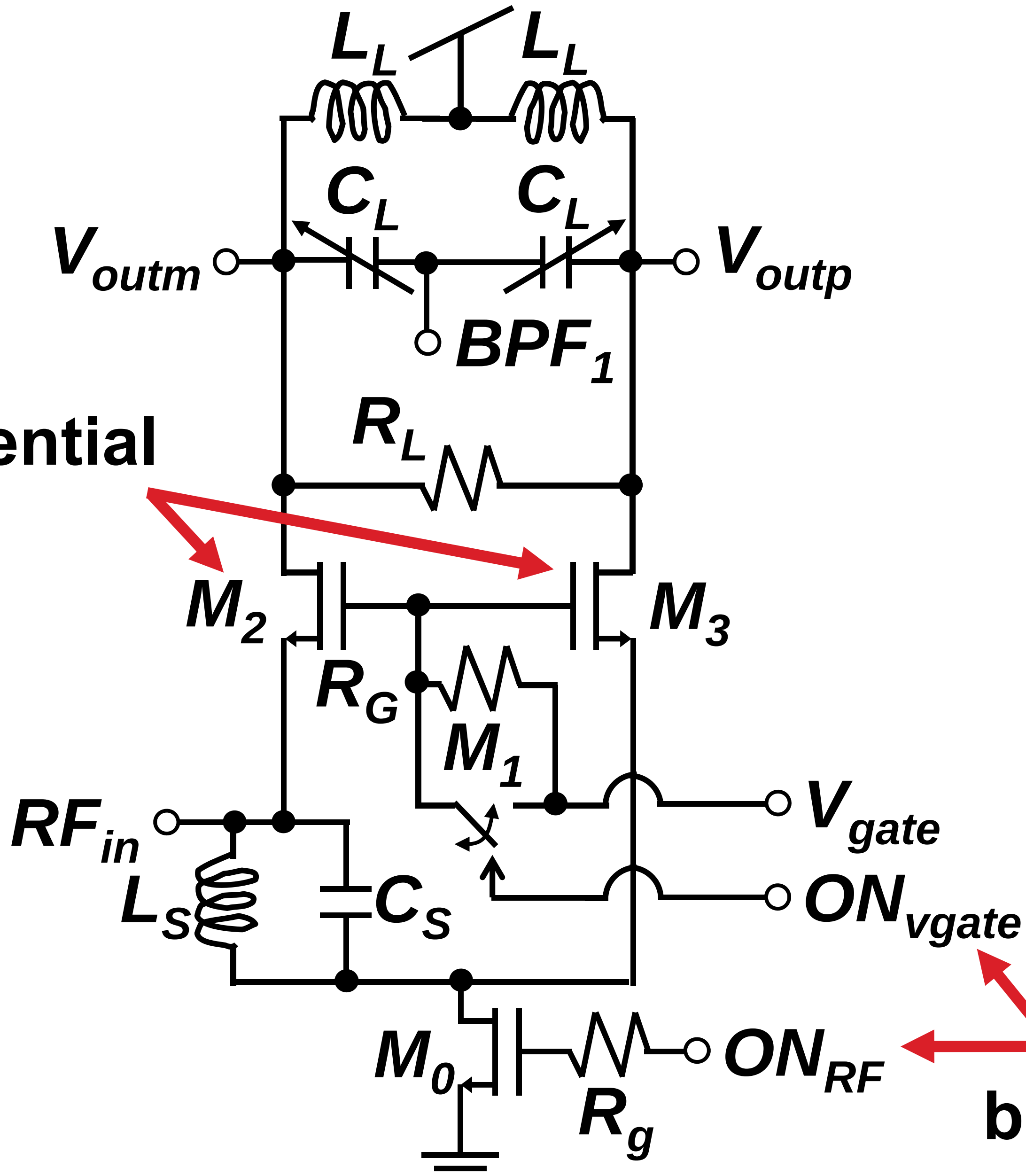
- Energy-detecting receiver
  - Simple architecture → 2.5nJ/bit
- All-digital transmitter
  - Only CV^2 switching power and subthreshold leakage power → 43pJ/bit
- Non-coherent system does not require high speed synchronization or PLLs
- Run-length limits in transmitter phase scrambler can increase low-rate system energy efficiency when maximizing communication distance

Acknowledgements: C2S2, NSF, DARPA, NSERC
IC fabrication provided by STMicroelectronics

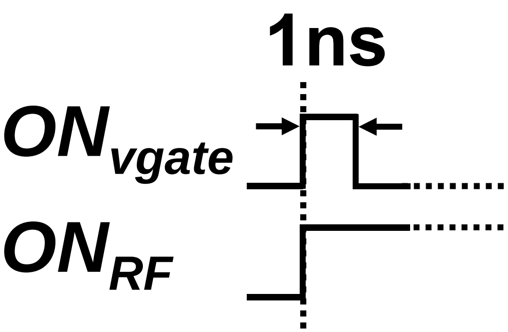
Backup Slides

0.5V-0.65V *LNA*

Common-gate single-to-differential conversion

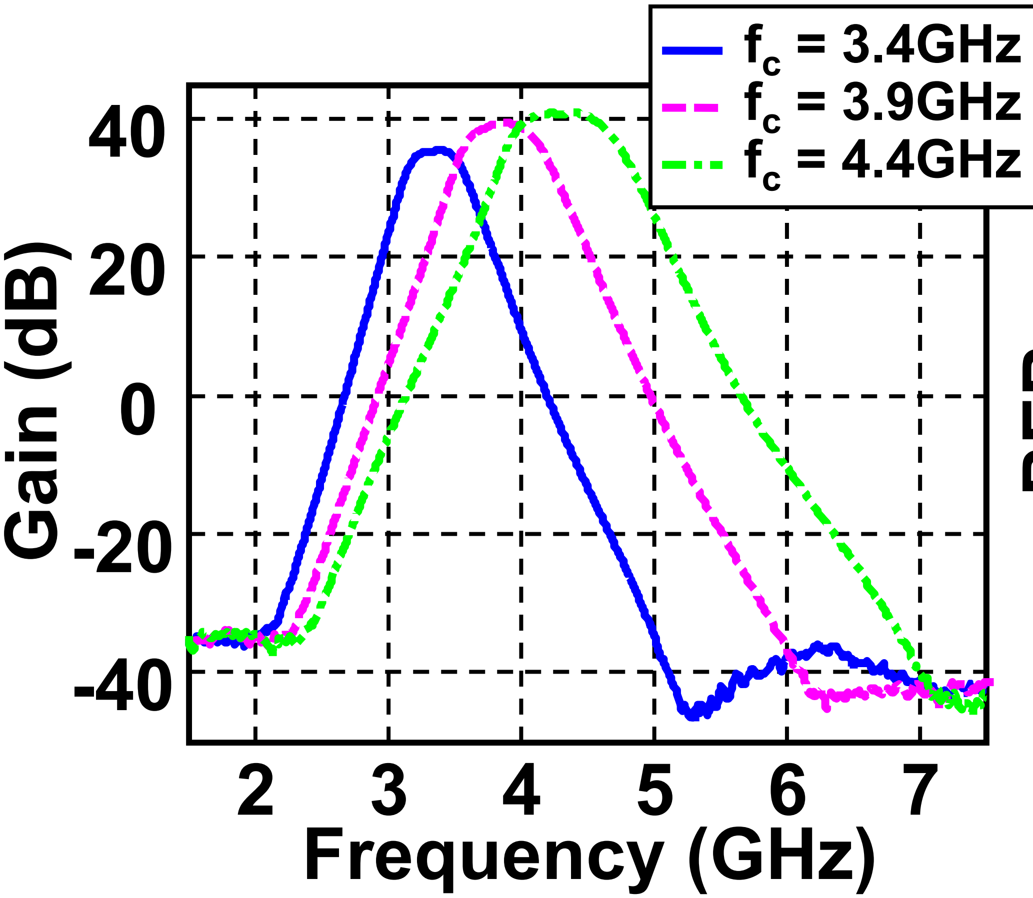


Dynamically biased in ~2ns

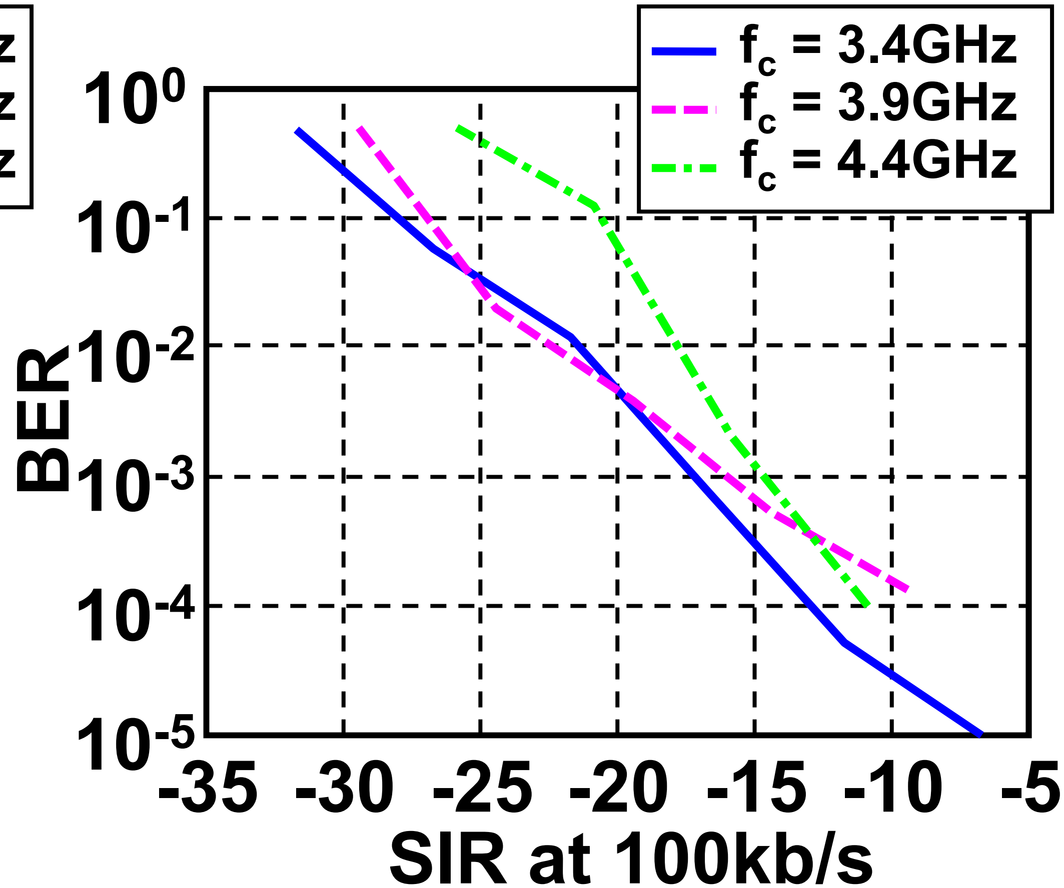


Measurement Results

RF Gain



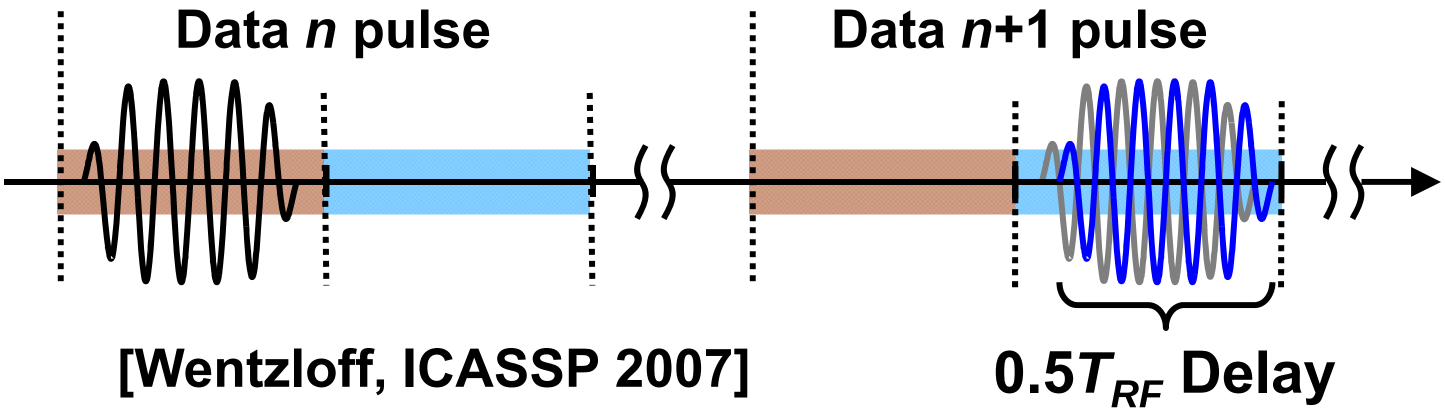
Performance in interference



Out-of-band SIR: -15dBm at 2.45GHz, -20dBm at 5.45GHz

Delay-Based BPSK Scrambling

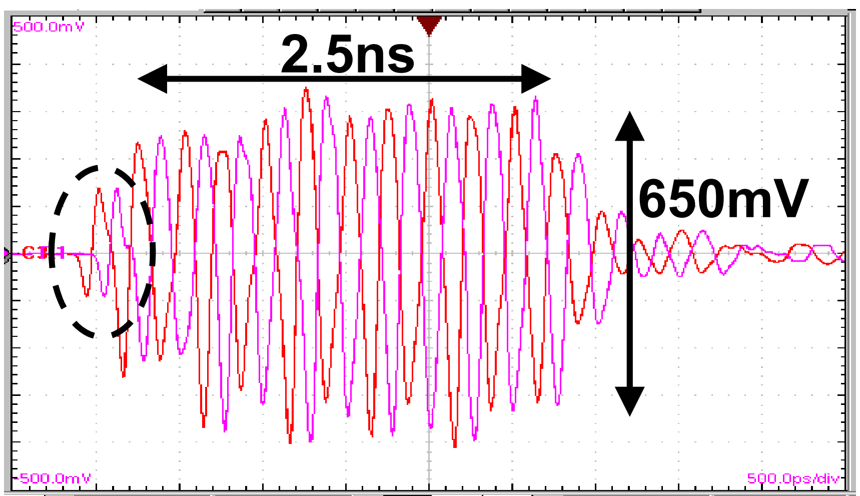
- Architecture enables new signaling scheme



[Wentzloff, ICASSP 2007]

Emulates BPSK with minimal overhead

DB-BPSK Pulses



PPM + DB-BPSK Spectrum