A Low-Voltage 1Mb FeRAM in 0.13µm CMOS Featuring Time-to-Digital Sensing for Expanded Operating Margin

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ISSCC 2011

Sensing Challenge for Non-Volatile RAM

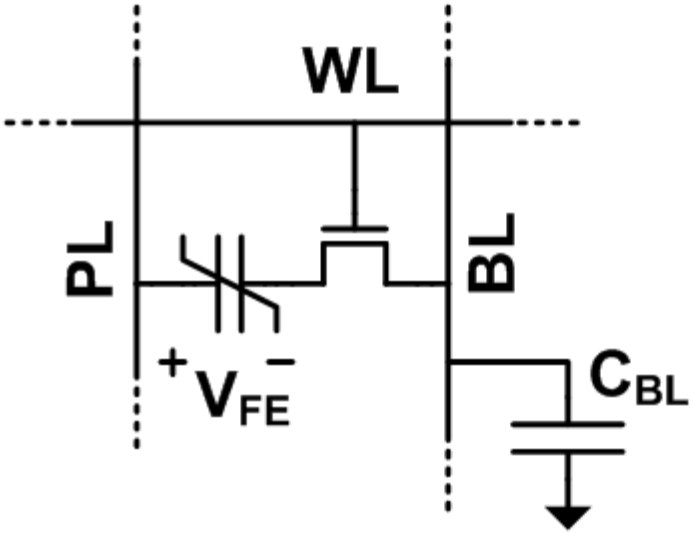
	NAND Flash	NOR Flash	PRAM	FeRAM	MRAM
Density (Mb/mm^2)	216	20.6	5.86	1.47	0.502
CMOS node	32nm	65nm	90nm	150nm	130nm
Timescale of bitcell	1.89ms (prog.)	70ns (read) 435µs (prog.)	78ns (read) 430ns (write)	70ns (read)	32ns (read) 70ns (write)
Endurance	$\sim 10^5$	$\sim 10^5$	$>10^5$	$>10^{13}$	$>10^{15}$
Energy per written bit	1.4nJ(prog.)	—	9.8nJ	50pJ	253pJ
Citation	Lee '11 JSSC	Villa '08 JSSC	Lee '08 JSSC	Kang '06 VLSI	Sugib. '07 JSSC

Sensing considerations

- Technology scaling: mismatch tolerance and low voltage operation
- Area efficiency
- Time scale of cell >> F04 delay

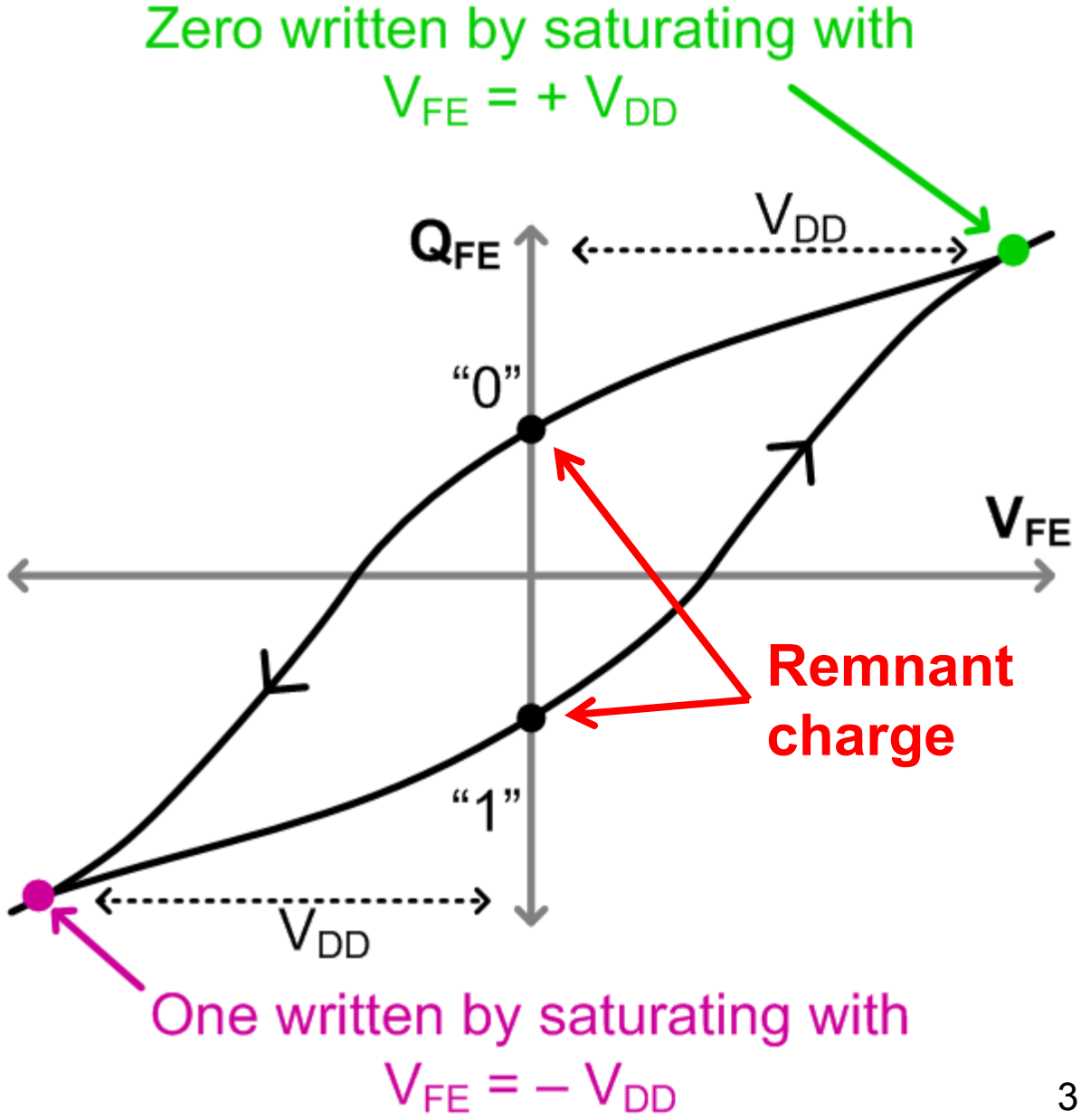
Time-to-digital sensing for low-energy FeRAM

Non-volatile Ferroelectric Capacitor (FeCap)

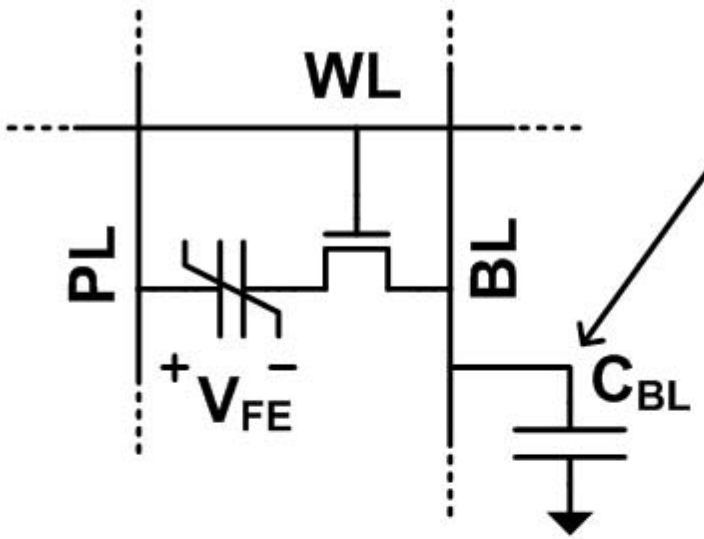


$V_{WL} = V_{DD} + 0.7V$

	V_{PL}	V_{BL}
Write "0"	V_{DD}	0V
Write "1"	0V	V_{DD}
Retention	0V	0V

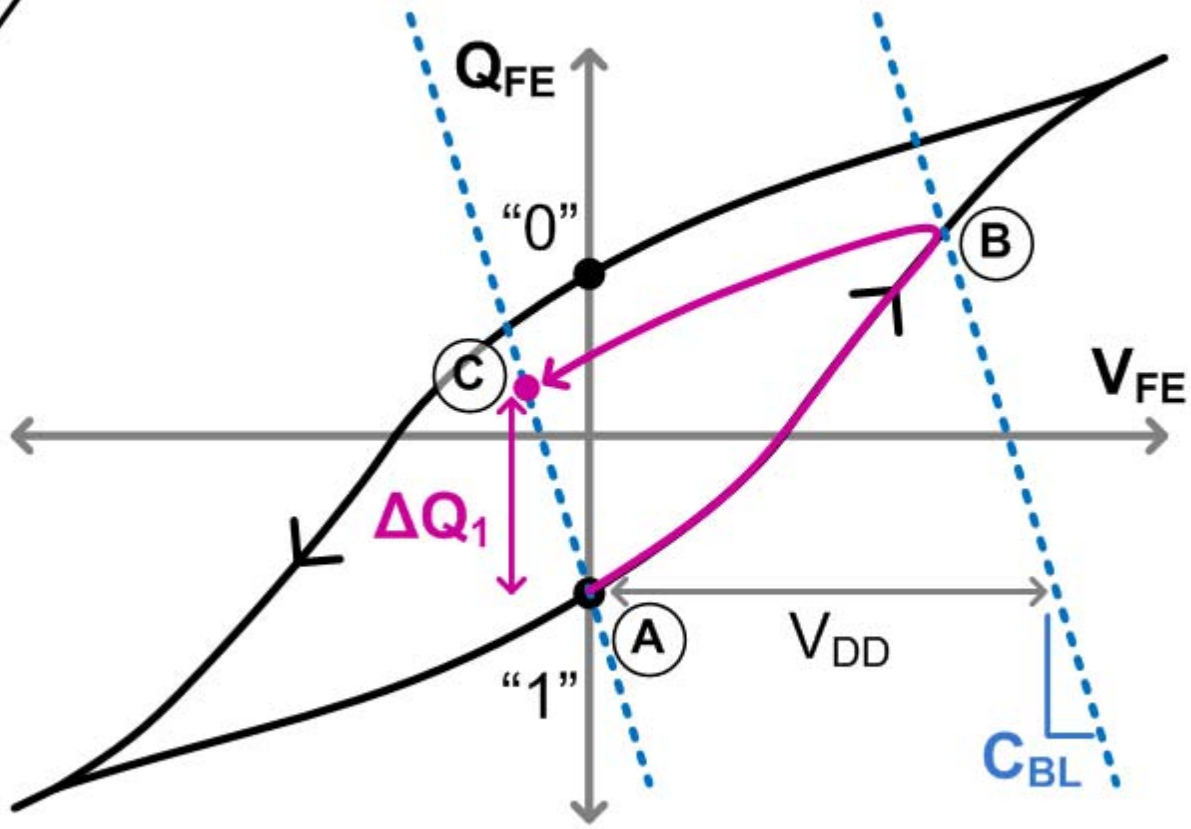


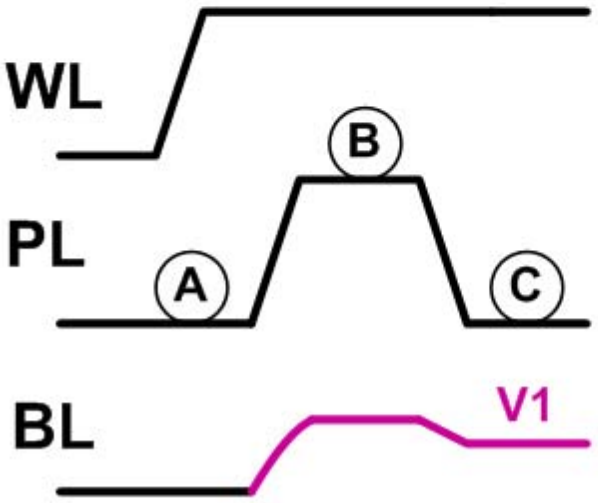
Non-volatile Ferroelectric Capacitor (FeCap)



Floating bitline precharged to 0V

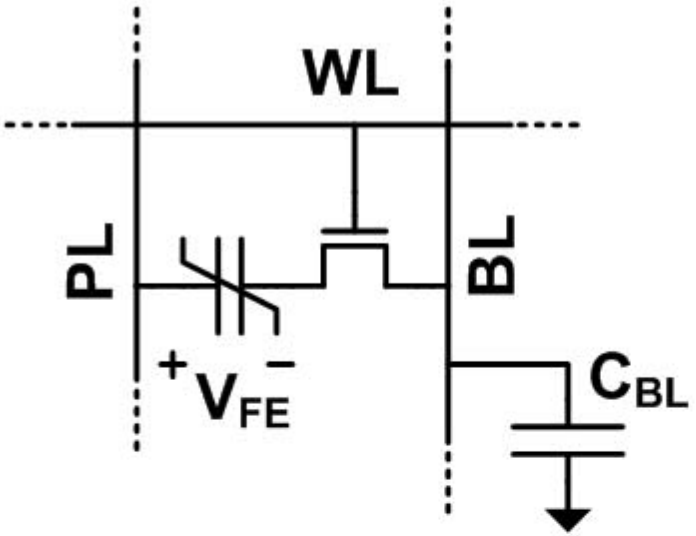
Read “1”



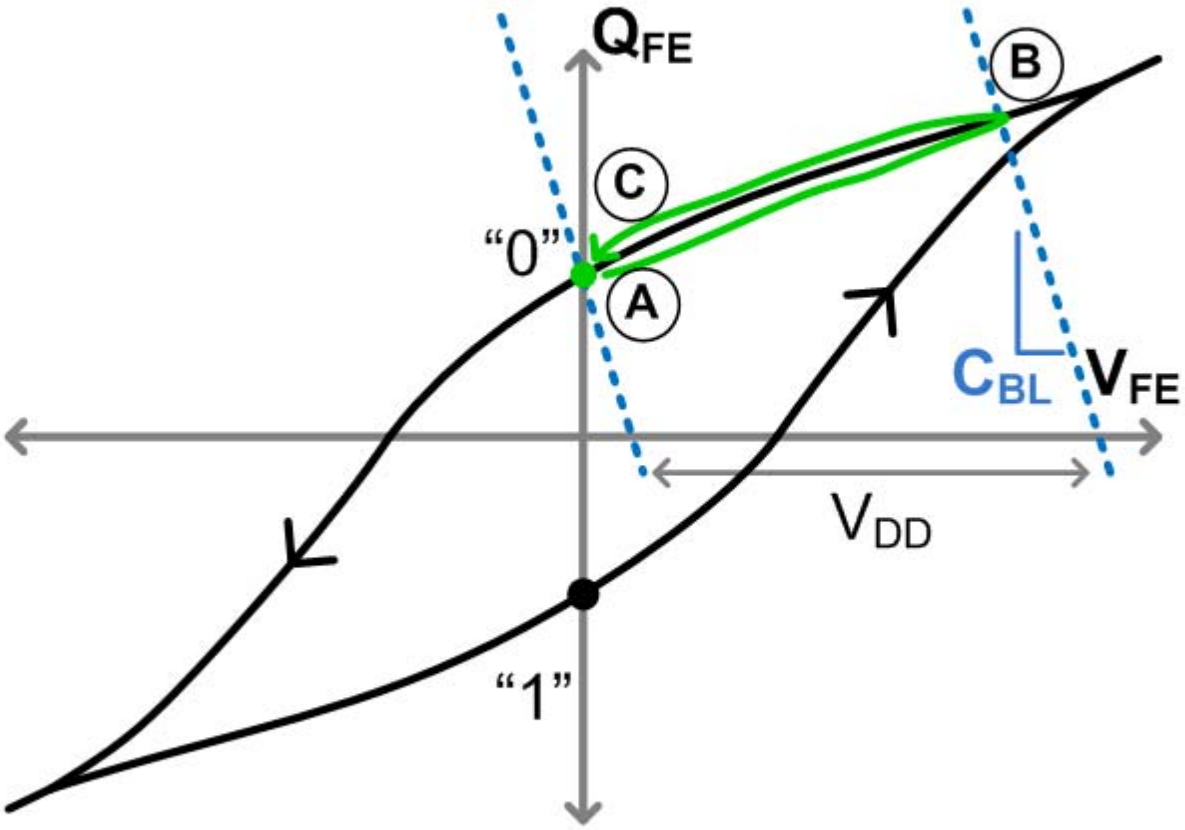


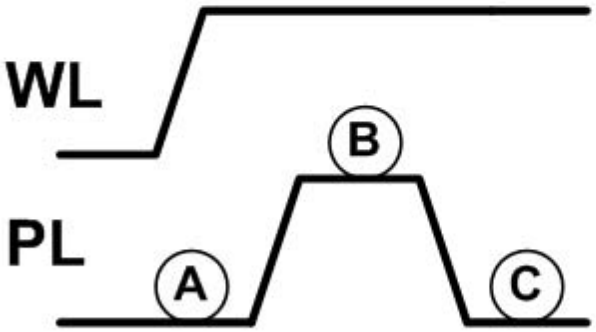
Extracts remnant charge onto floating bitline capacitance

Non-volatile Ferroelectric Capacitor (FeCap)



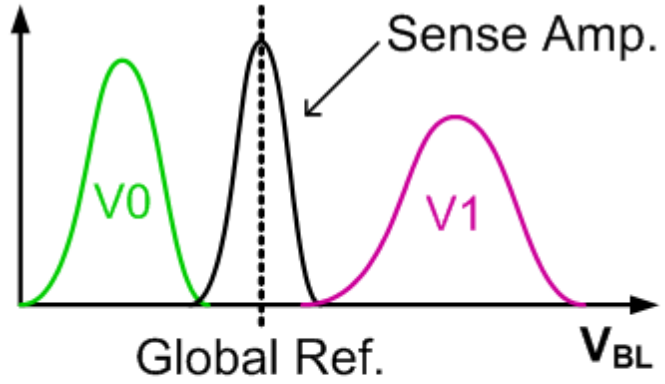
Read “0”

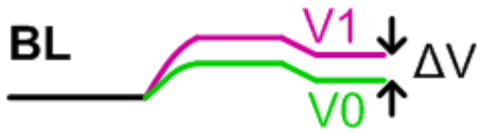


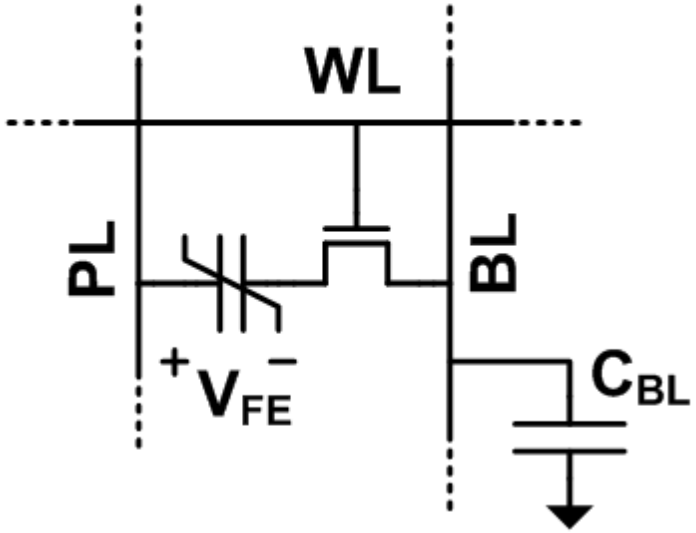


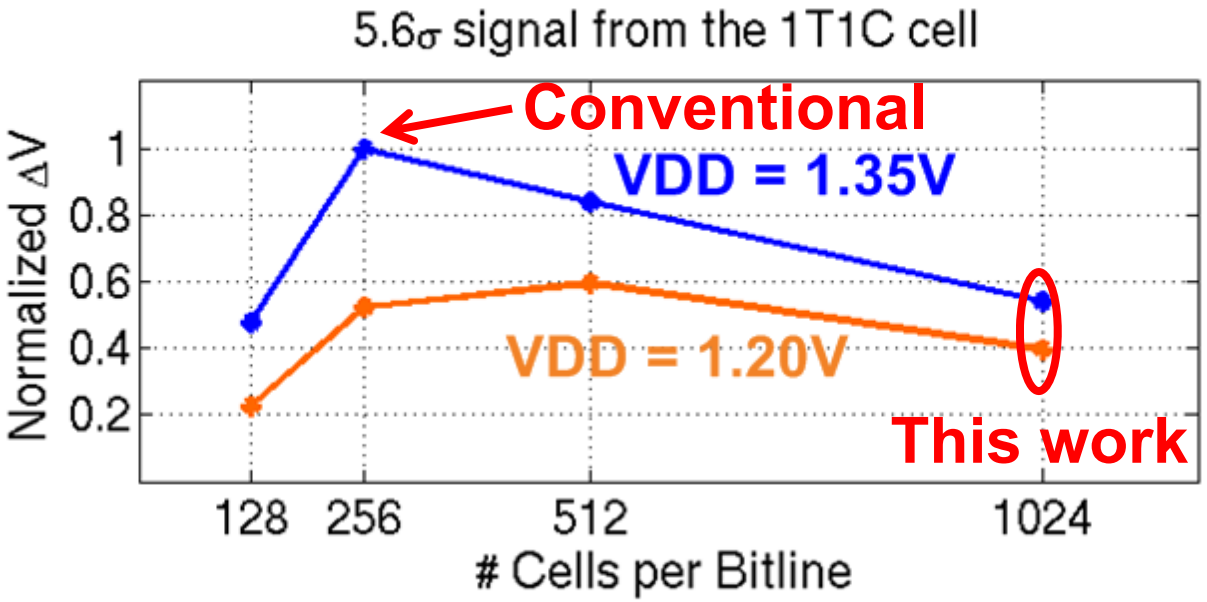
Traces non-hysteretic linear capacitance

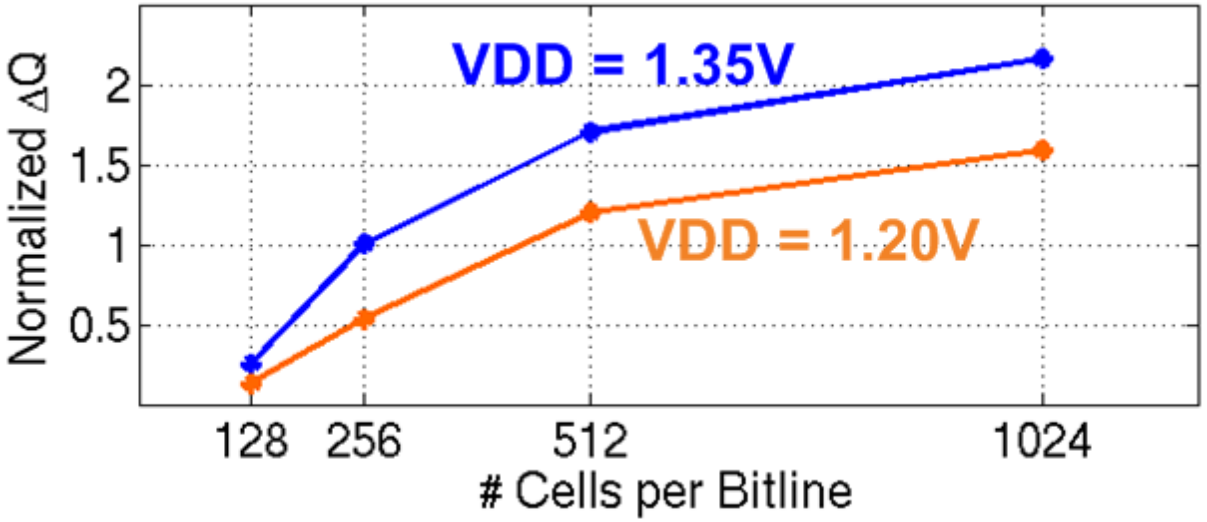
1T1C FeCap Cell Signal Characteristics



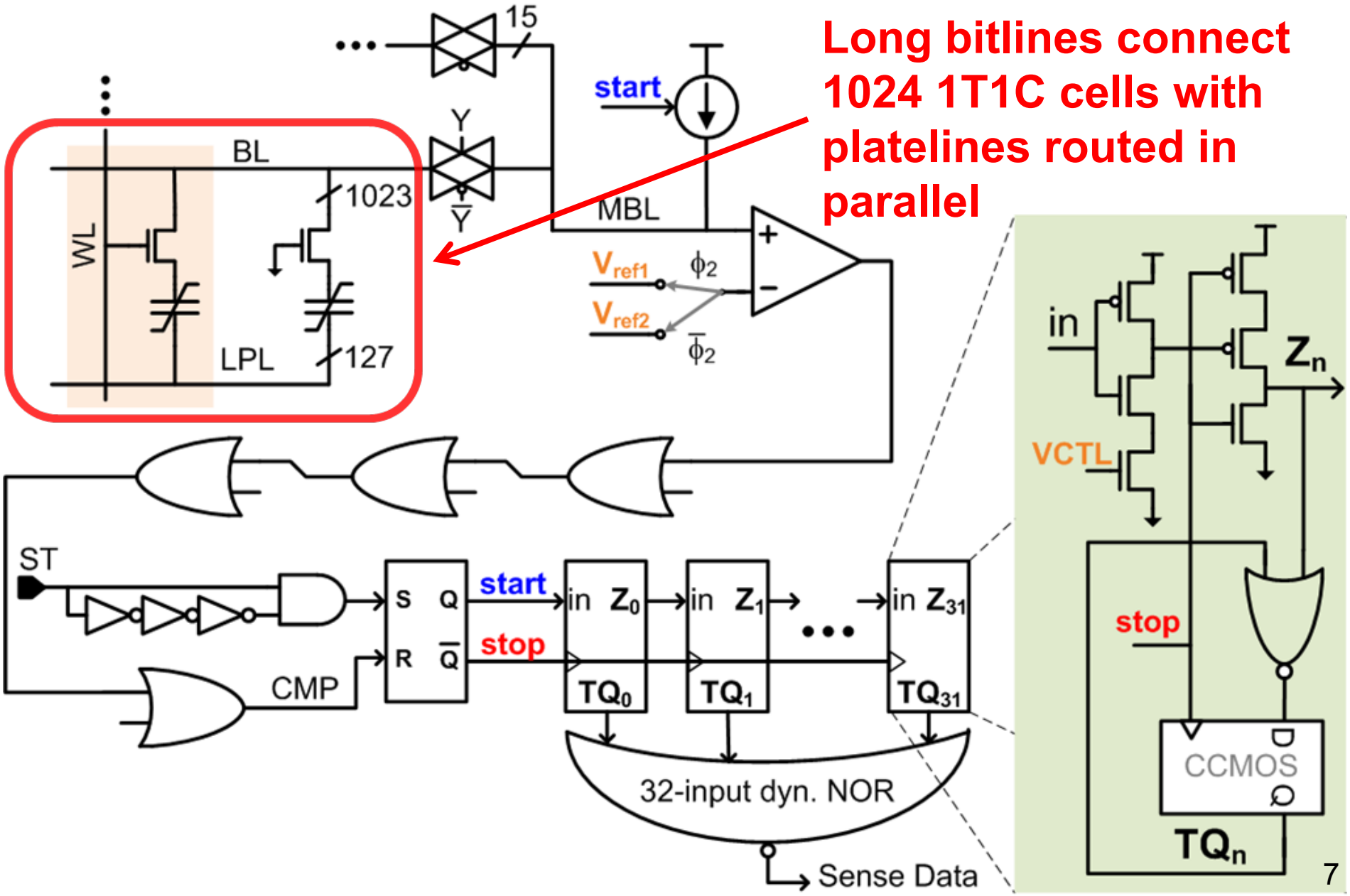




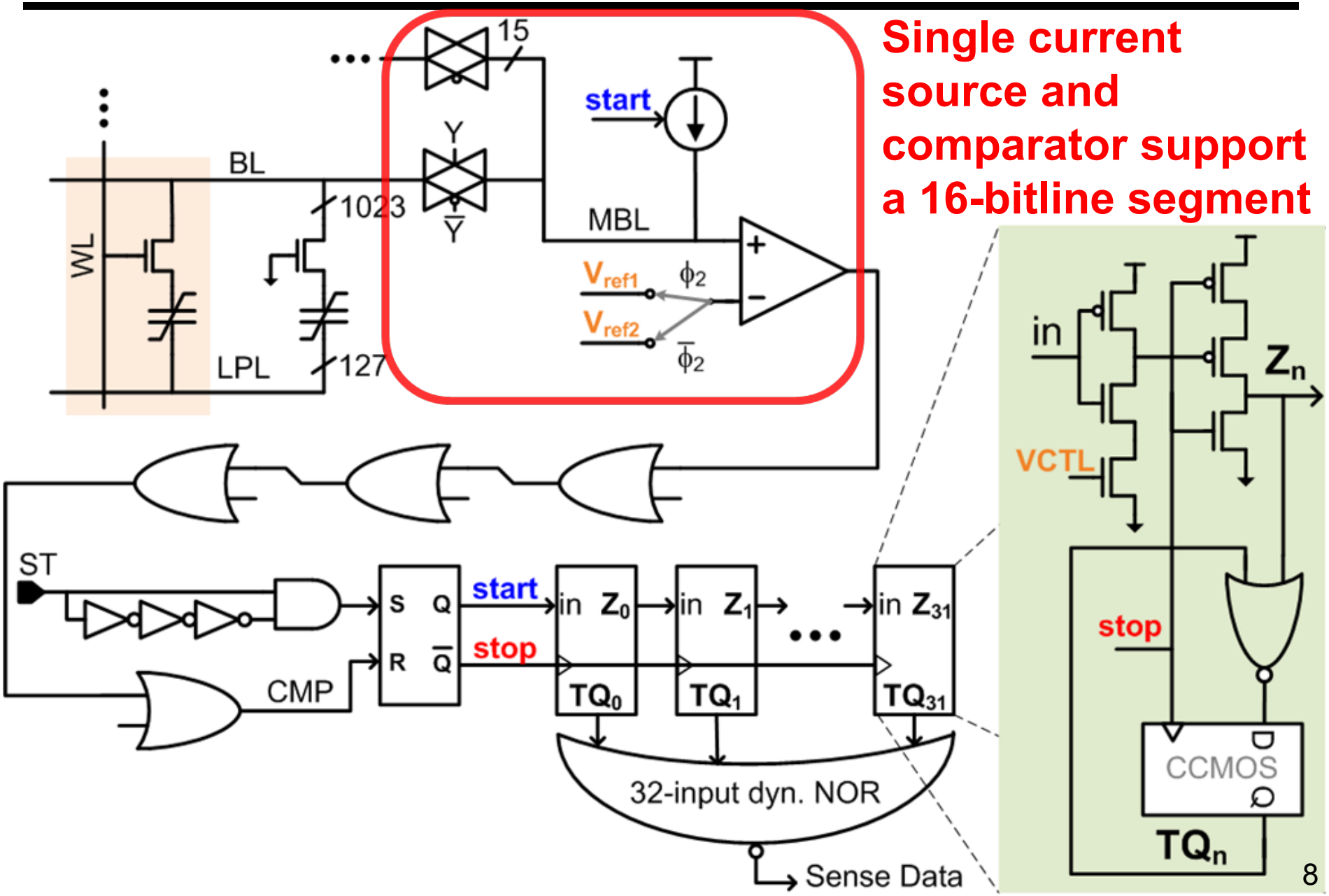




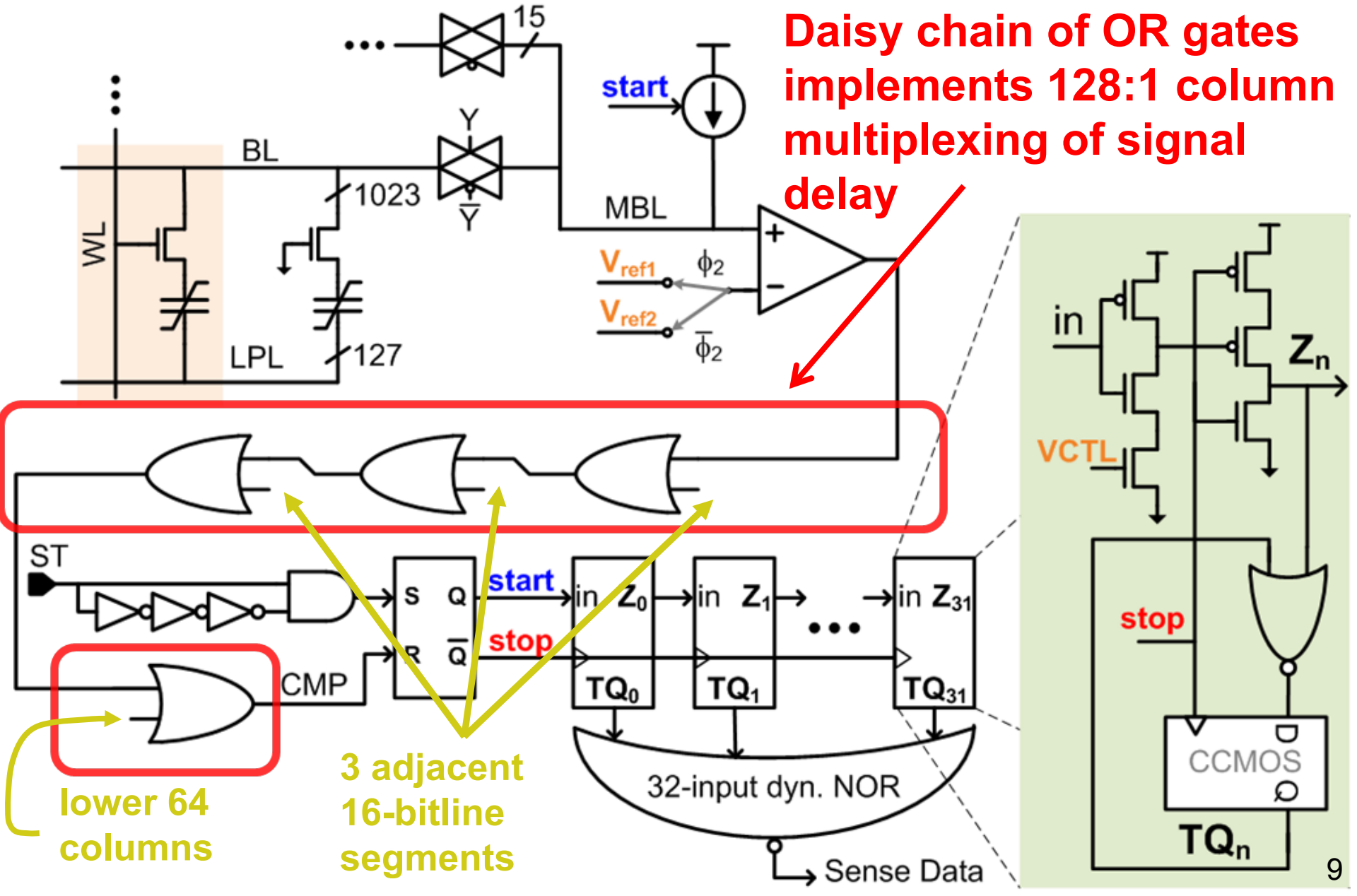
Simplified Schematic of TDC Read Path



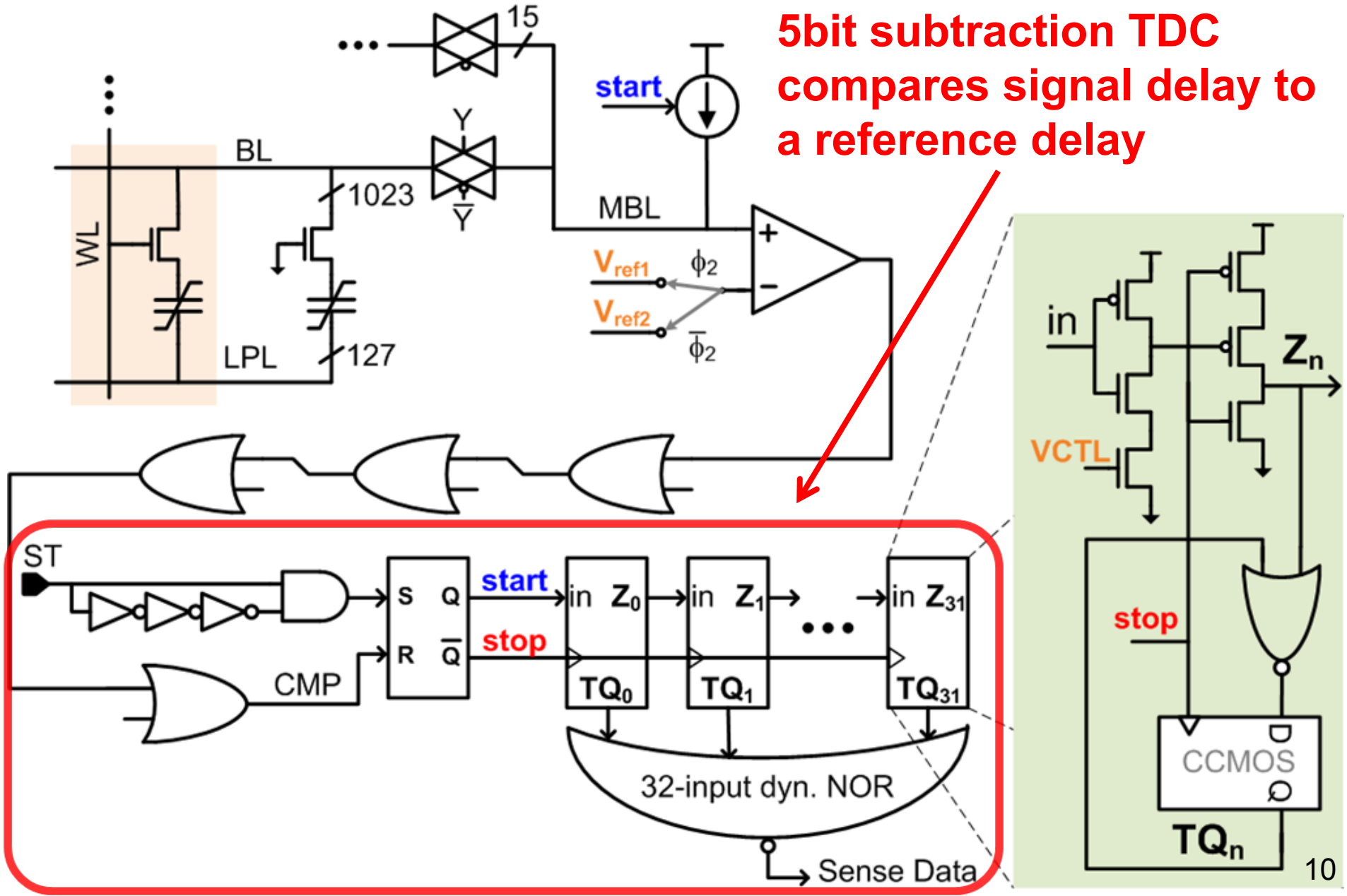
Simplified Schematic of TDC Read Path



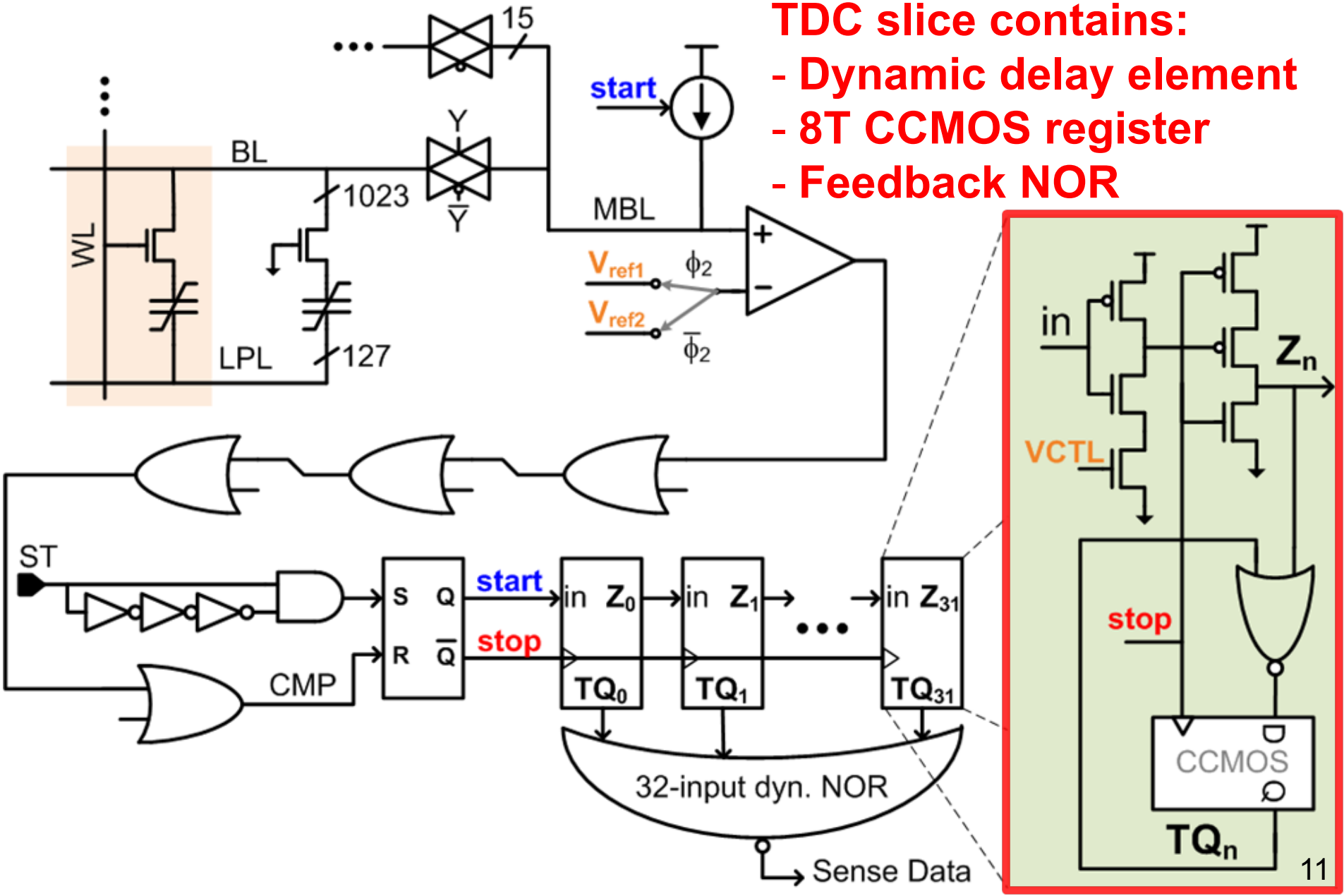
Simplified Schematic of TDC Read Path



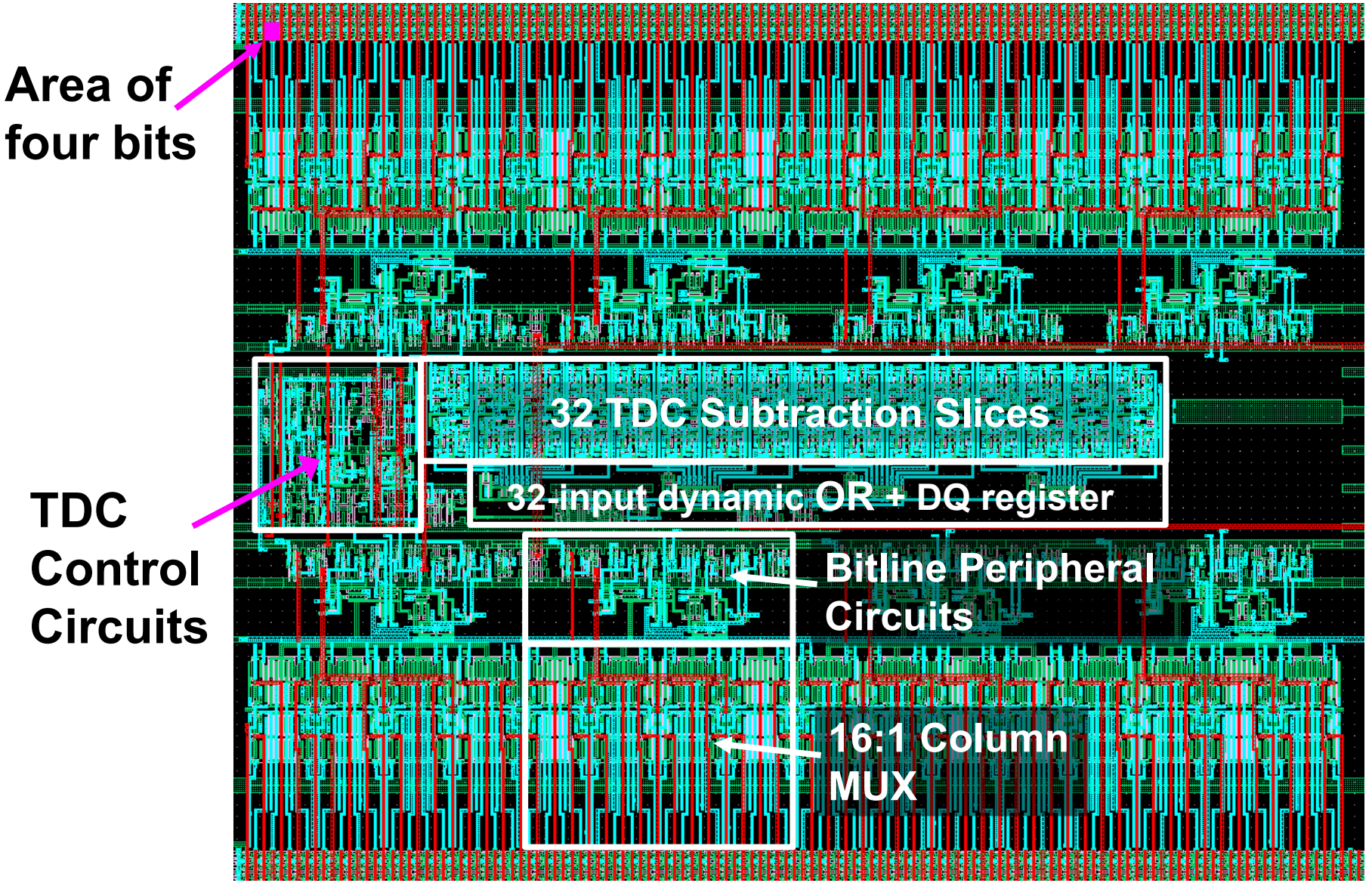
Simplified Schematic of TDC Read Path



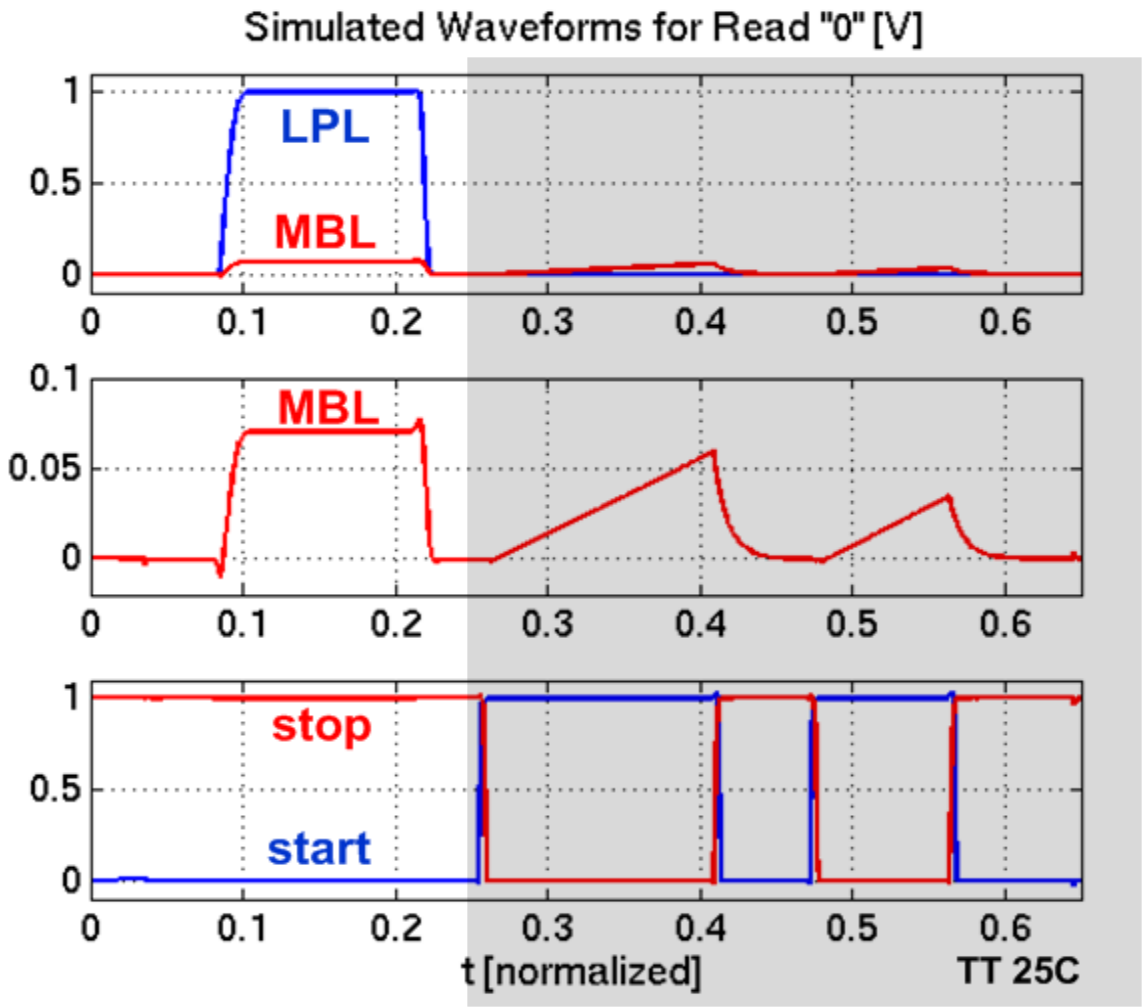
Simplified Schematic of TDC Read Path

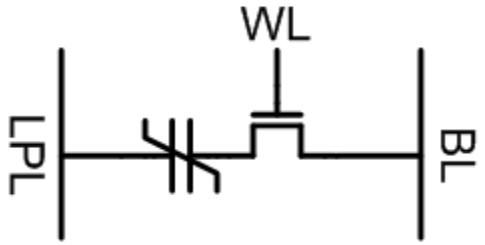


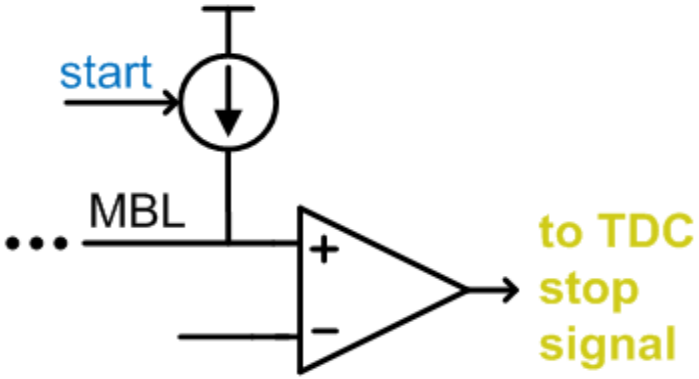
Implementation of Time-to-Digital Sensing

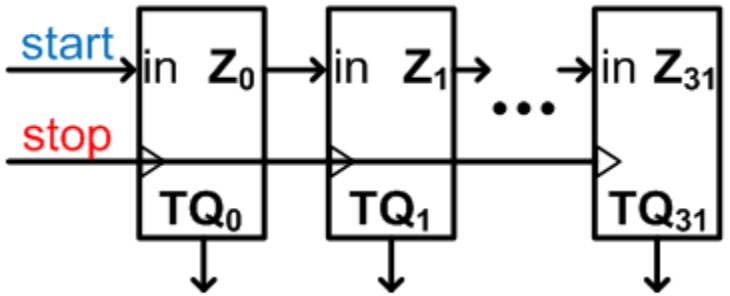


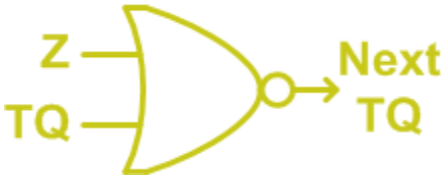
Time-to-Digital Sensing: Read 0







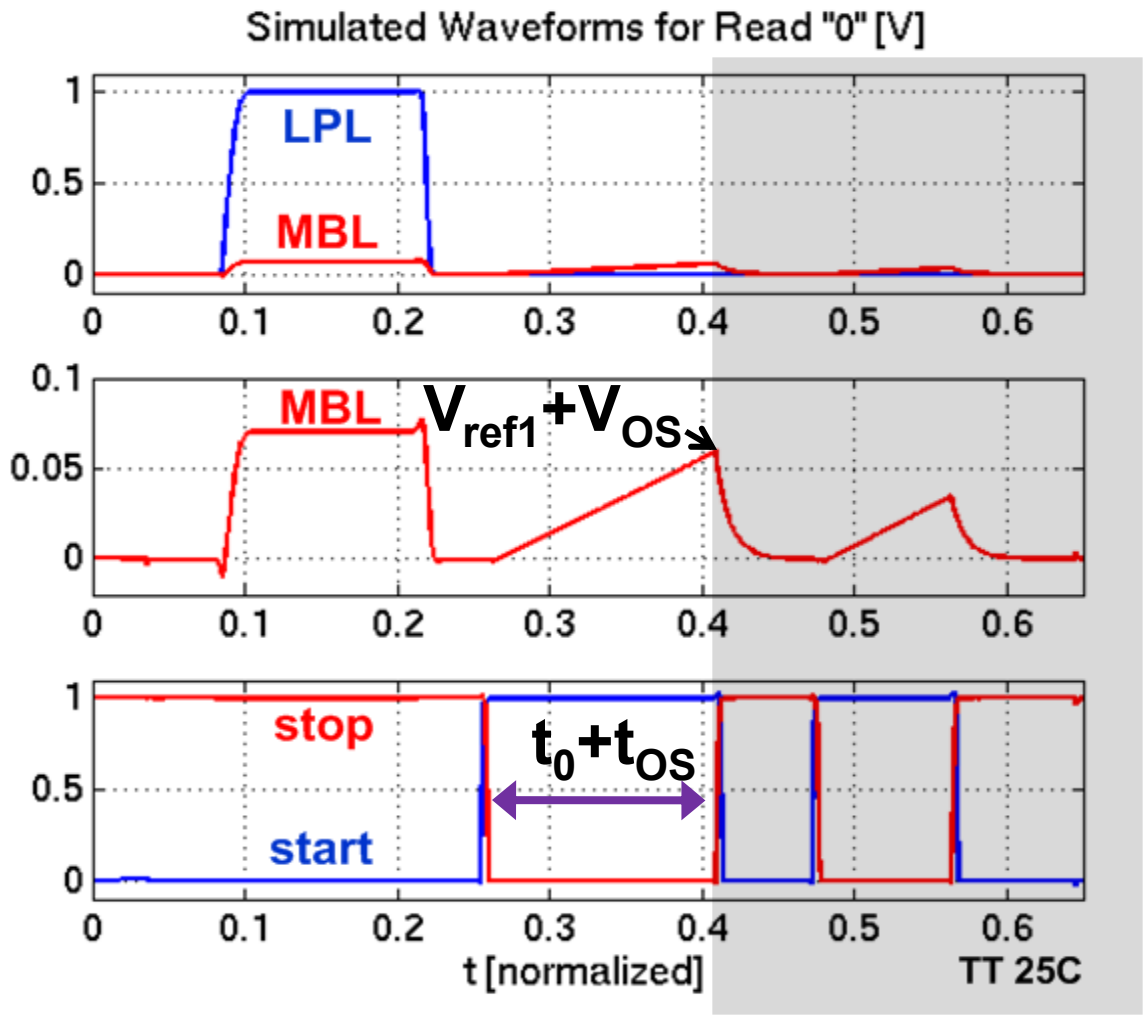


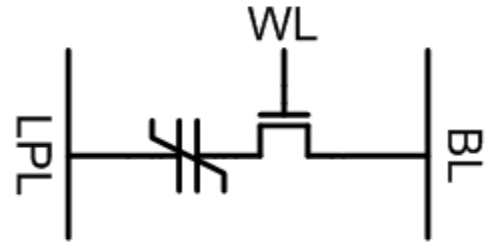


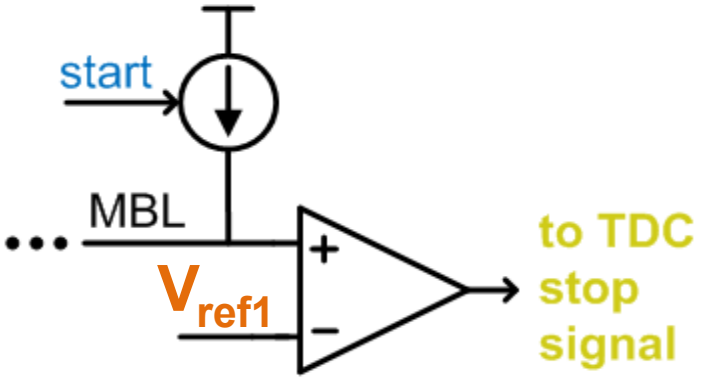
Z[0:31]: 00000000000000000000000000000000

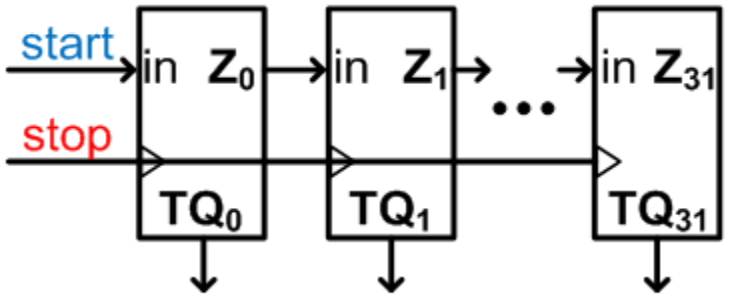
TQ[0:31]: 00000000000000000000000000000000

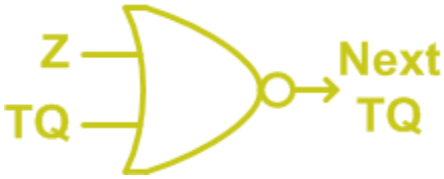
Time-to-Digital Sensing: Read 0









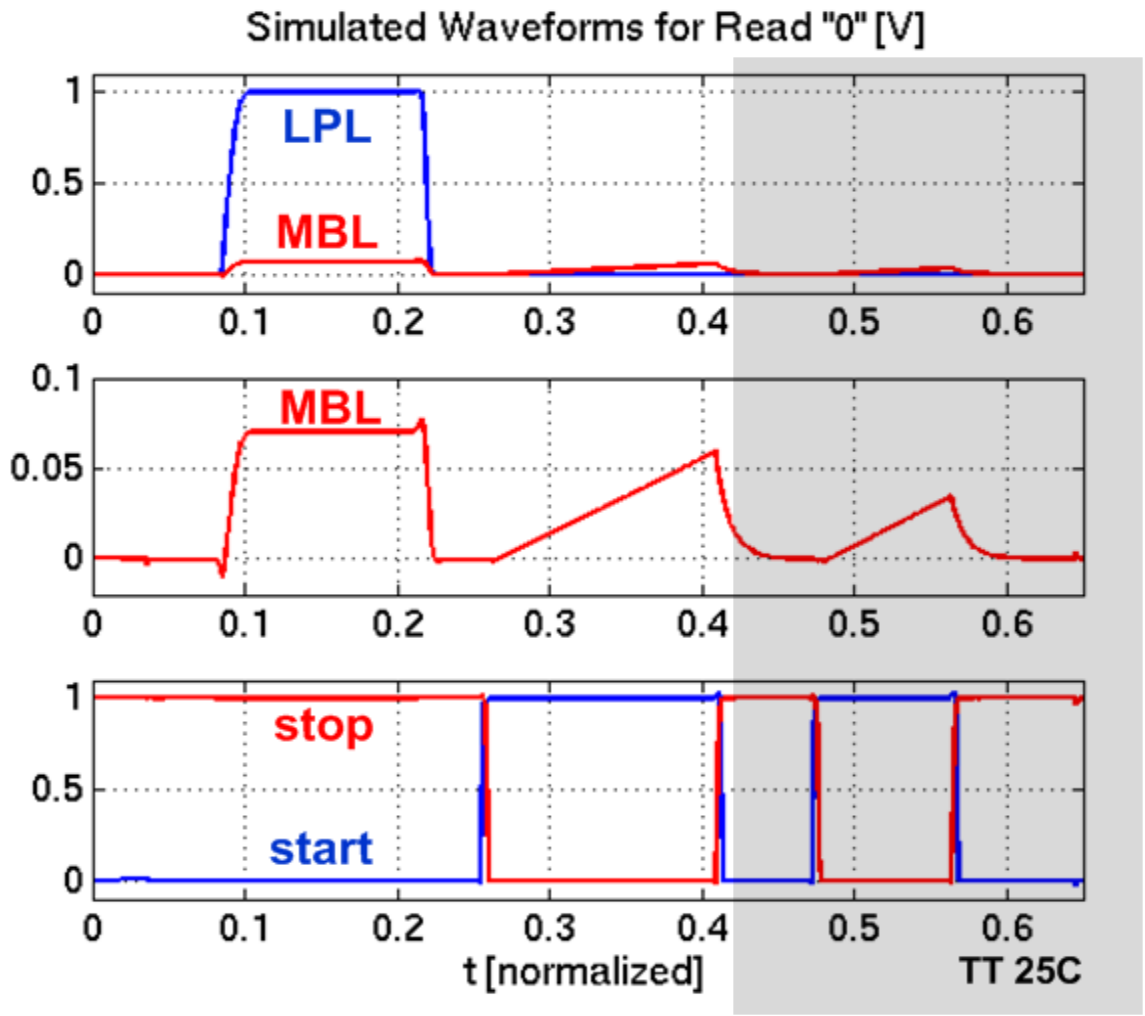


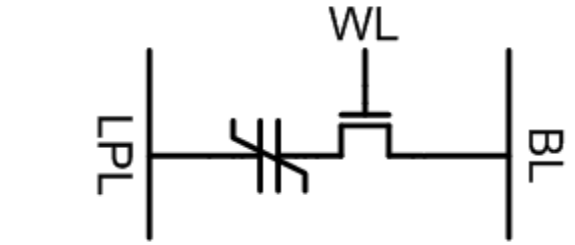
Z[0:31]: 11111111111111111111111111000000

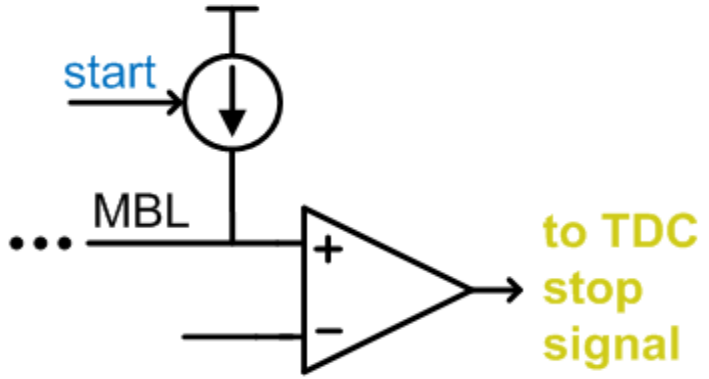
TQ[0:31]: 00000000000000000000000000000000

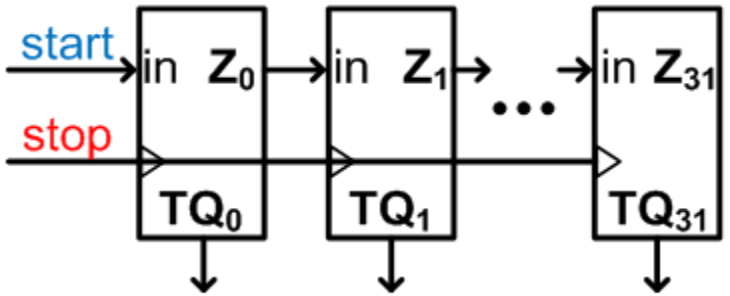
t_0+t_{OS}

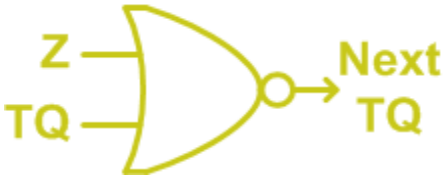
Time-to-Digital Sensing: Read 0









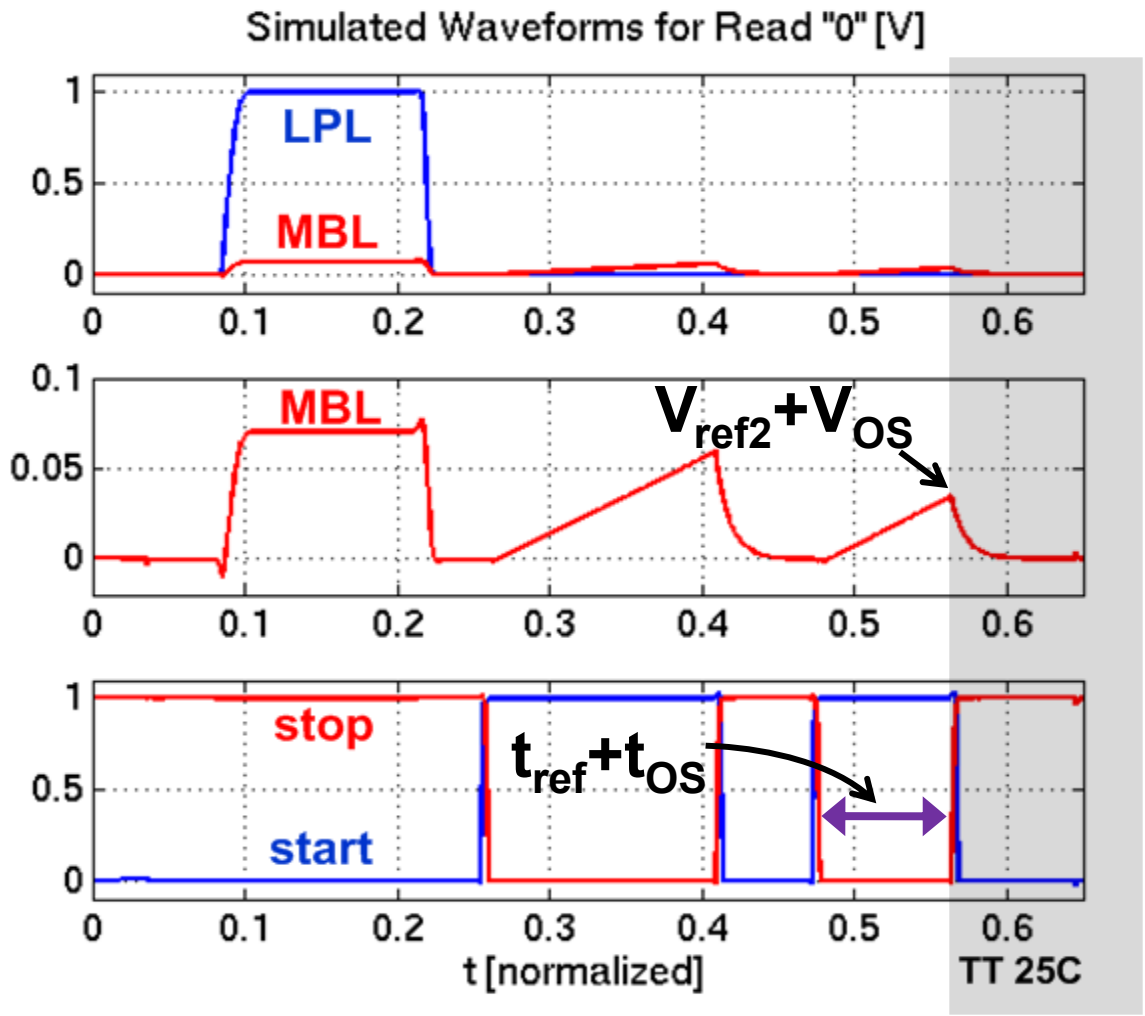


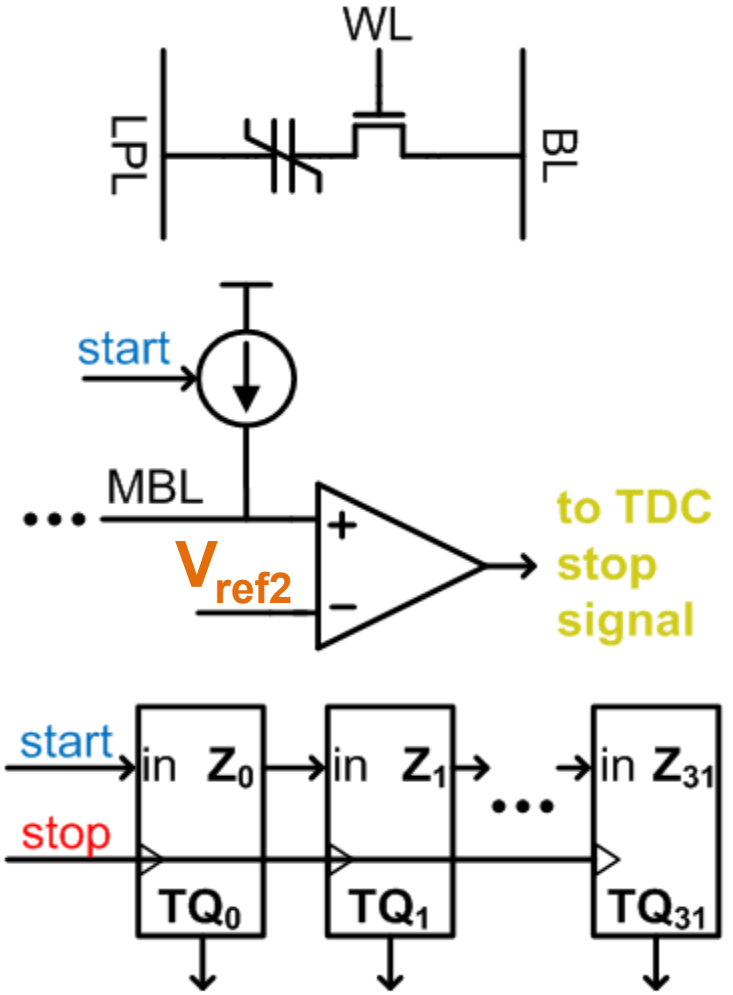
Z[0:31]: 00000000000000000000000000000000

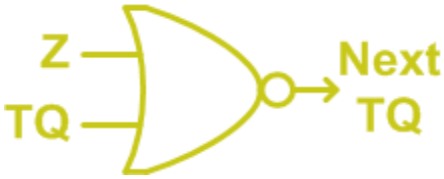
TQ[0:31]: 00000000000000000000000000111111

t_0+t_{OS}

Time-to-Digital Sensing: Read 0





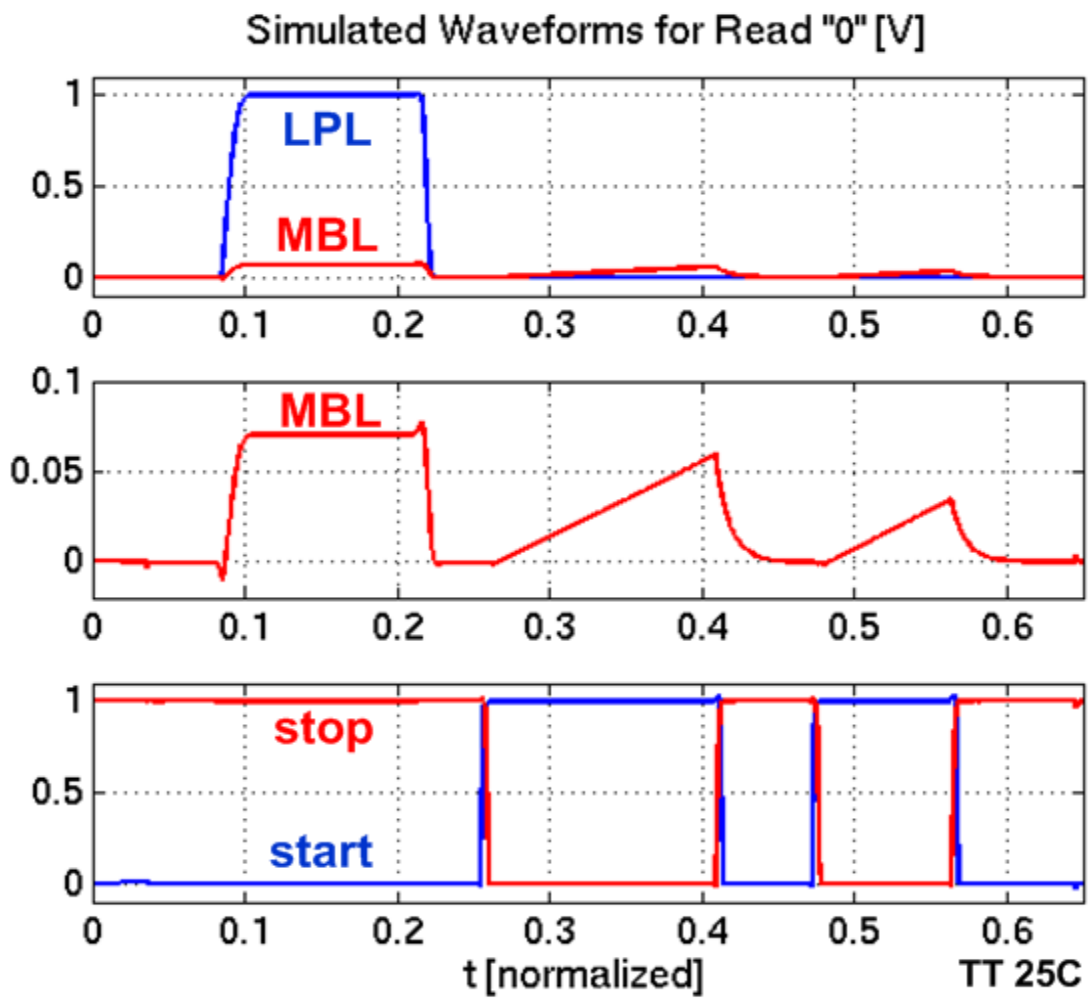


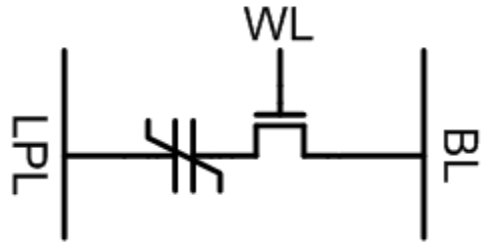
Z[0:31]: 11111111111111100000000000000000

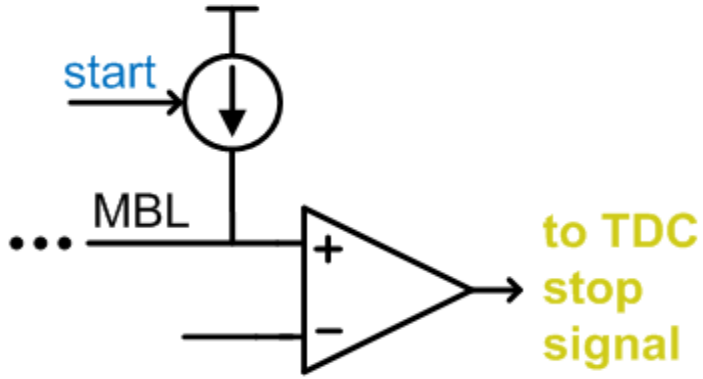
TQ[0:31]: 00000000000000001111111111111111

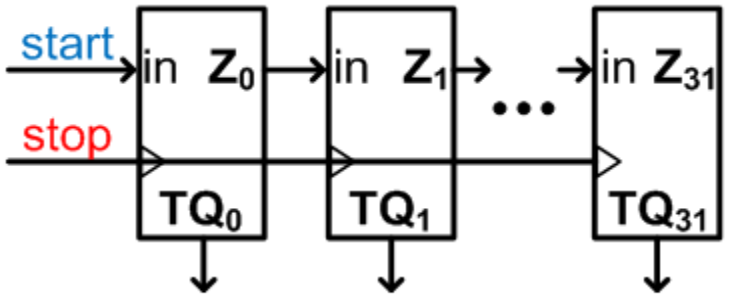
$t_{ref}+t_{OS}$ → t_0+t_{OS} →

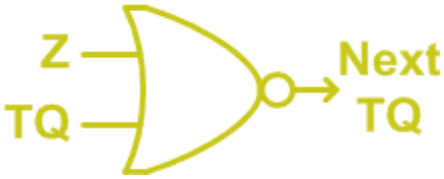
Time-to-Digital Sensing: Read 0









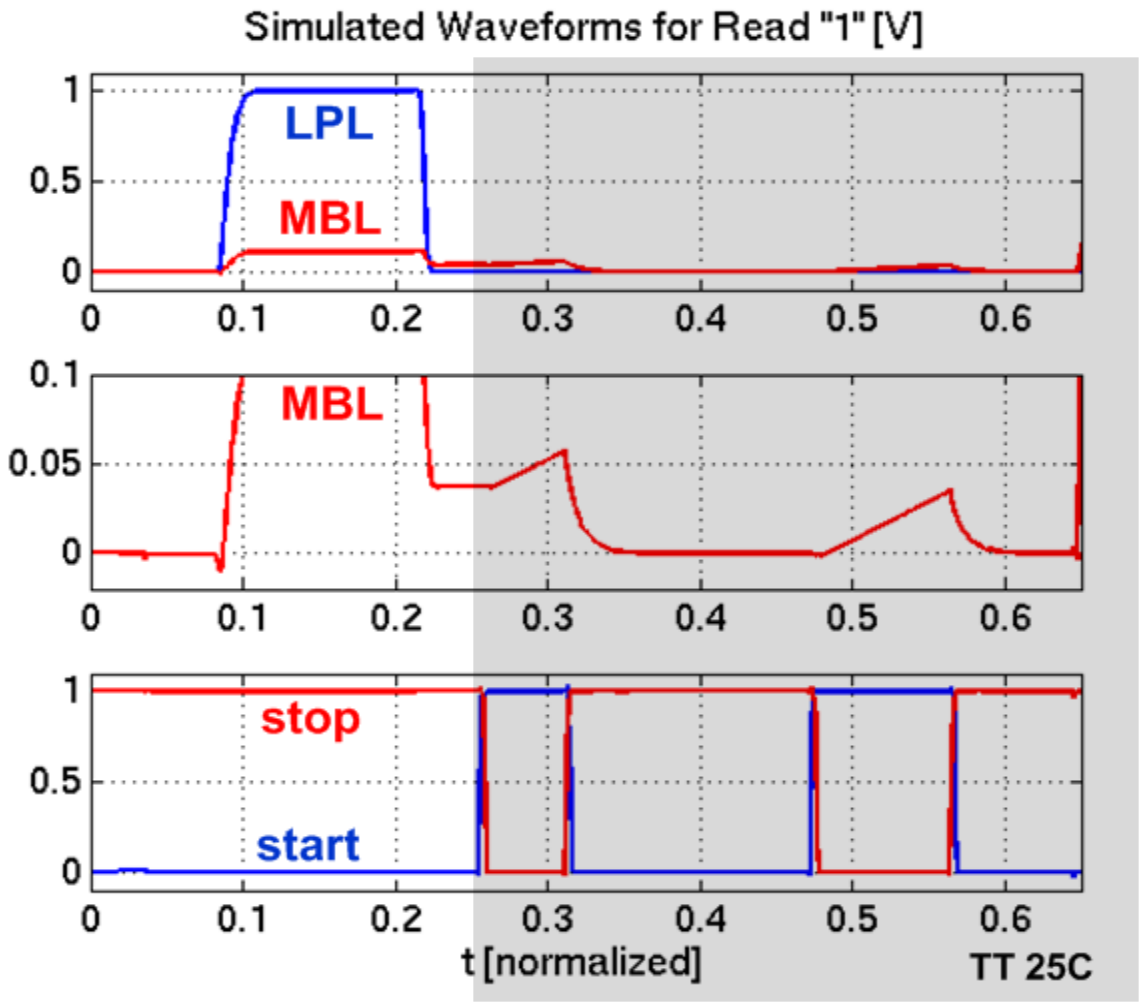


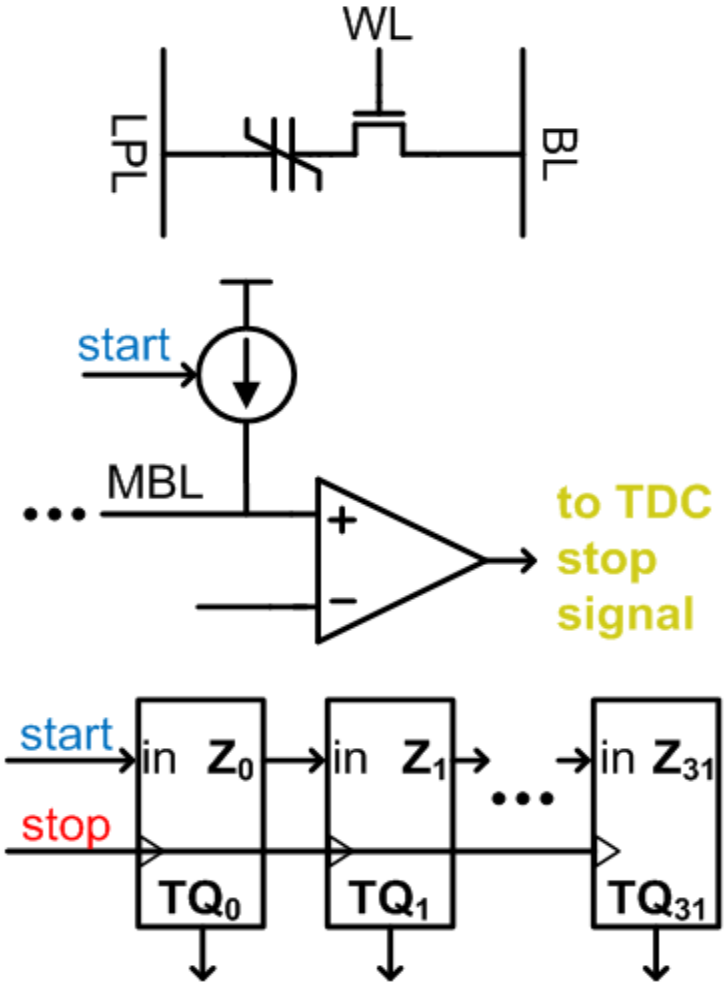
Z[0:31]: 00000000000000000000000000000000

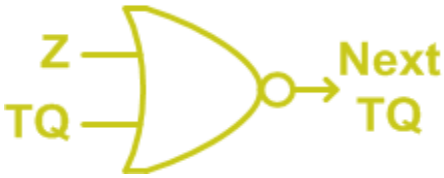
TQ[0:31]: 00000000000000001111111110000000

$t_0 - t_{ref} > 0$

Time-to-Digital Sensing: Read 1



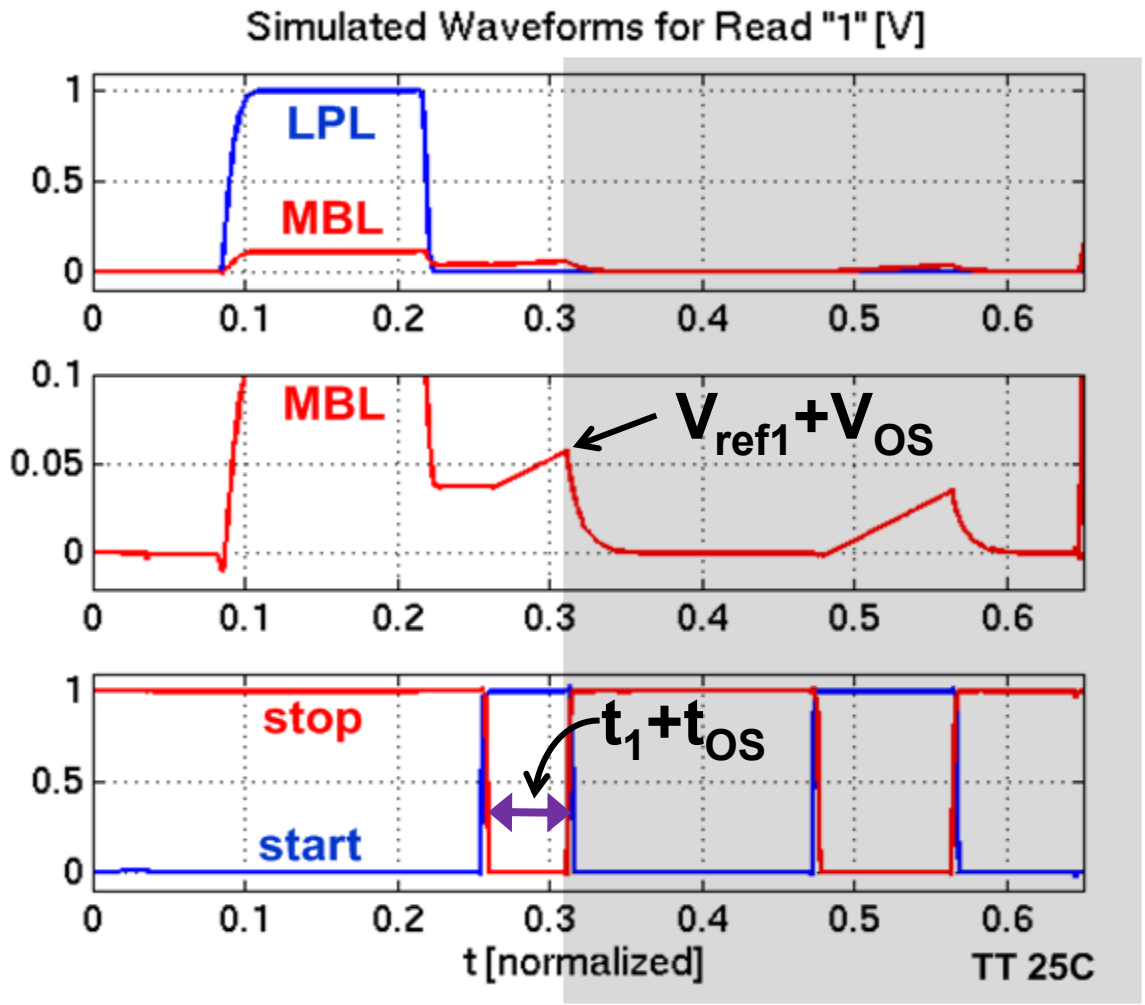


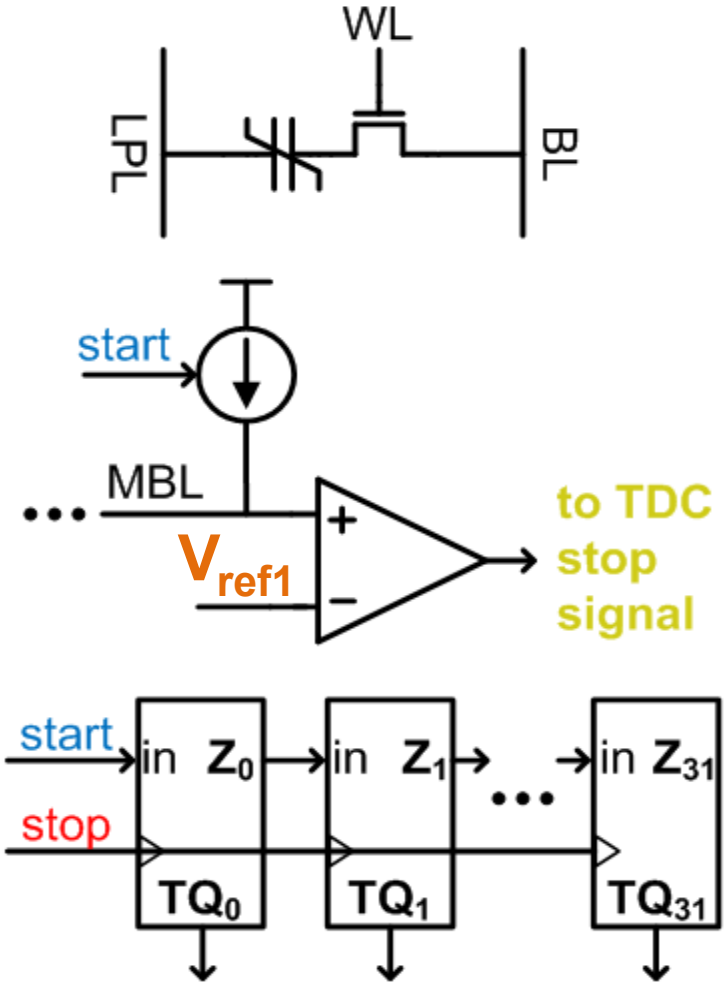


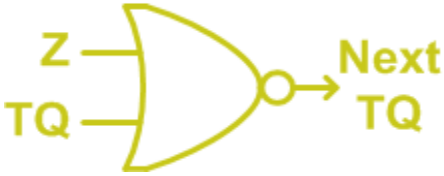
Z[0:31]: 00000000000000000000000000000000

TQ[0:31]: 00000000000000000000000000000000

Time-to-Digital Sensing: Read 1





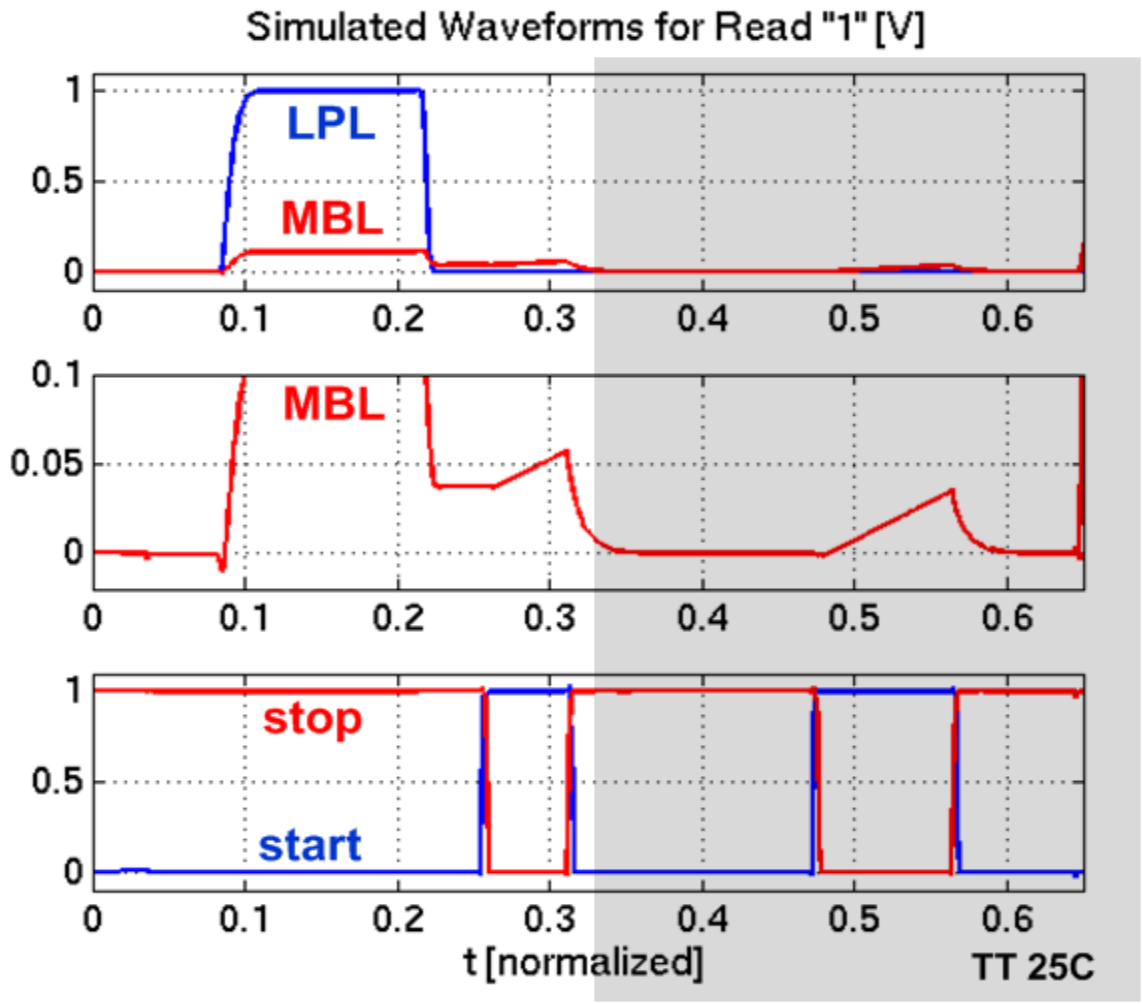


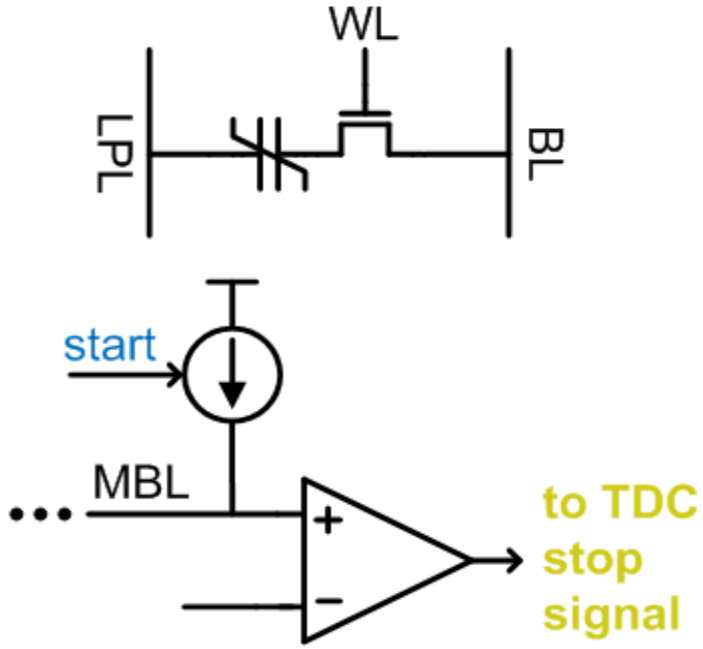
Z[0:31]: 11111111000000000000000000000000

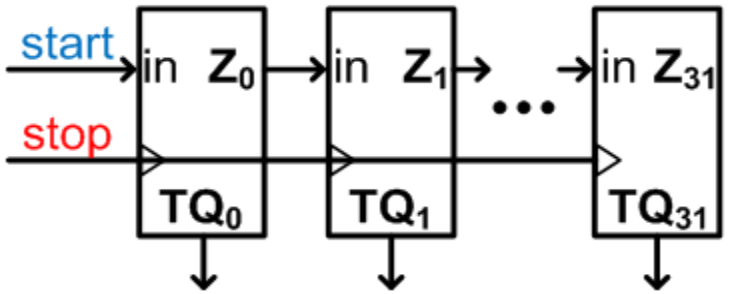
TQ[0:31]: 00000000000000000000000000000000

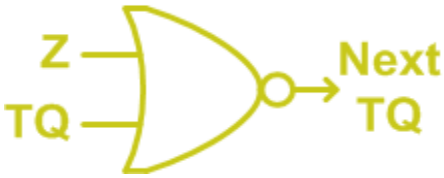
t_1+t_{OS}

Time-to-Digital Sensing: Read 1







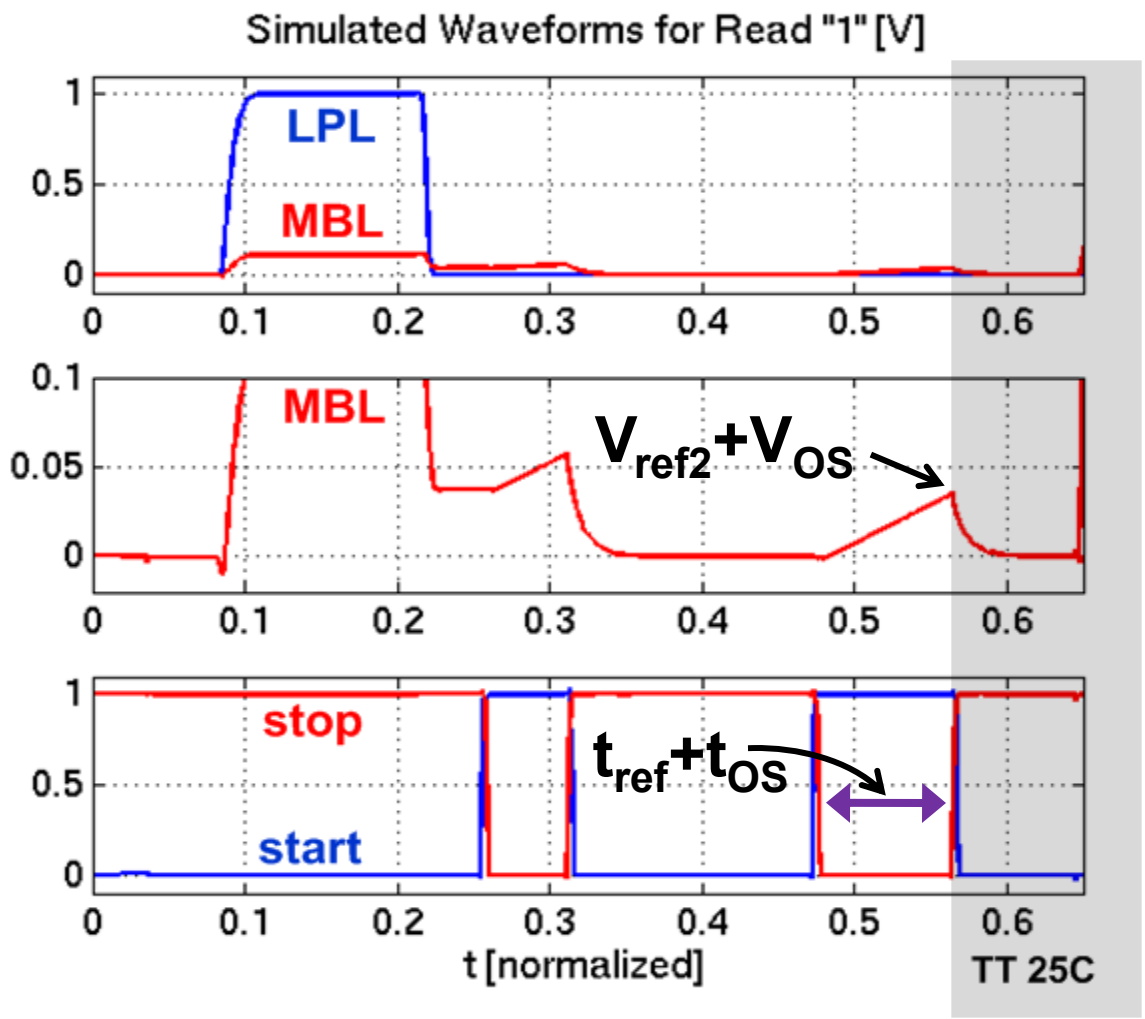


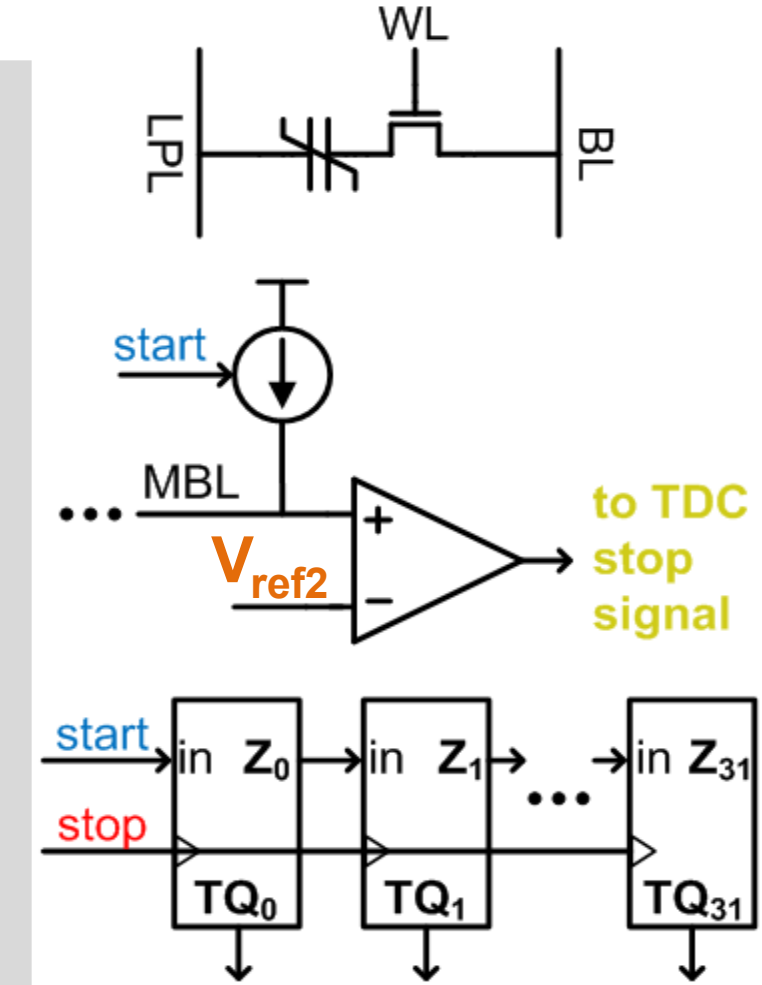
Z[0:31]: 00000000000000000000000000000000

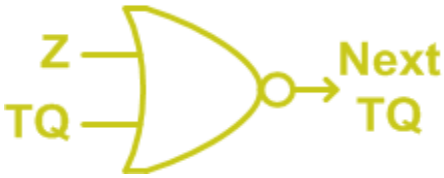
TQ[0:31]: 00000000111111111111111111111111

t_1+t_{OS}

Time-to-Digital Sensing: Read 1





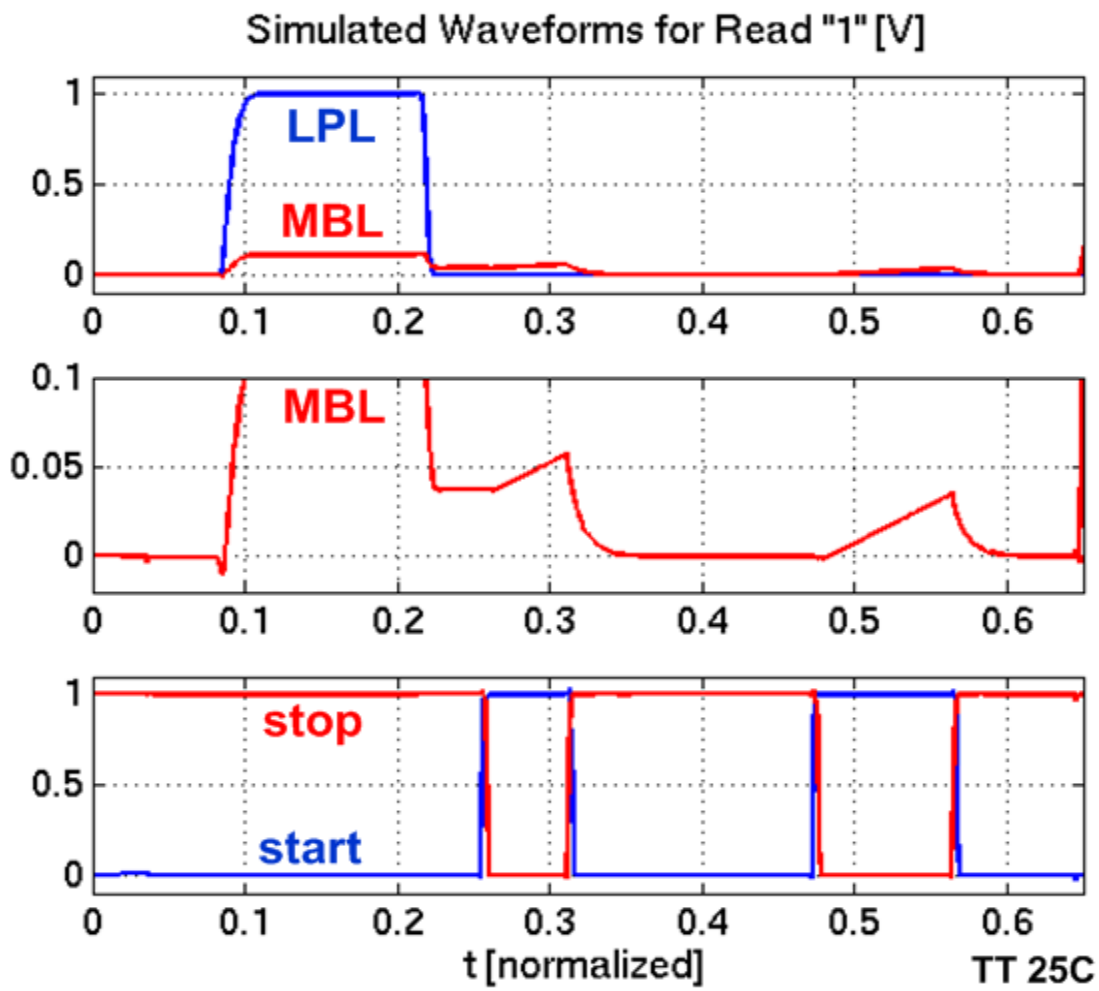


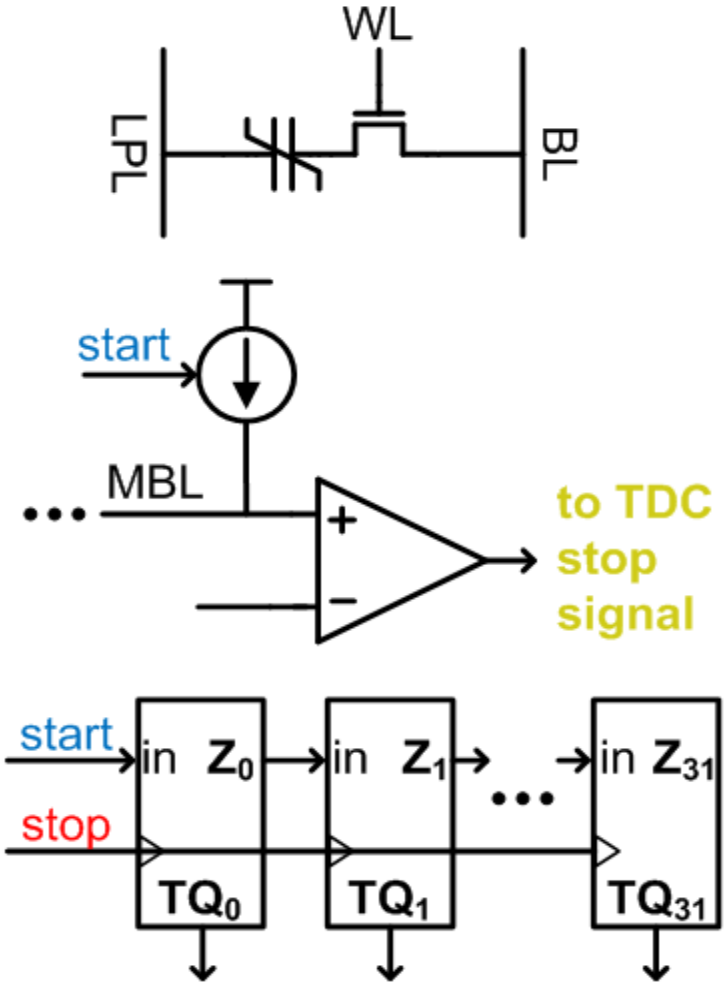
Z[0:31]: 11111111111111110000000000000000

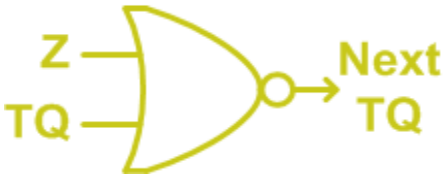
TQ[0:31]: 00000000111111111111111111111111

t_1+t_{OS} → $t_{ref}+t_{OS}$ →

Time-to-Digital Sensing: Read 1





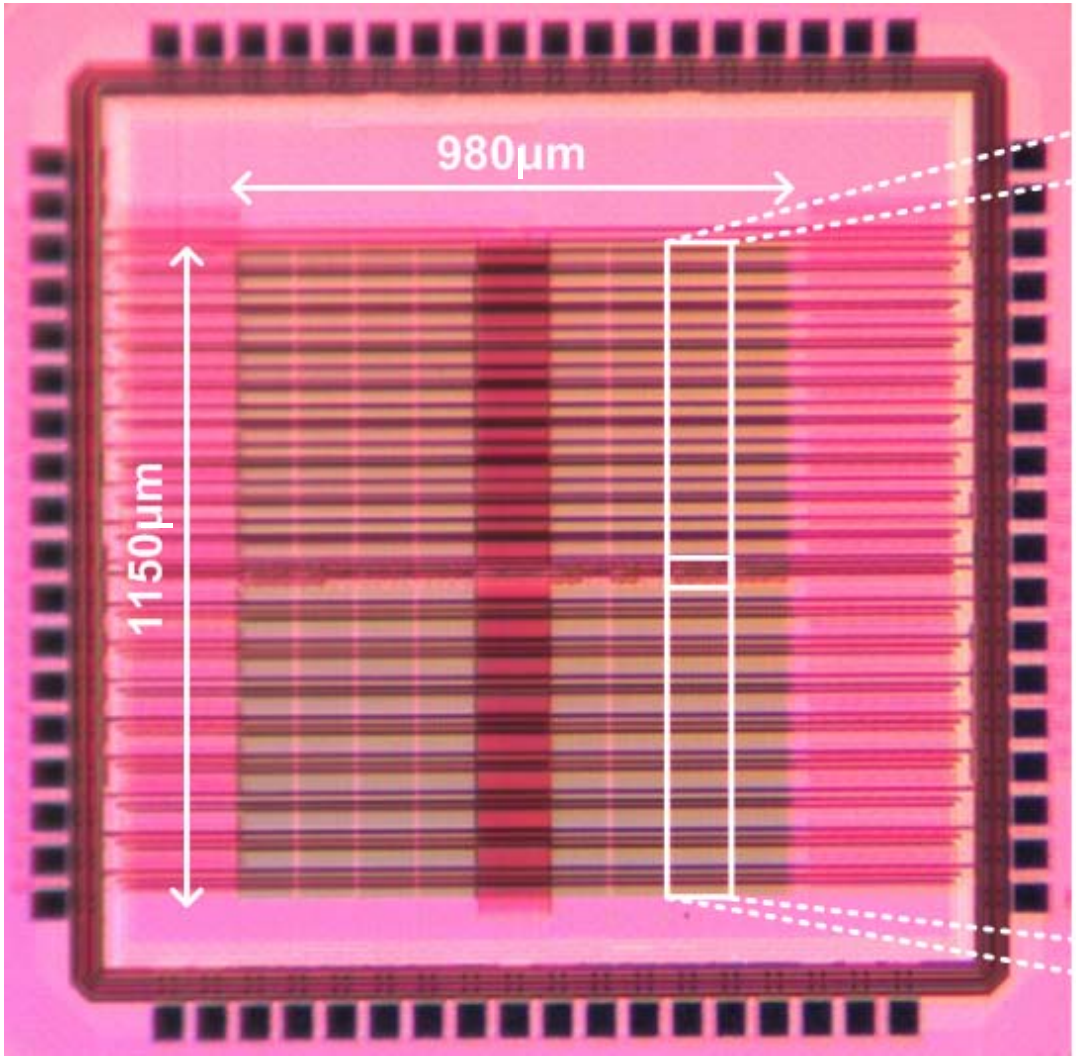


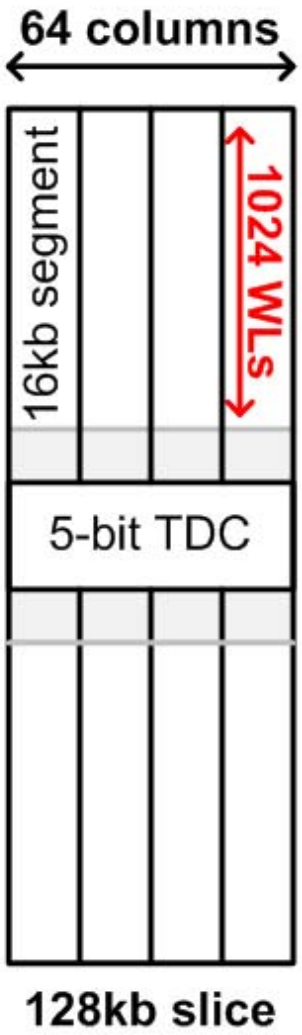
Z[0:31]: 00000000000000000000000000000000

TQ[0:31]: 00000000000000000000000000000000

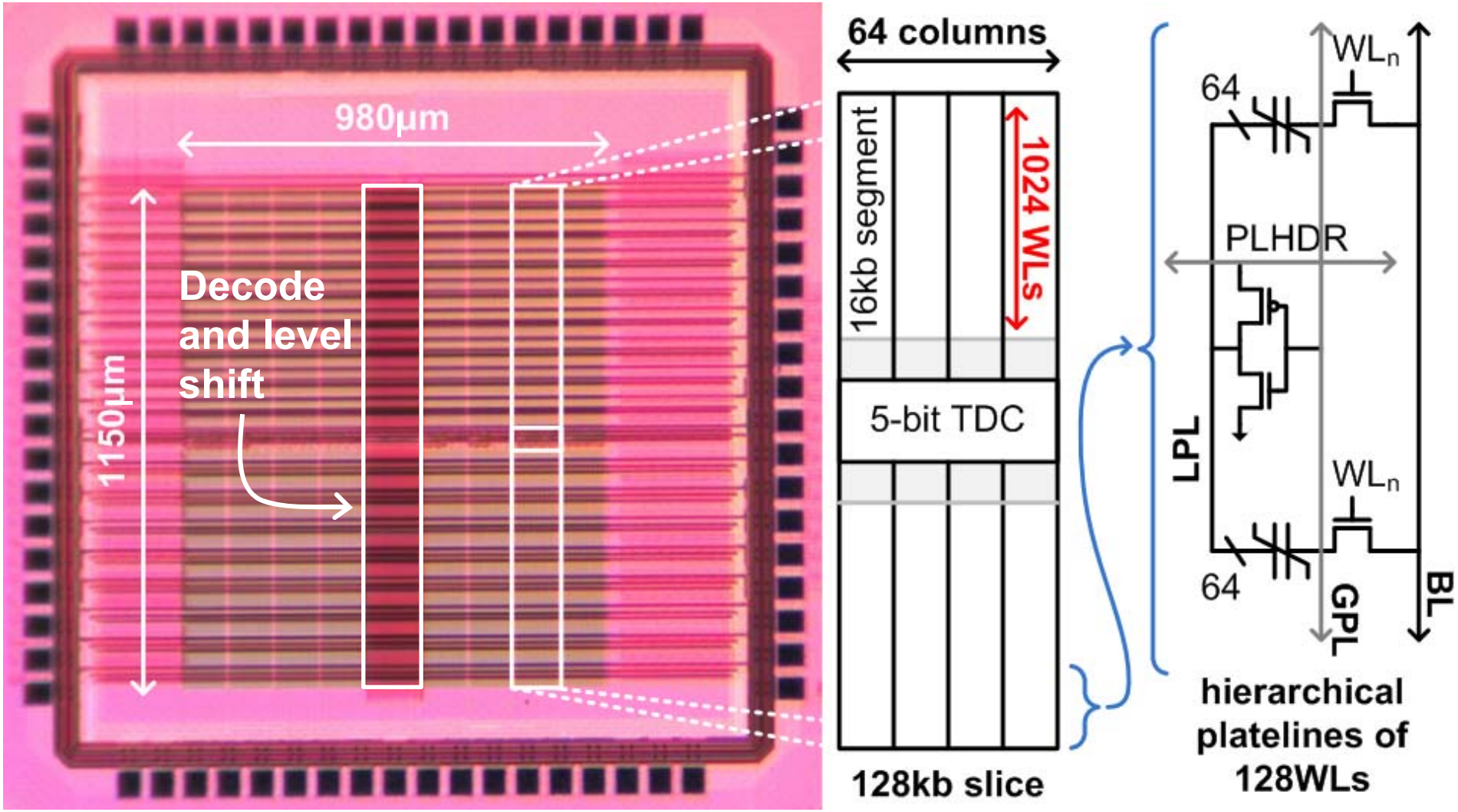
$t_1 - t_{ref} < 0$

1Mb FeRAM Prototype Architecture

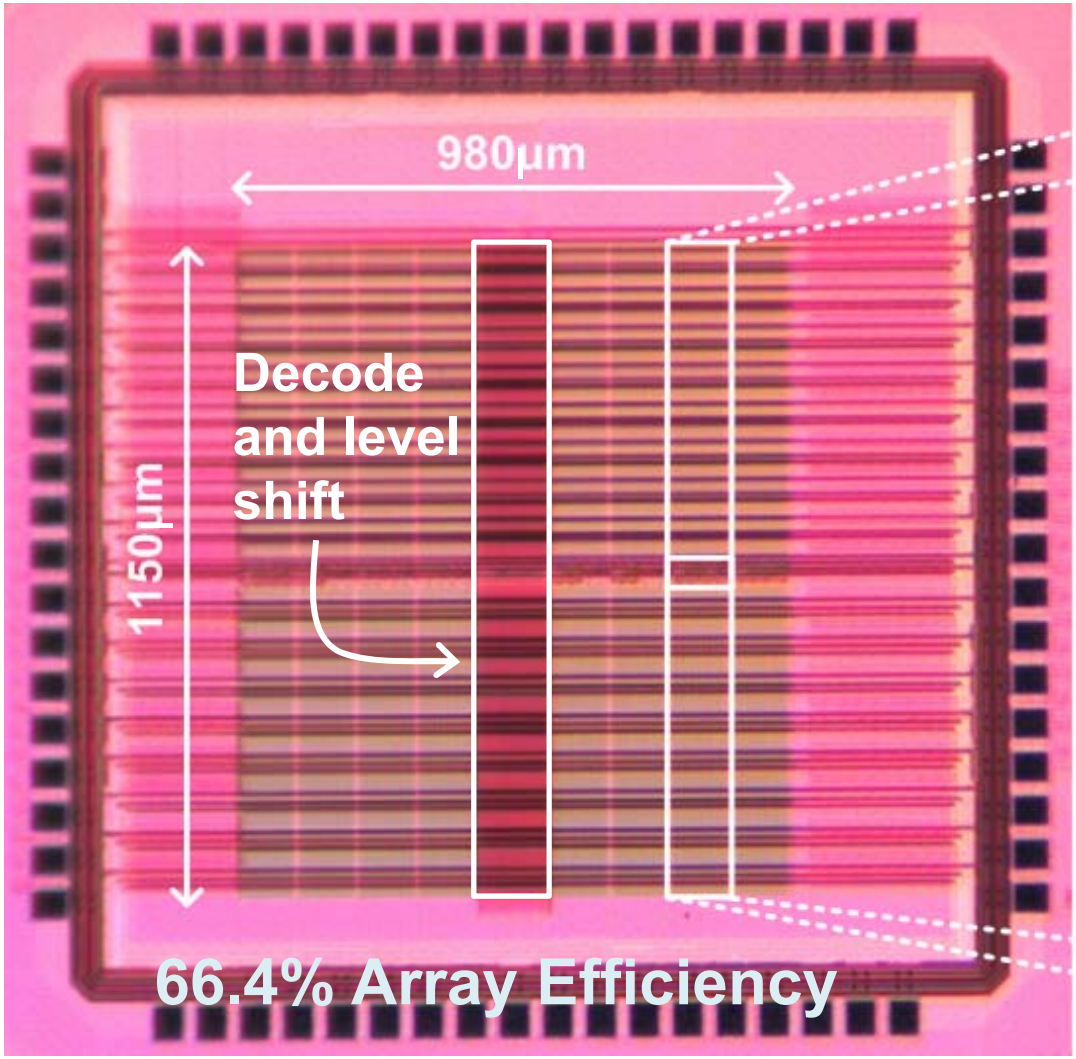


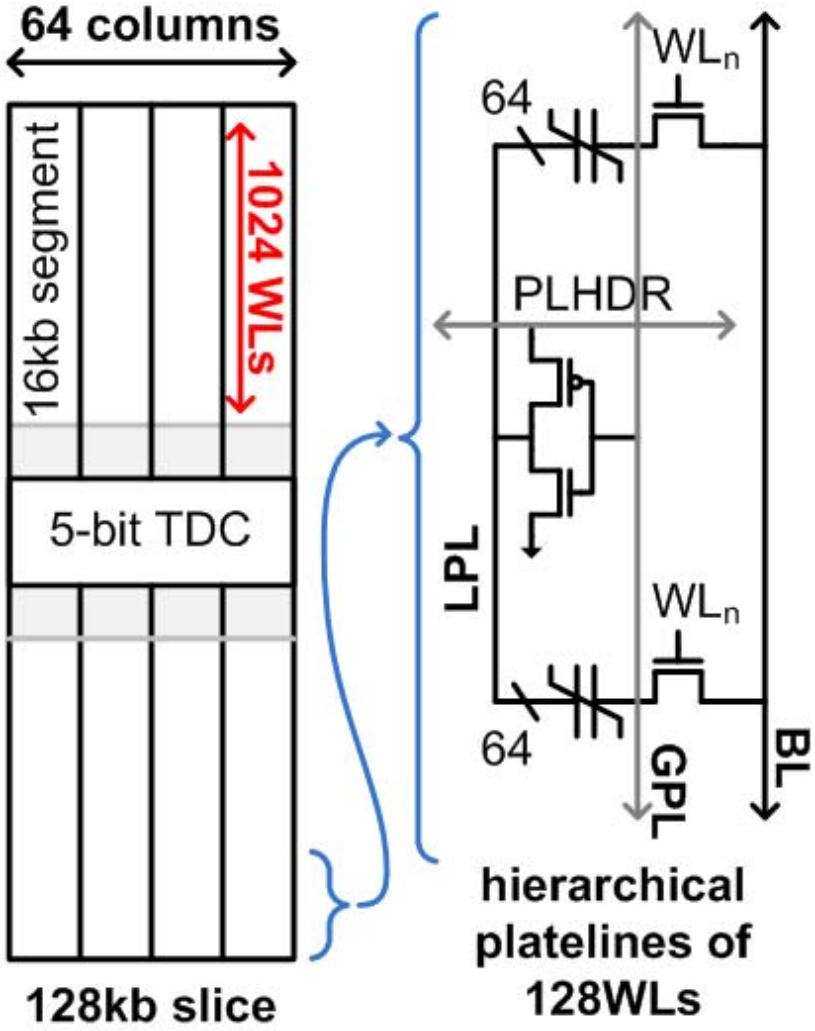


1Mb FeRAM Prototype Architecture



1Mb FeRAM Prototype Architecture





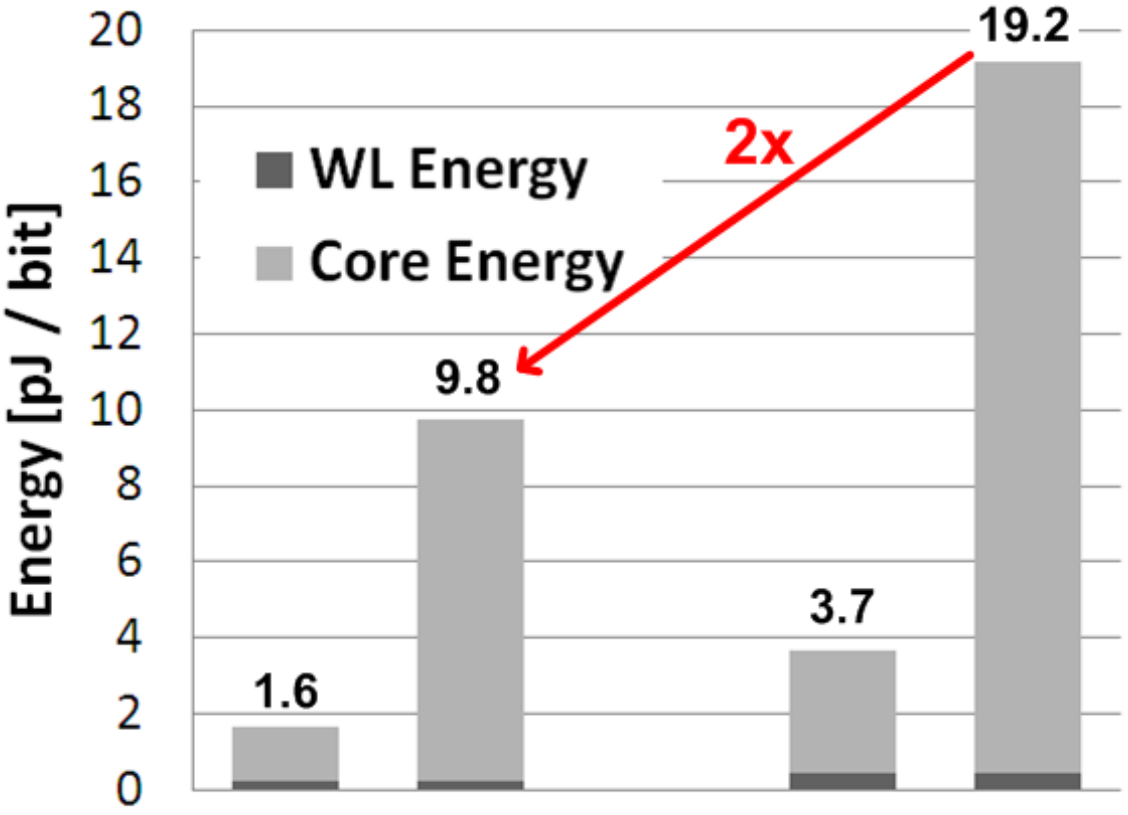
2^{20} 1T1C cells multiplex to eight 110µm^2 5bit TDCs

Measurement of Energy Scaling

Exploration of references and timings with:

- Alternating checkerboard patterns
- 30 min. power-down between write and read (VDD shorted to GND)

Measurement points correspond to zero fails in 1Mb chip.



	Write	Read	Write	Read
VDD	1.0V	1.0V	1.5V	1.5V
VWL	1.7V	1.7V	2.2V	2.2V
Read Cycle	728ns		199ns	

Significance of Time-to-digital Sensing

1. Area-efficient way to compensate analog offset with digital circuits
2. Such digital circuits scale in voltage, consume less static power, and improve with technology scaling.
3. Representing the signal as a delay better serves the essential multiplexing operation of a memory.

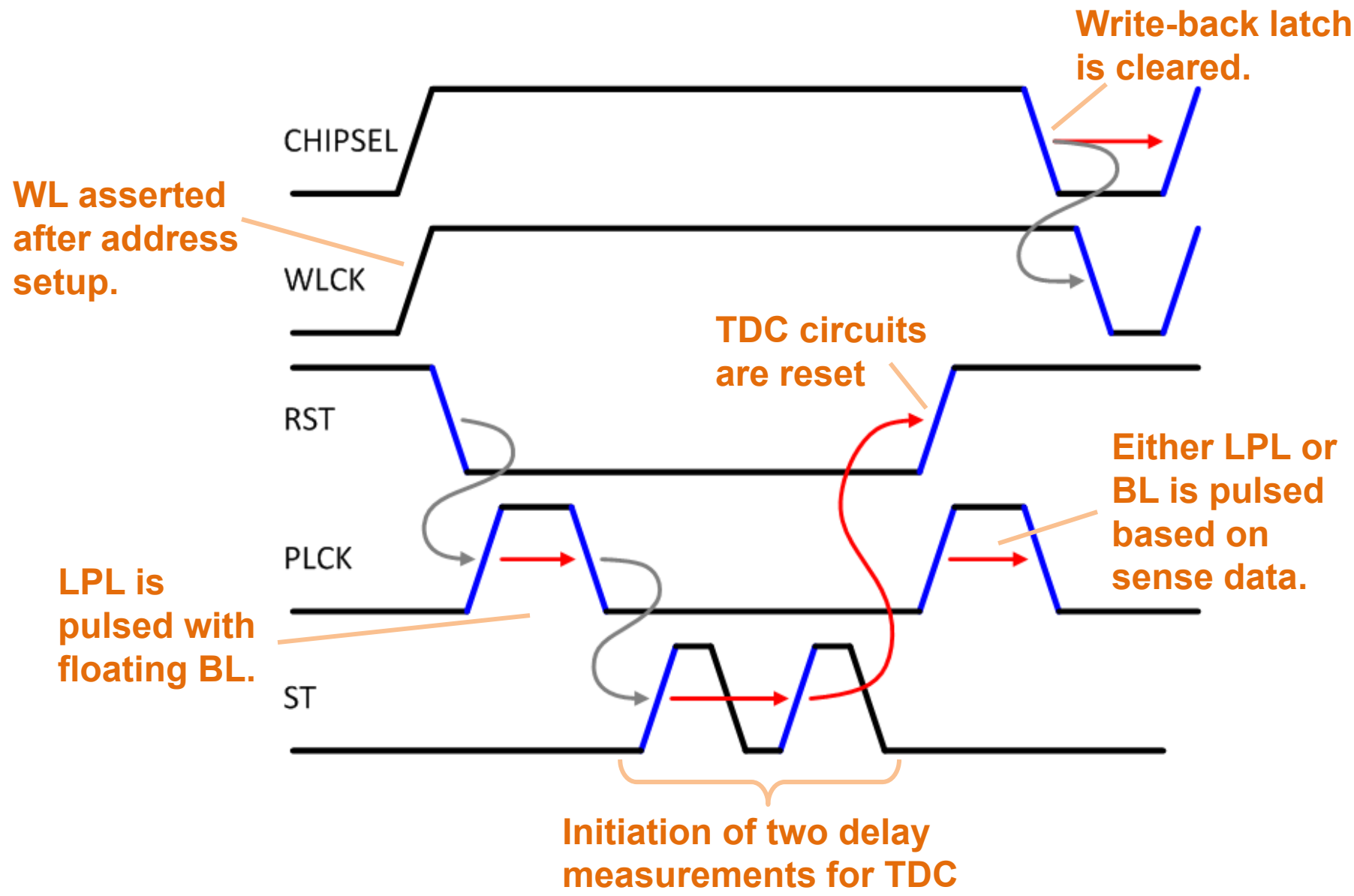
1Mb FeRAM Chip Summary

Organization	128k words of 8 bits
Technology	130nm LP CMOS
Full Macro-level Density	0.936 Mb/mm^2
Operating Voltage (CORE / WL)	1.5V/2.2V to 1.0V/1.7V
Read Cycle Time	200ns to 730ns
Read Power	772μW to 107μW

This work was funded in part by the FCRP Focus Center for Circuit & System Solutions (C2S2).

End

Timing Diagram – Read Cycle



The problem of imprint and midpoint reference

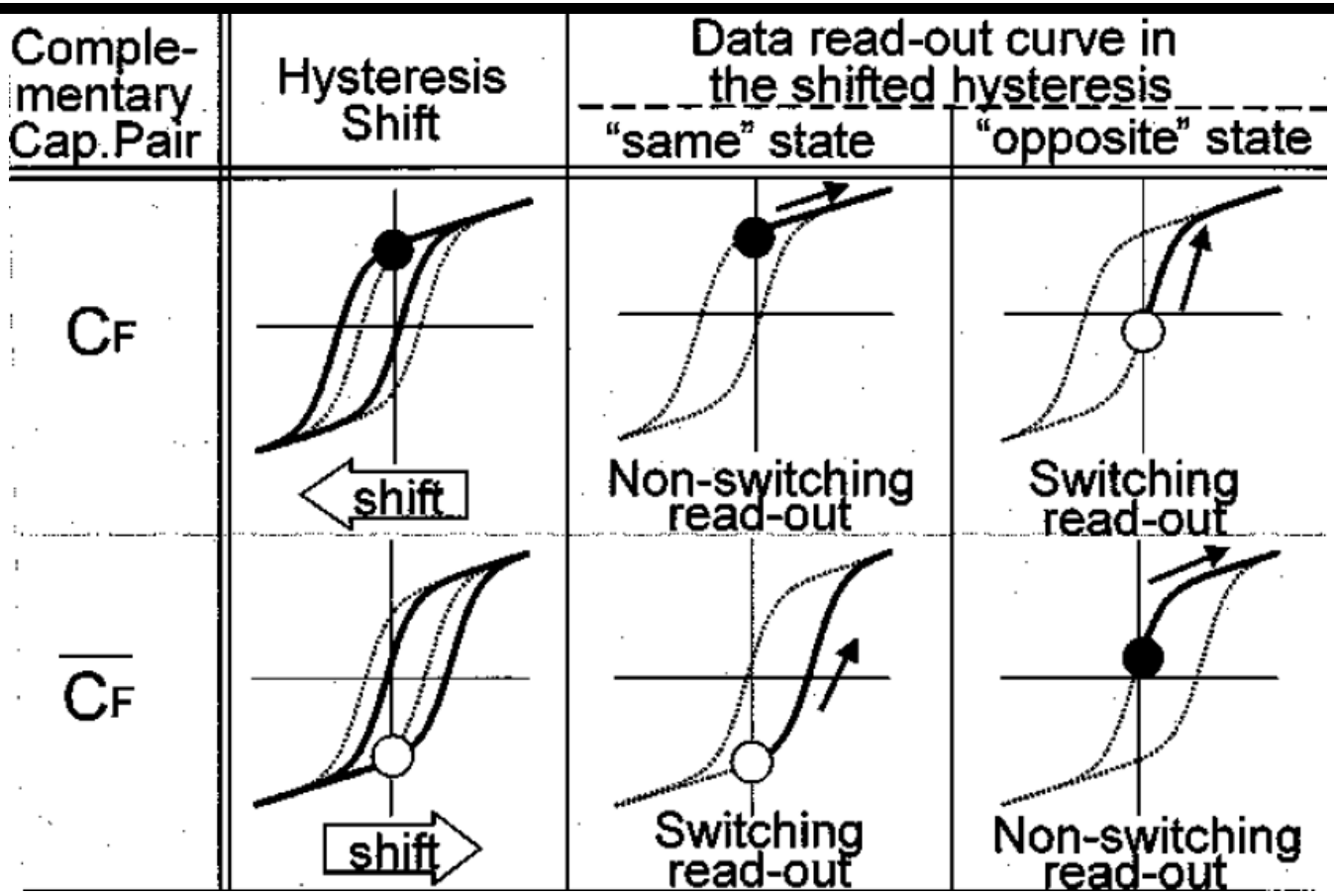


Figure courtesy of [Inoue 2001 TED]

- Imprint reduces "read 1" (switching) charge
- *For on-pulse sensing*: Imprint also changes relative voltage of *both* V0 and V1 bitline voltages
- *For after-pulse sensing*: It is not expected that V0 is increased significantly because of imprint.