Minimum Energy Tracking Loop with Embedded DC-DC Converter Delivering Voltages Down to 250mV in 65nm CMOS

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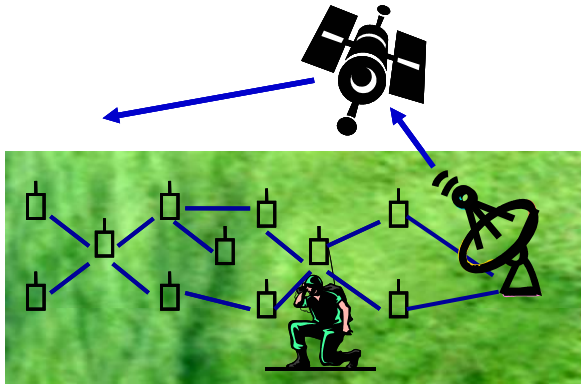
Micro-Power Applications

Wireless-sensor Networks



Medical Devices

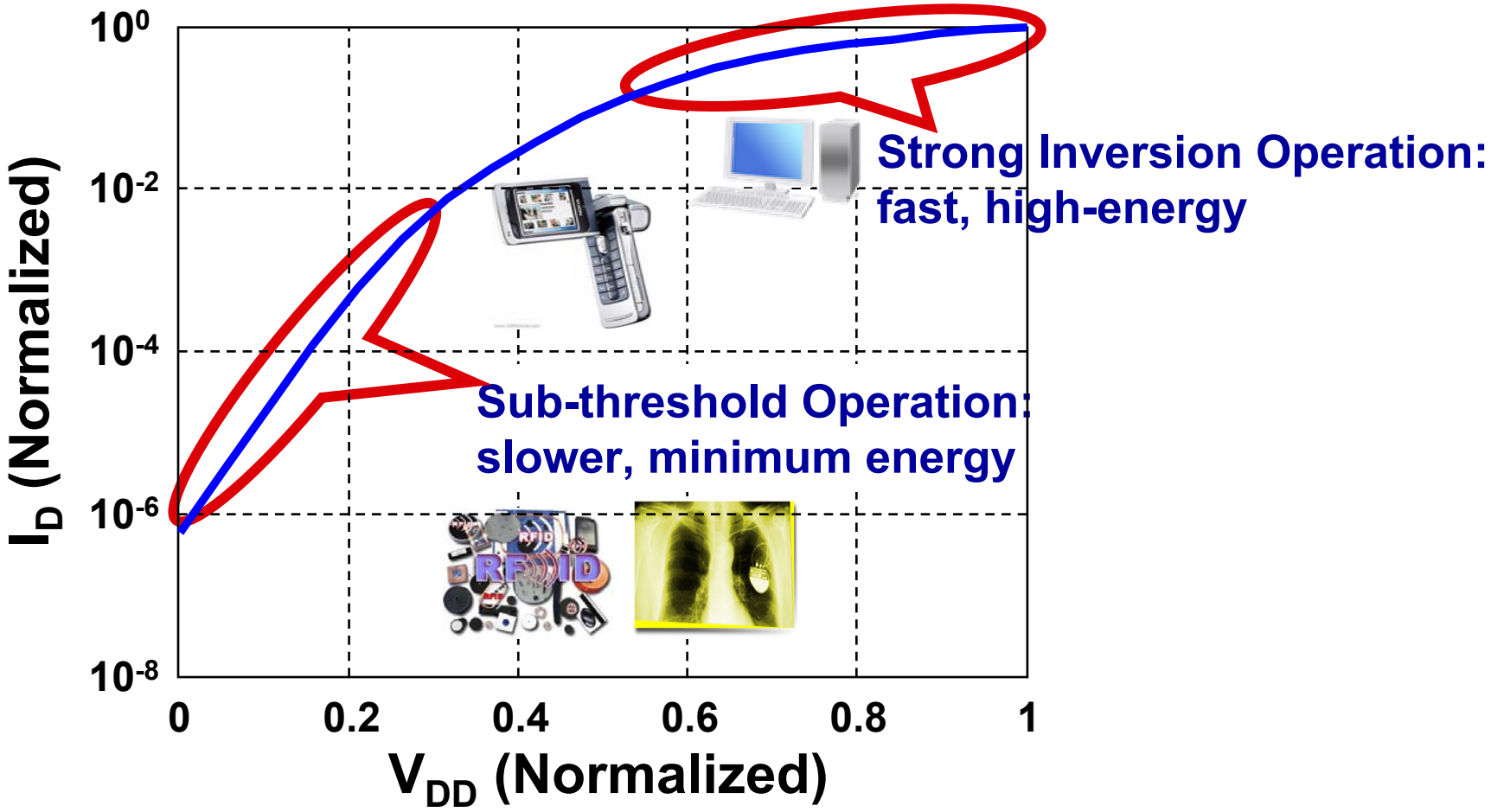
Ambient Intelligence, RFID

- Emerging energy-constrained applications
- Increase battery life-time through system-level energy management techniques
- Energy scavenging possible - system power <10µW

Outline

- Motivation and System Architecture
- Energy Sensing Technique
- Low Power DC-DC Converter
- Measurement Results
- Conclusions

Sub-threshold Operation

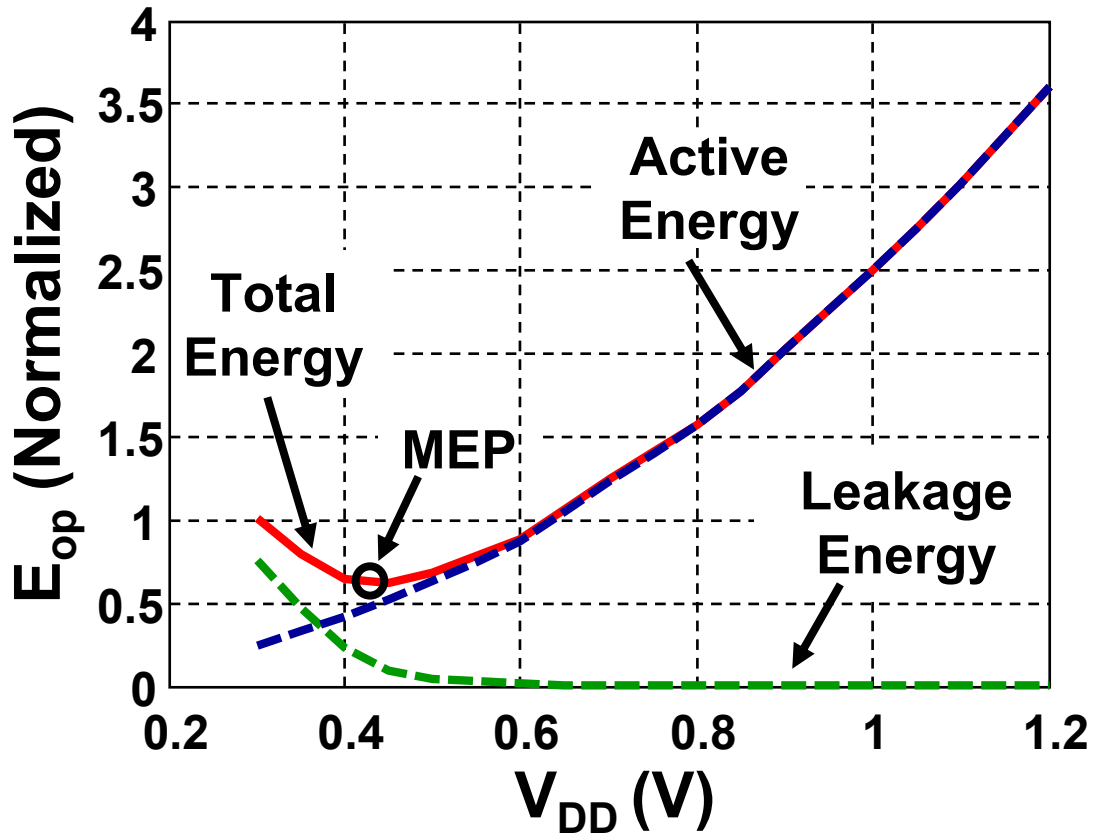


Goal: Minimize Energy per Operation

Minimum Energy Point (MEP)

$$E_{TOTAL} = E_{ACTIVE} + E_{LEAKAGE}$$

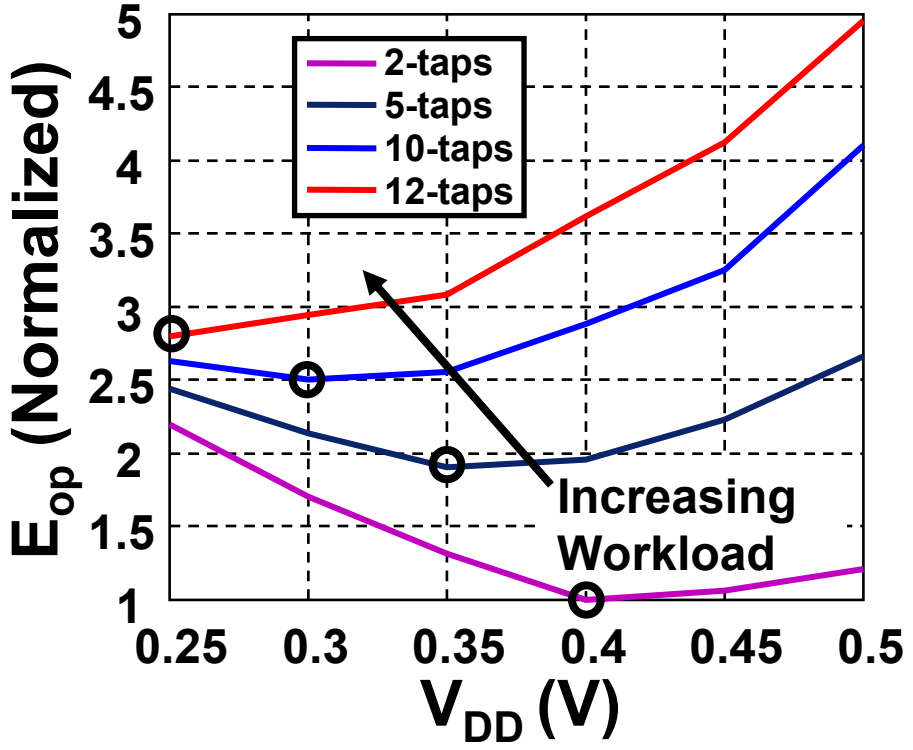
$$= CV_{DD}^{2} + I_{OFF} V_D T_D = V_{DD}^{2} \left(C_{eff} + L_{eff} e^{\frac{-V_{DD}}{nV_{th}}} \right)$$



65nm simulation for 7-tap FIR filter showing minimum energy operation

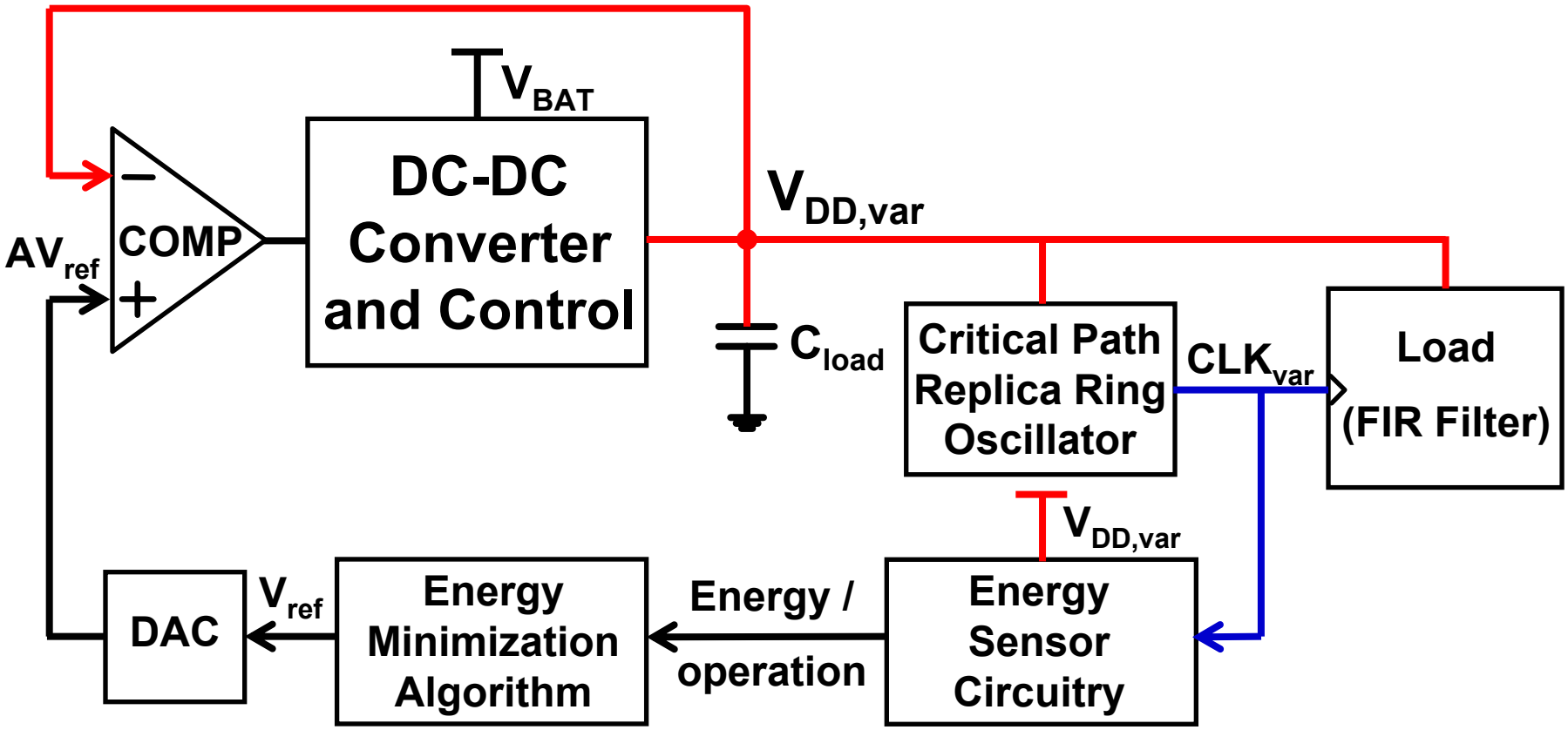
Motivation – Minimum Energy Tracking

Workload, Activity ↑	E_{ACTIVE} ↑	V_{MEP} ↓
Temperature, Duration of Leakage ↑	$E_{LEAKAGE}$ ↑	V_{MEP} ↑



- Minimum Energy Point (MEP) varies with workload and temperature
- MEP moves when ratio of active to leakage energy changes
- Tracking the MEP : 0.5X – 1.5X energy savings

Minimum Energy Tracking Loop



- Completely on-chip except for the passive filter components

Energy/Operation (E_{op}) Formulation

- Voltage across storage capacitor C_{load} droops from V_1 to V_2 in the course of N (i.e. 32 or 64) operations.

$$E_{op} = \frac{C_{load}}{2 \times N}\left(V_1^2 - V_2^2\right) = \frac{C_{load}}{2 \times N}\left(V_1 + V_2\right)\left(V_1 - V_2\right) \approx \frac{C_{load}}{N} V_1\left(V_1 - V_2\right)$$

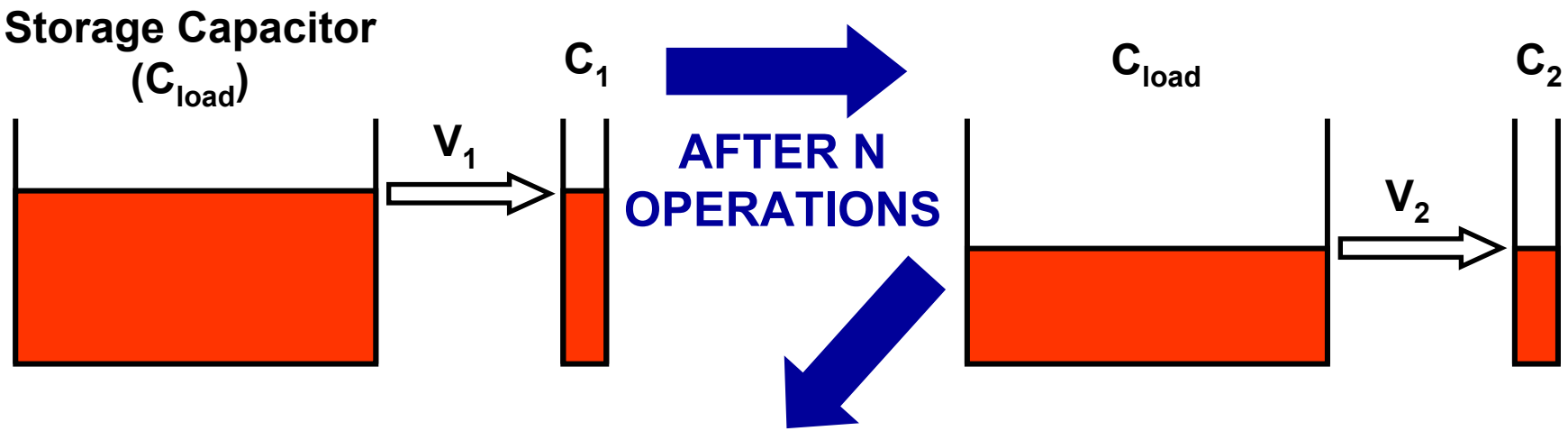
$$E_{op} \propto V_1\left(V_1 - V_2\right)$$

- V_1 is set digitally as V_{ref} to the DC-DC converter
- $(V_1 - V_2)$ needs to be estimated

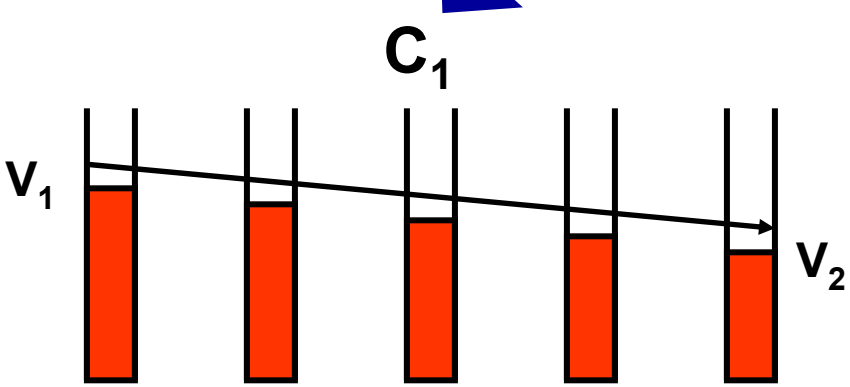
Calculating $V_1 - V_2$

1. Sample V_1 across C_1

2. Sample V_2 across C_2

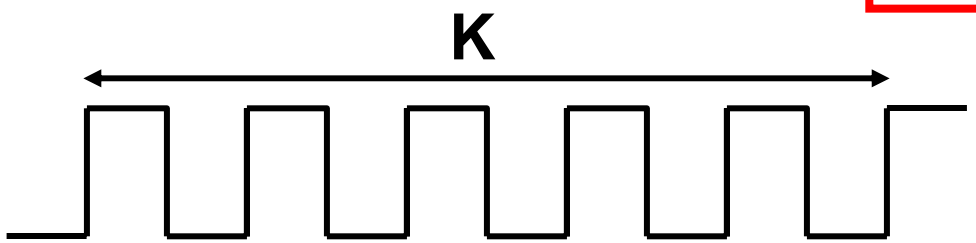


3. Drain C_1 to V_2

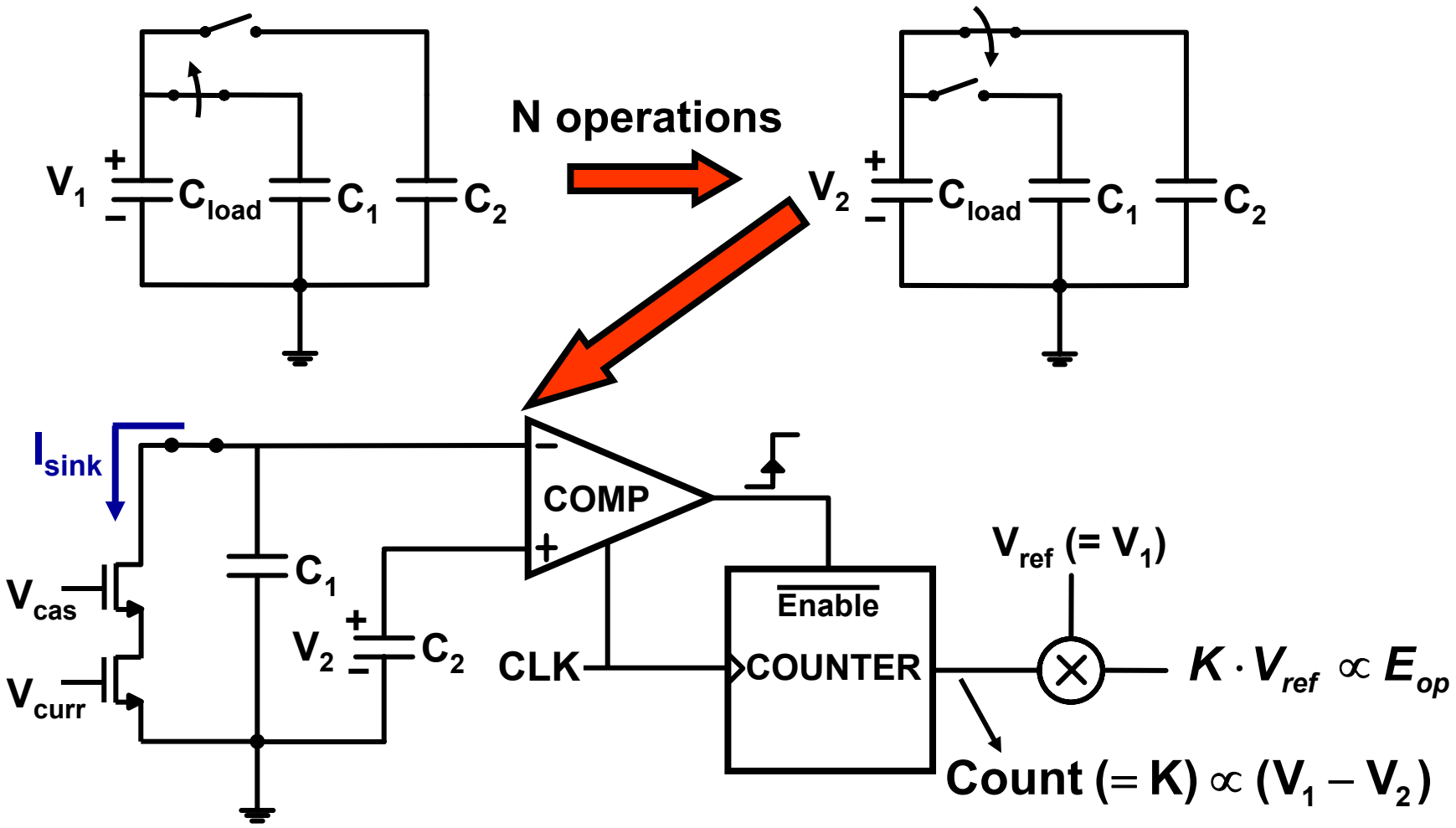


$$K \propto (V_1 - V_2)$$

Count no. of clock cycles

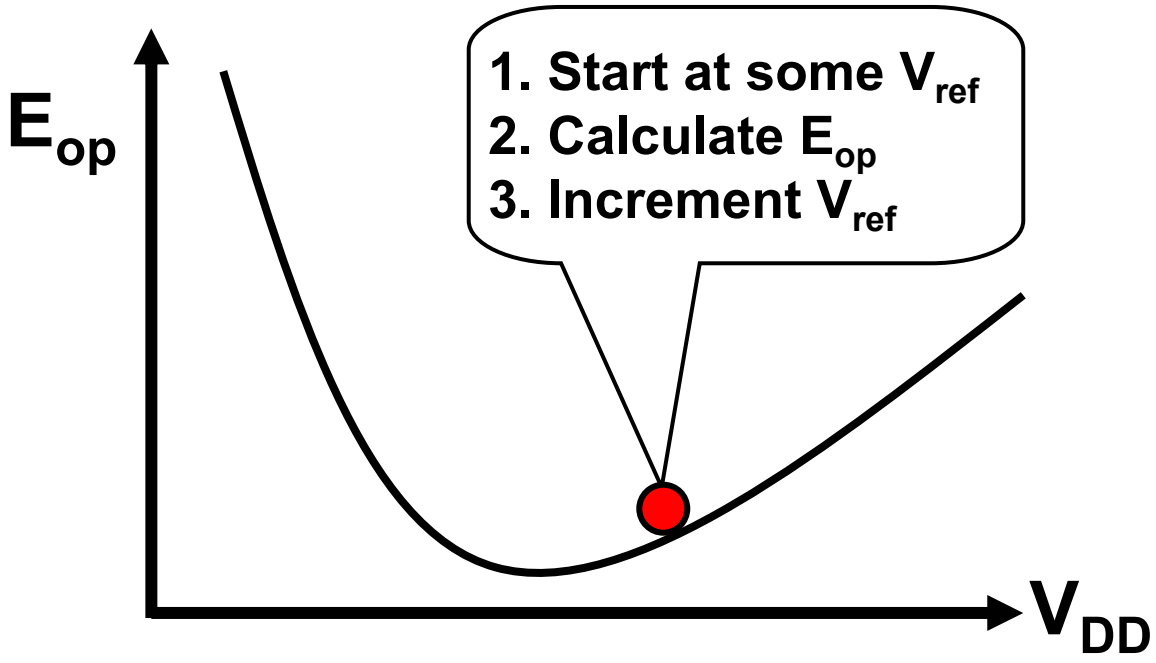


Calculating Energy/Operation



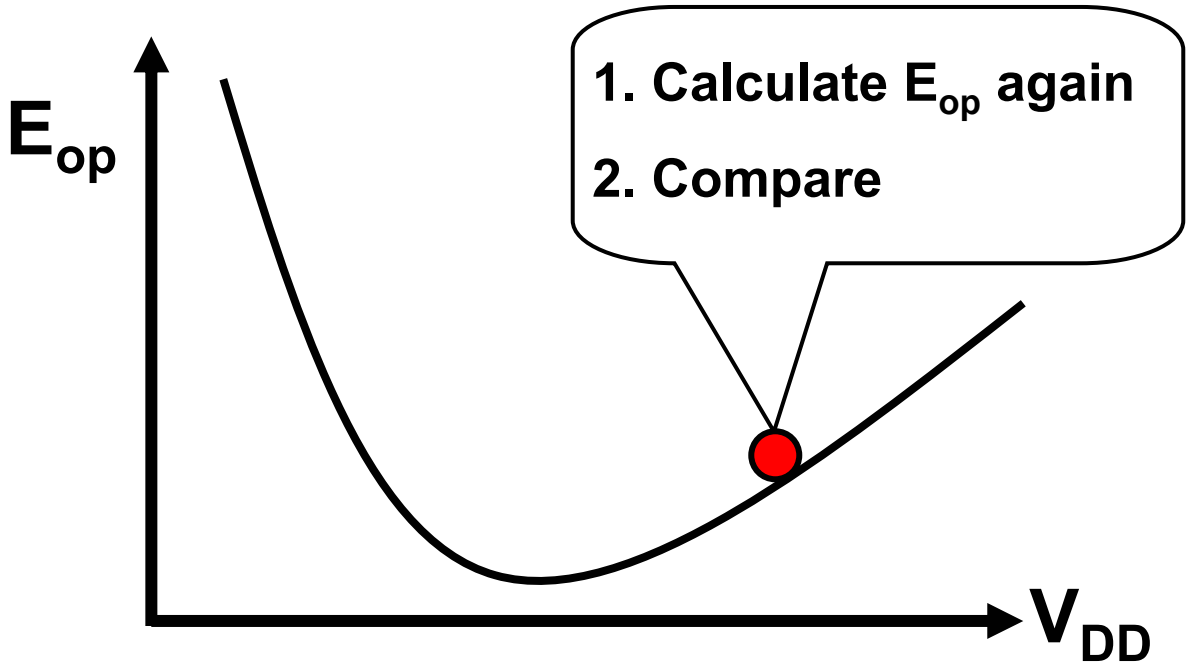
- Digital representation of E_{op} is obtained
- Absolute value of E_{op} not required

Minimum Energy Tracking Algorithm



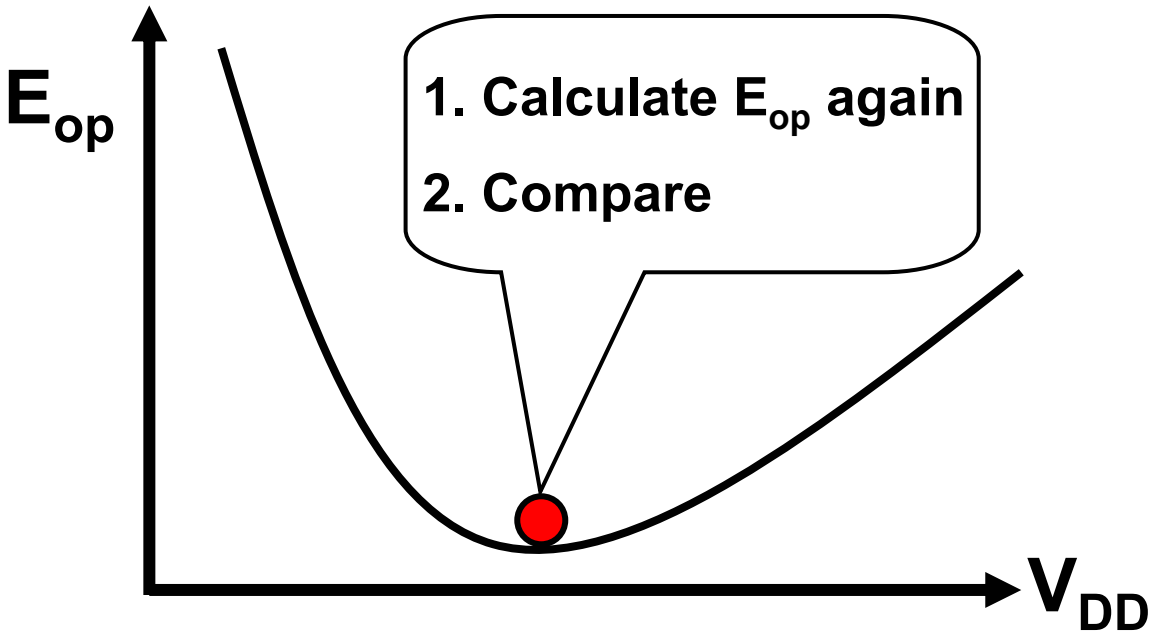
- Uses a slope tracking algorithm
- Starting V_{ref}, initial direction can be set by the user

Minimum Energy Tracking Algorithm



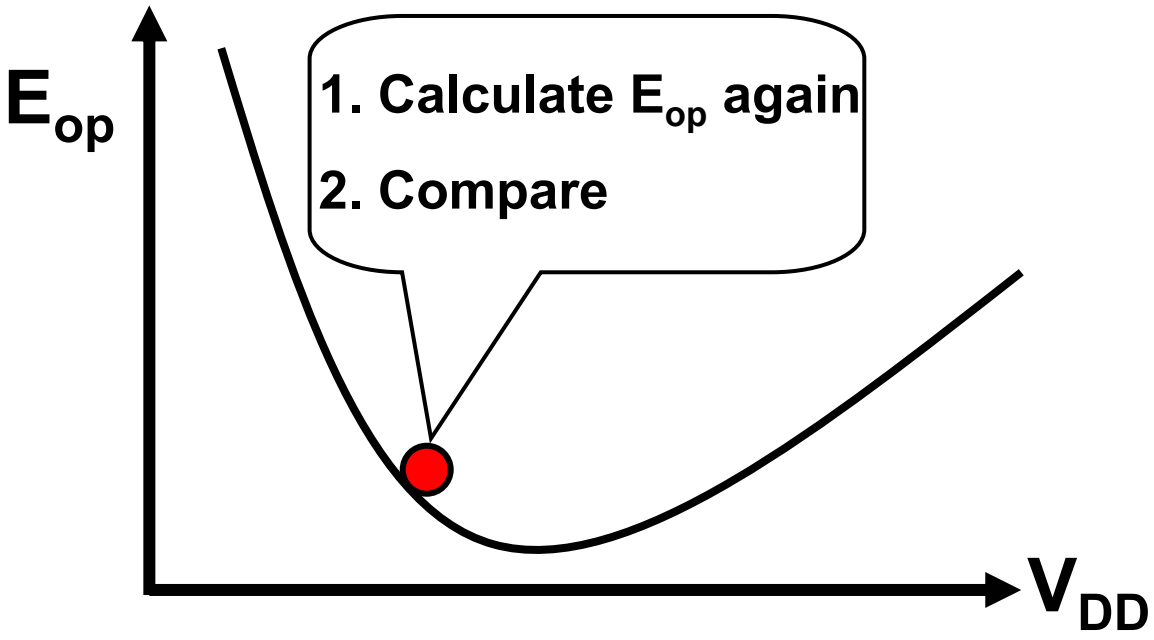
- If new E_{op} is smaller, continue incrementing V_{ref}
- Else, change direction and decrement V_{ref} until minimum is achieved

Minimum Energy Tracking Algorithm



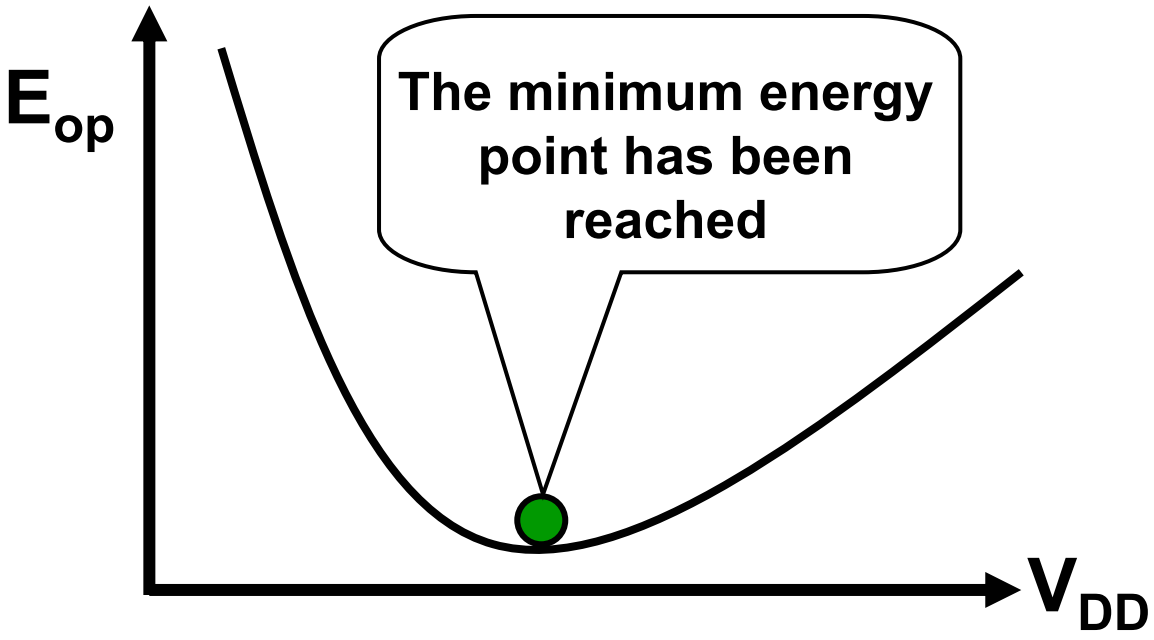
- The new E_{op} is smaller, hence the loop continues to decrement V_{ref}
- One more computation is required before the loop settles to the minimum energy

Minimum Energy Tracking Algorithm



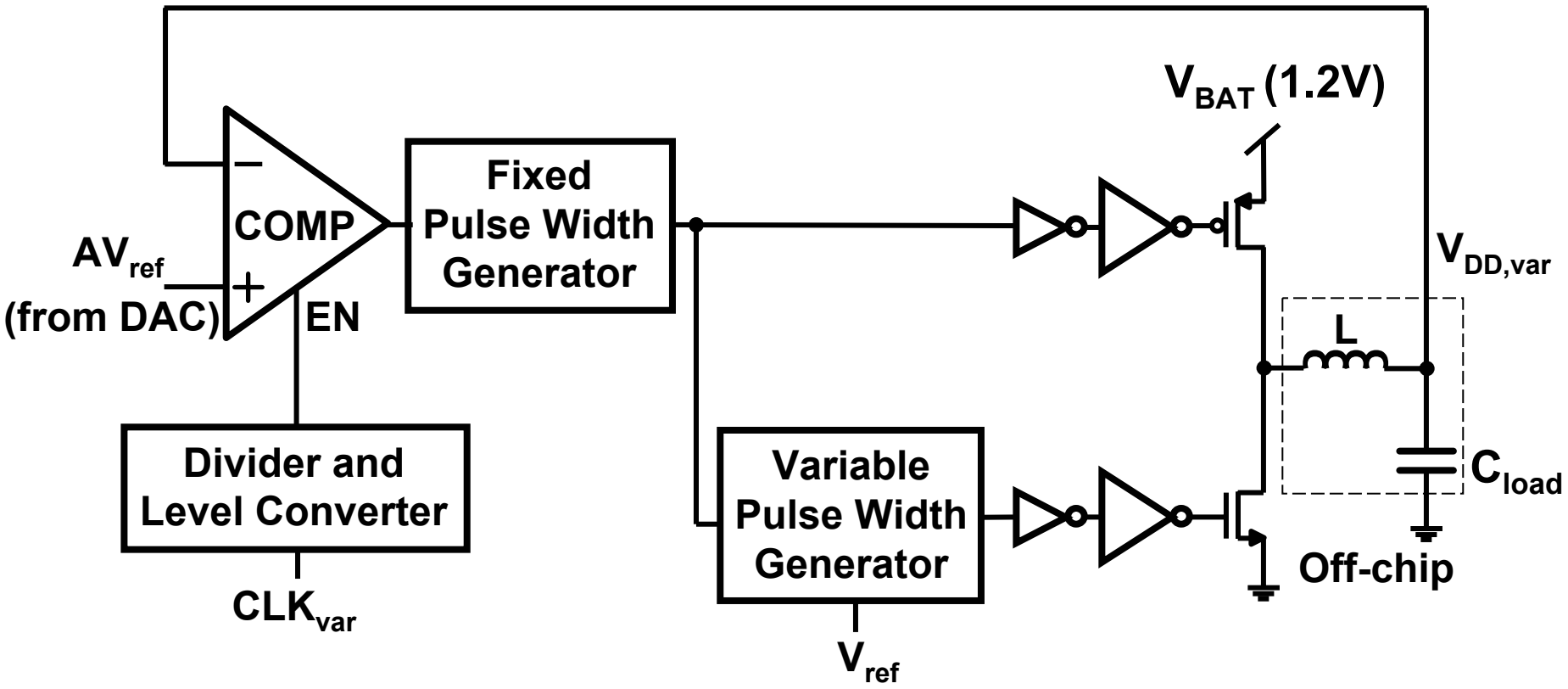
- The new E_{op} is higher, so the loop reverses direction and increments V_{ref} one last time

Minimum Energy Tracking Algorithm



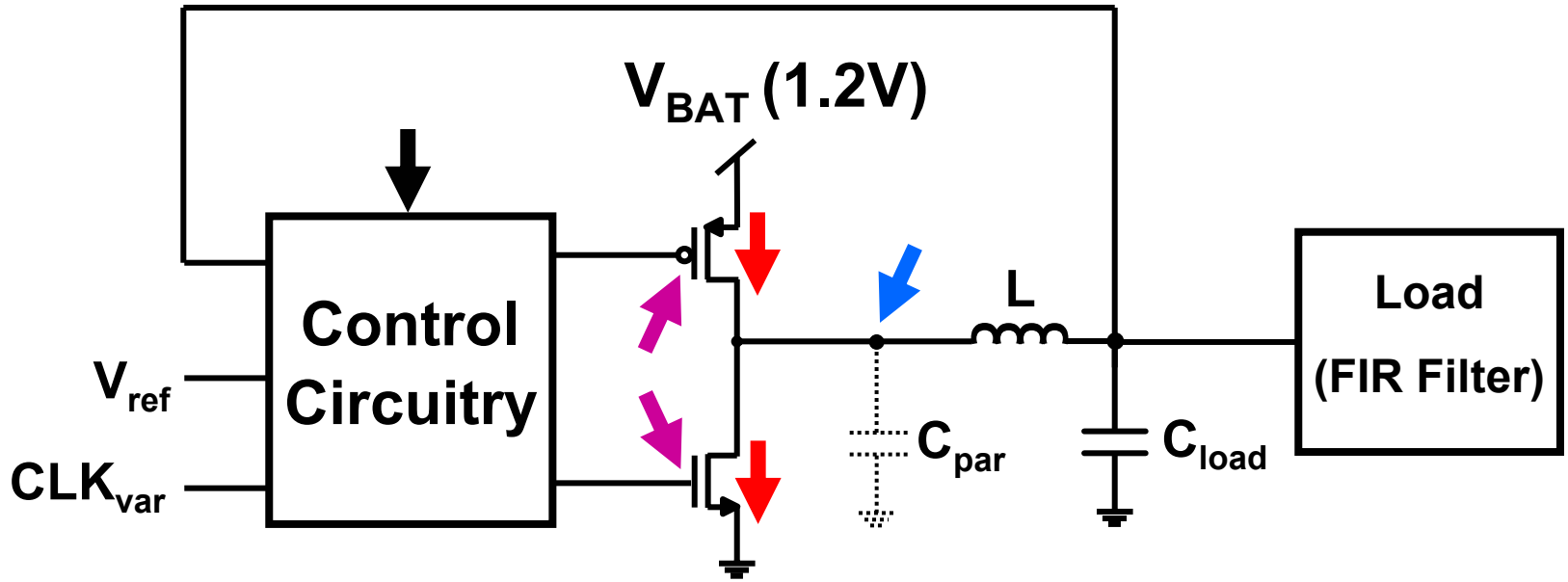
- V_{ref} is set at the minimum energy point
- The loop shuts down
- The load circuit continues to operate

DC-DC Converter Architecture



- V_{DD} : 250mV – 700mV ; Load Power : 1µW – 100µW
- Converter operates in Pulse Frequency Modulation (PFM) mode
- V_{ref} is set digitally by the loop

DC-DC Converter Loss Mechanisms



→ Conduction Loss (E_{cond})

→ Parasitic Loss (E_{par})

→ Switching Loss (E_{sw})

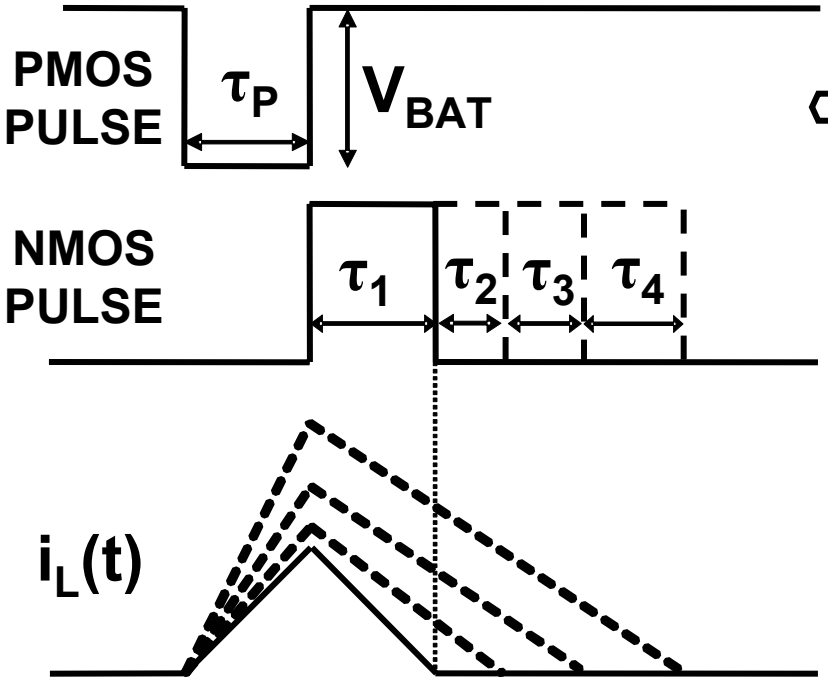
→ Control Loss (E_{cont})

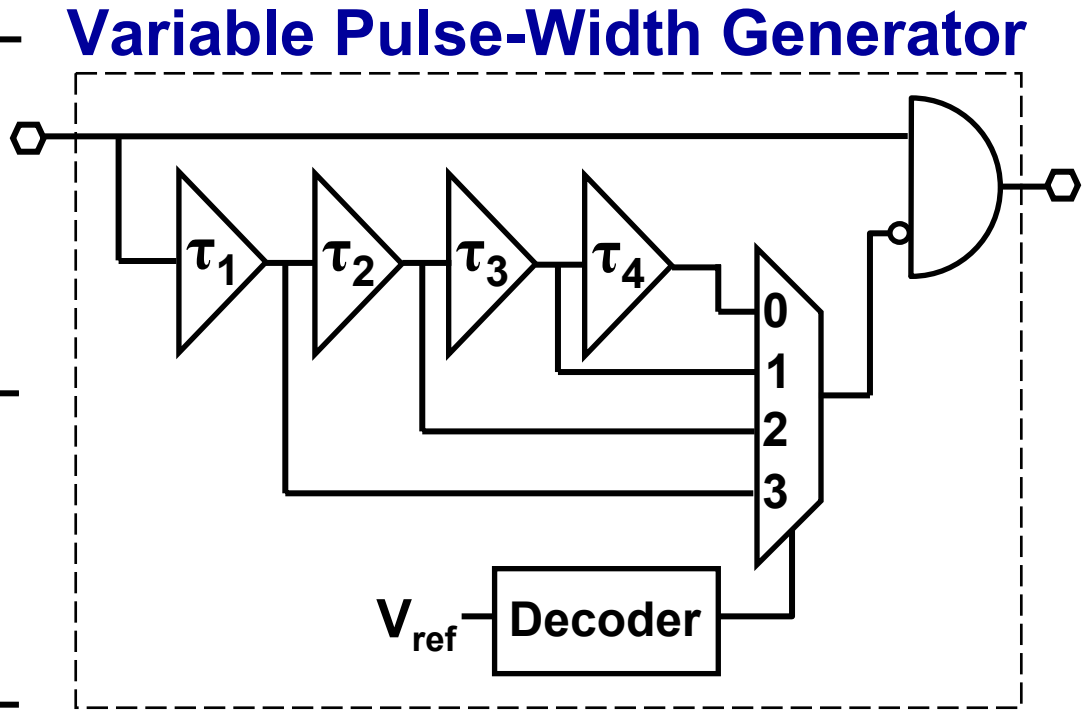
E_{load} – Energy Delivered to the load / cycle

Efficiency

$$\eta = \frac{E_{load}}{E_{load} + E_{cond} + E_{sw} + E_{par} + E_{cont}}$$

Approximate Zero-Current Switching





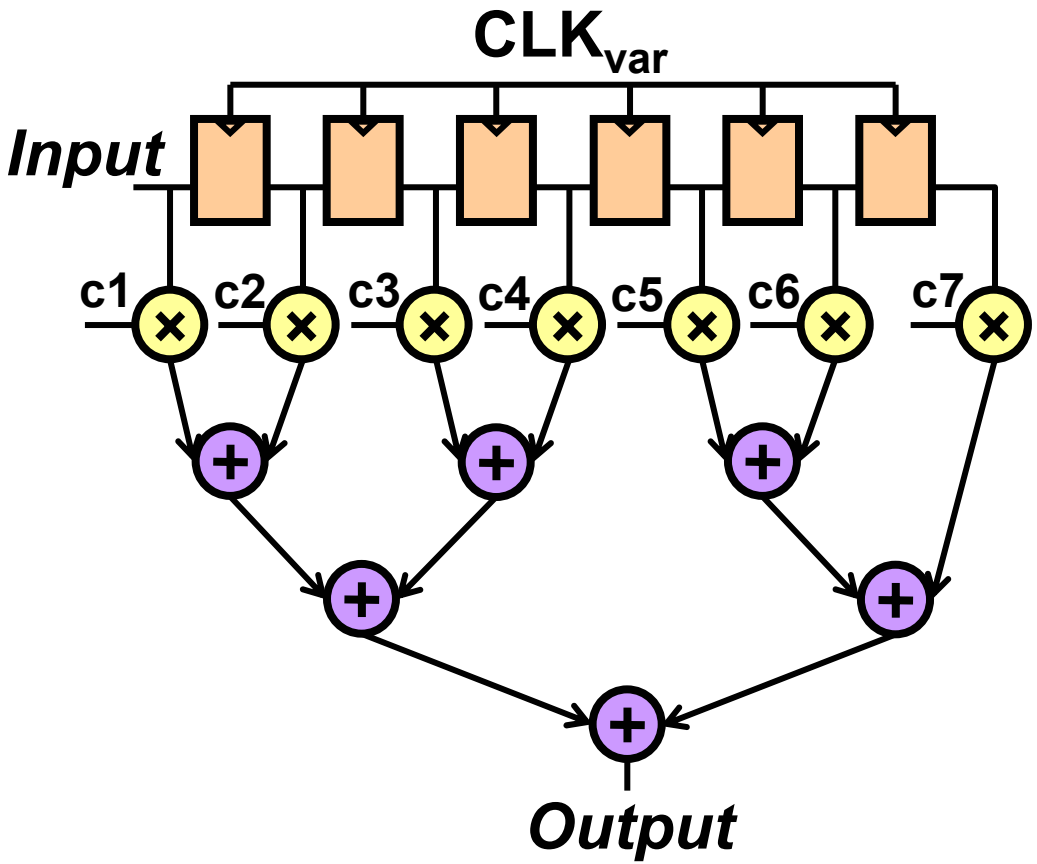
$$\frac{\tau_N}{\tau_P} = \frac{V_{BAT} - V_{DD}}{V_{DD}}$$

- No high gain amplifiers
- PMOS pulse width set constant
- NMOS pulse width adjusted to achieve ZCS
- Independent of L, absolute delay values

Techniques to Improve Efficiency

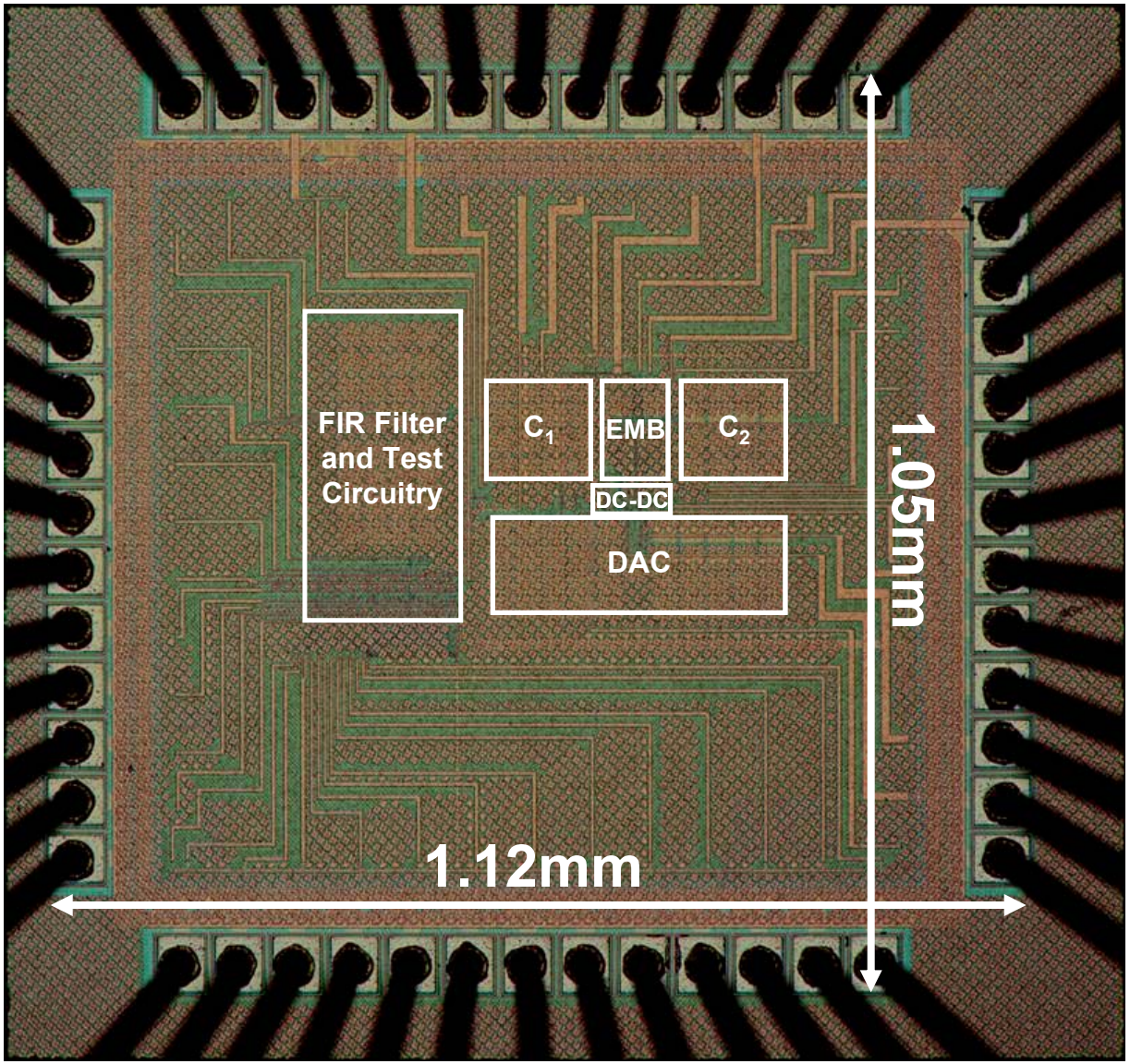
- **Conduction, Switching Loss**
  - Optimal Power Transistor Sizing
- **Control Loss (affects low load efficiency)**
  - Simple PFM Control
  - All-digital control to achieve approximate ZCS
  - Comparator clock scales with load power
- **Parasitic Capacitance Loss**
  - Finite delay between PMOS and NMOS pulses
  - Increase E_{load}, minimize contribution of E_{par}

Test Load - FIR Filter



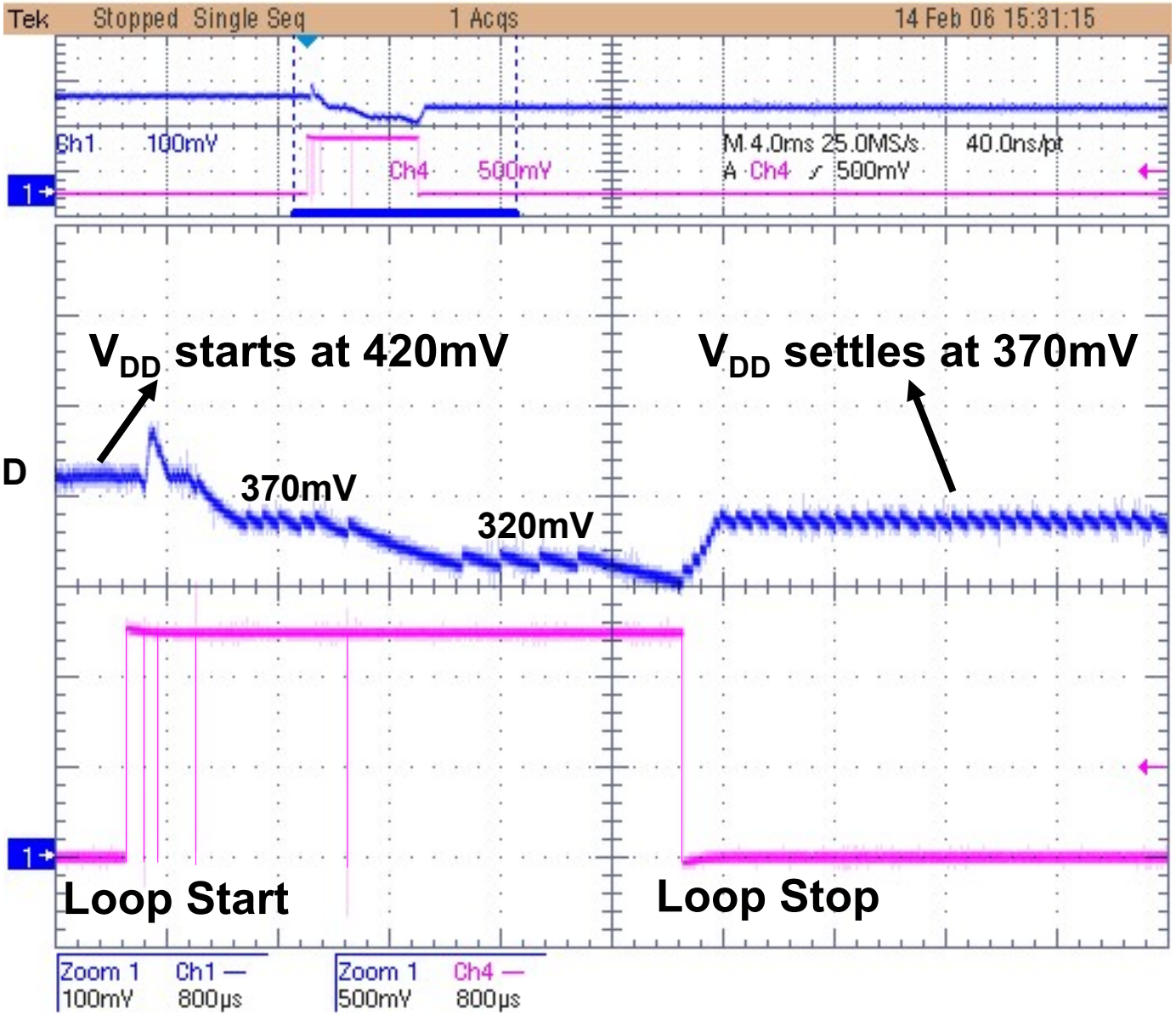
- 7-tap FIR filter capable of operation down to 250mV
- Workload varied by changing the number of taps
- Leakage remains constant as number of taps are changed

Test Chip Die Photo



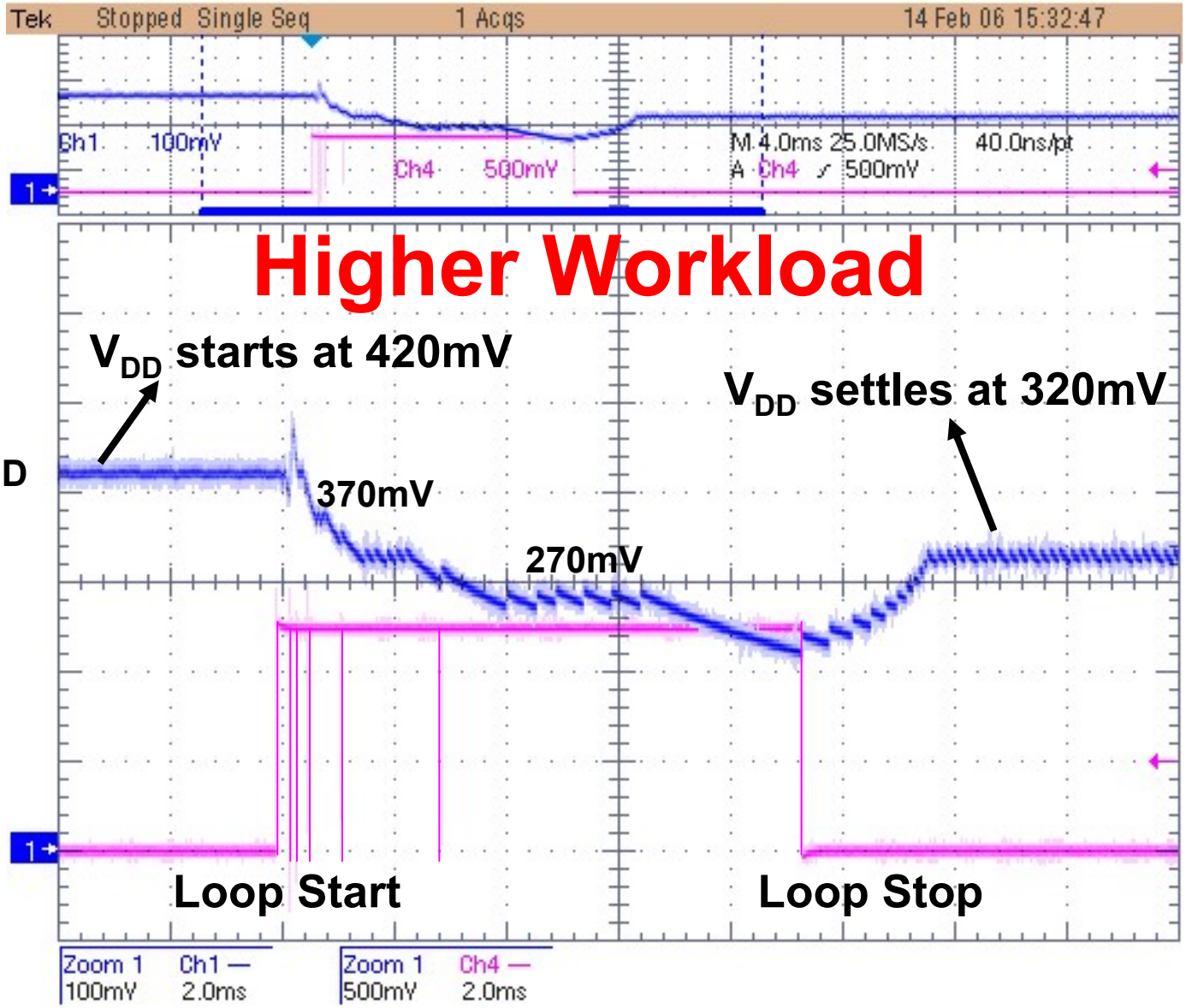
- 65nm,6LM CMOS
- Die area – 1.05mm x 1.12mm
- Circuit active area – 0.23 mm^2
- Minimum energy tracking circuitry occupies just 0.05mm^2

Operation of the Energy Minimizing Loop



1-tap MEP = 370mV

Operation of the Energy Minimizing Loop

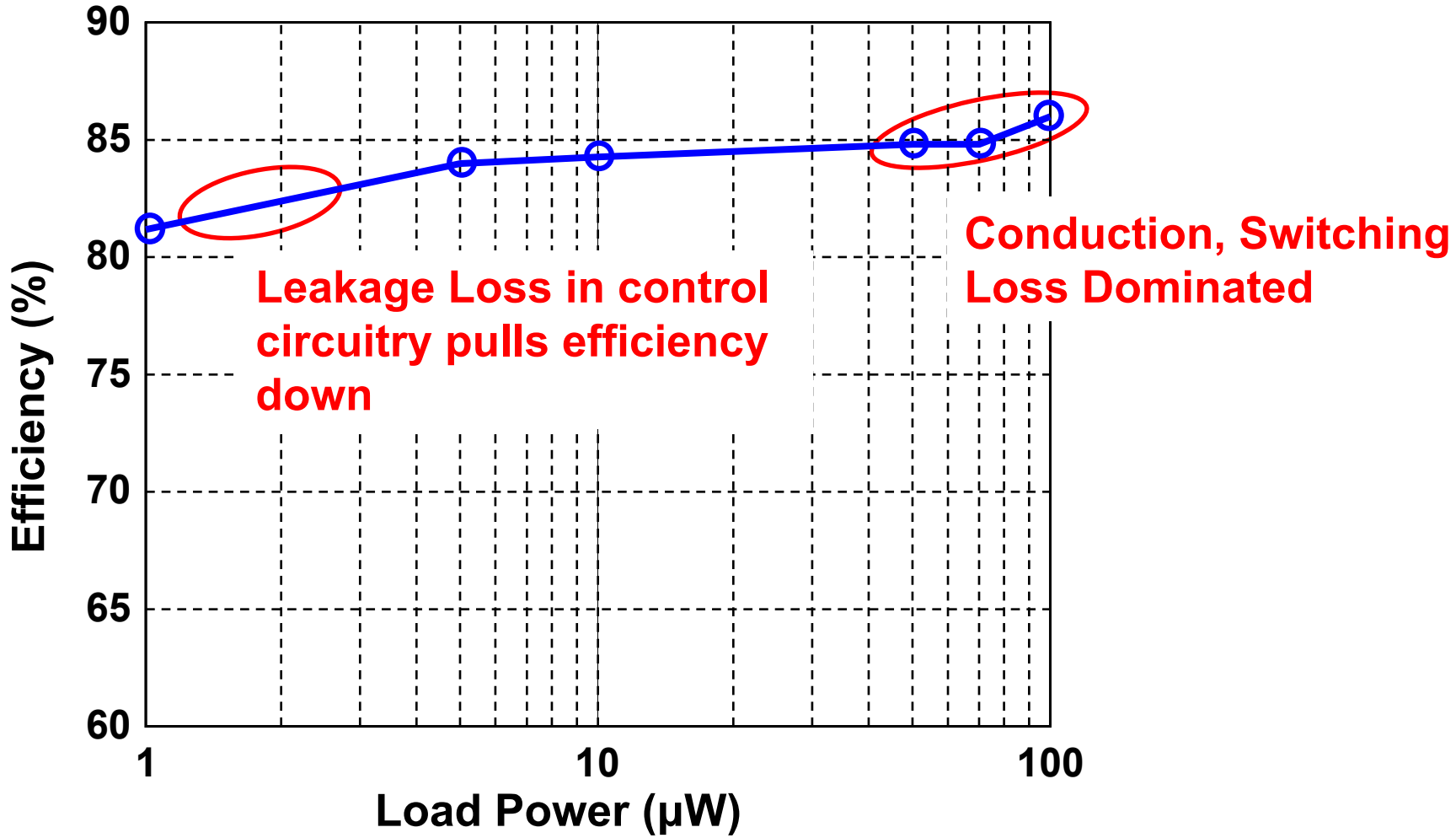


7-taps

MEP

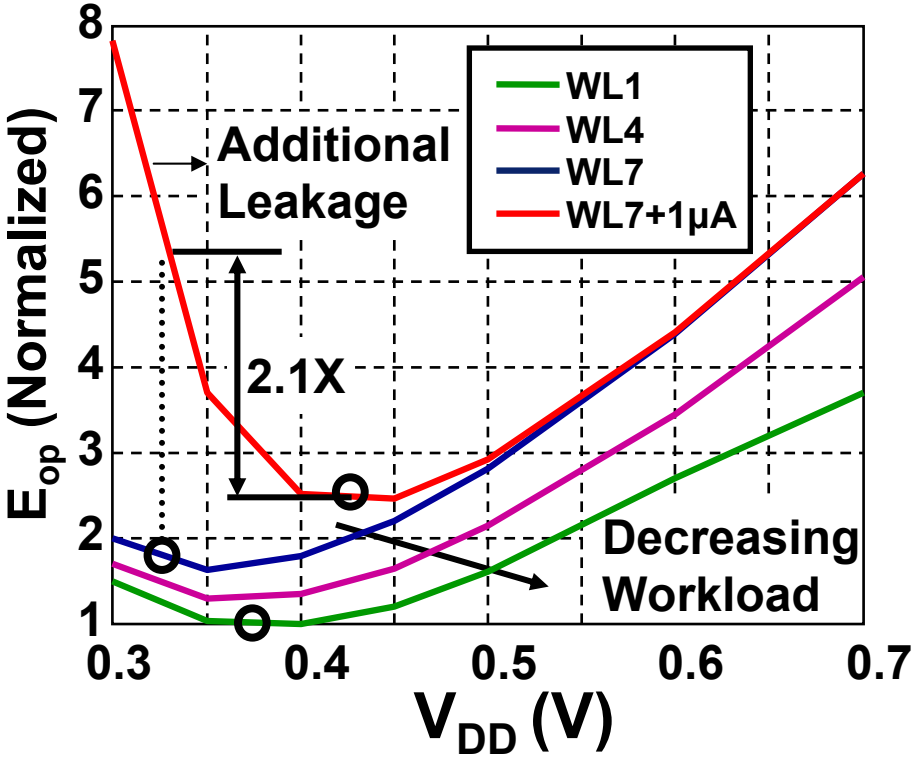
= 320mV

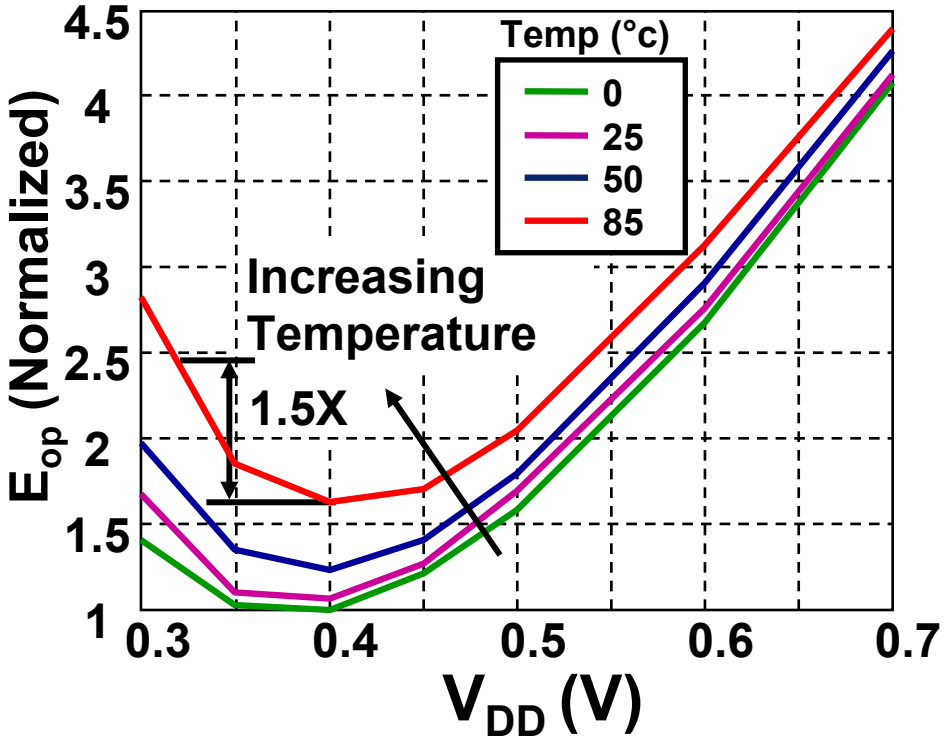
DC-DC Converter Efficiency



>80% efficiency while delivering 1µW load power

Measured Energy Savings





- MEP increases on decreasing workload – **1.1X** energy savings
- MEP increases with increase in temperature – **0.5X** energy savings

MEP Tracking Loop Properties

- **Tracking Loop**
  - Non-invasive tracking
  - Energy computed of the actual circuit – no replicas
- **Tracking Methodology**
  - Independent of the size of the load circuit
  - Independent of the DC-DC converter topology
- **Overhead**
  - Energy overhead ~ 50 operations
  - Area overhead = 0.05mm^2
  - Multiple loops – distinct voltage domains

Conclusions

- Control loop tracks minimum energy voltage of arbitrary digital circuits
- On-chip energy sensor circuitry has very low energy and area overhead
- Low power DC-DC converter achieves >80% efficiency at 1μW load power

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