Voltage Scalable Switched Capacitor DC-DC Converter

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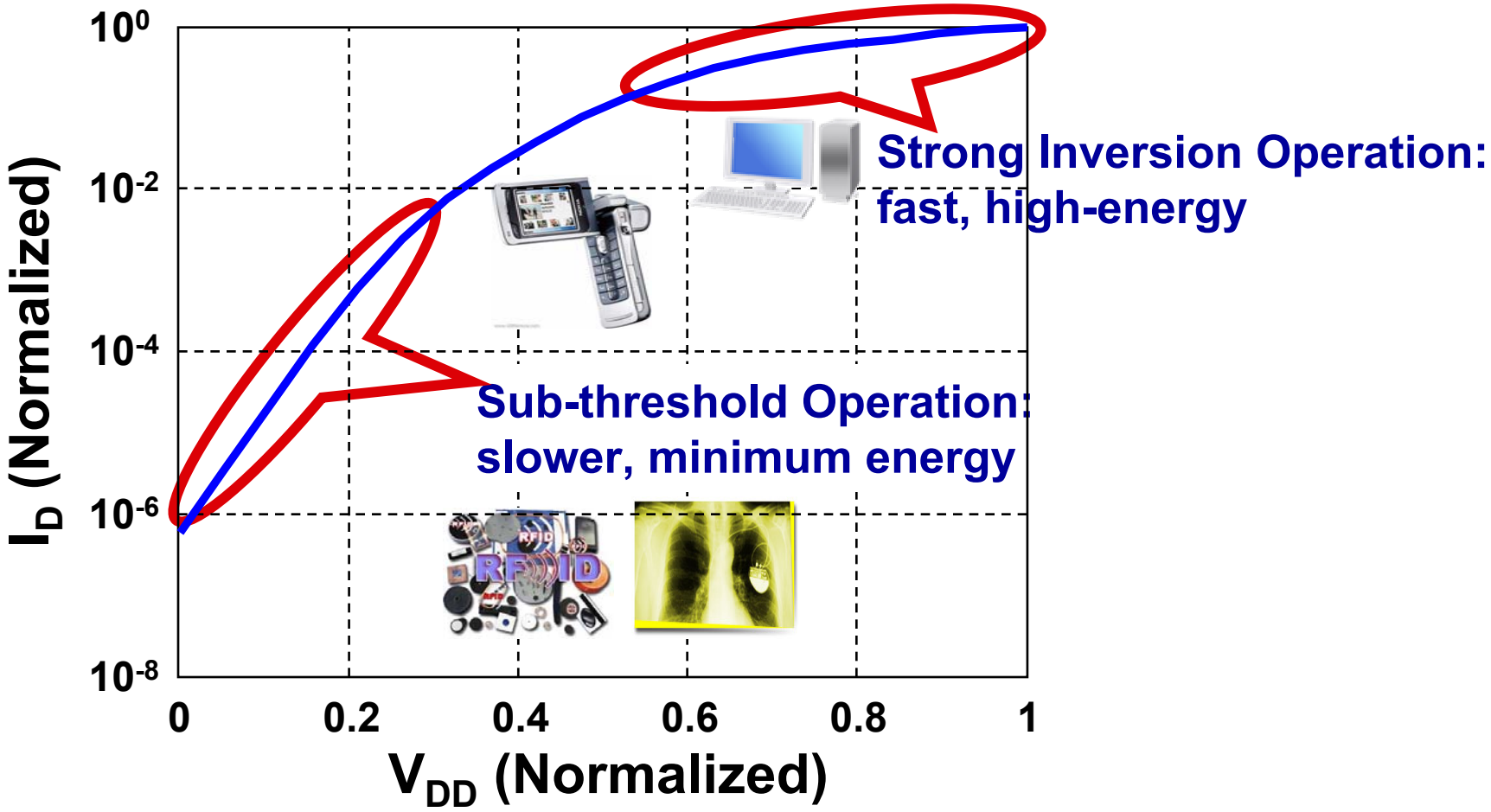
Outline

- Motivation
- Scalable Voltage Generation
- Techniques to improve Efficiency
- Measured Results
- Conclusions

Ultra-Dynamic Voltage Scaling (U-DVS)



Goal: Operate at the lowest voltage that meets performance requirements

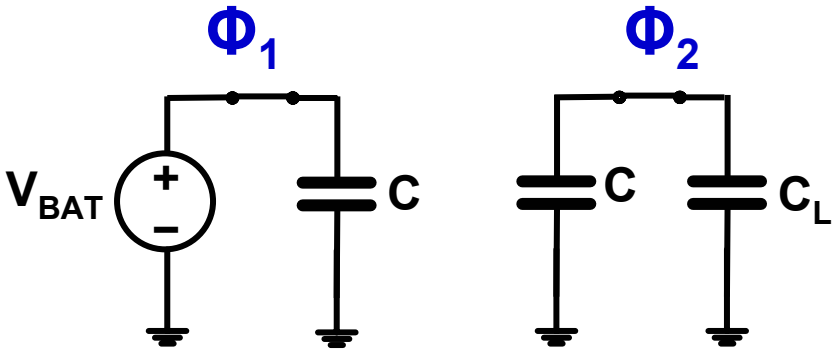
U-DVS DC-DC Converter Requirements

- Battery Voltage: 1.2V
- Output Load Voltage: 0.3 – 1.1V
- Output Load Power: 1μW – 1mW
- On-chip charge transfer capacitors
- Multiple Voltage Domains

Capacitive Charge Transfer

$V_L = V_{BAT} - \Delta V$

$$\eta_{BL} = \frac{V_{BAT} - \Delta V/2}{V_{BAT}} \cdot \frac{V_{BAT} - \Delta V}{V_{BAT} - \Delta V/2}$$

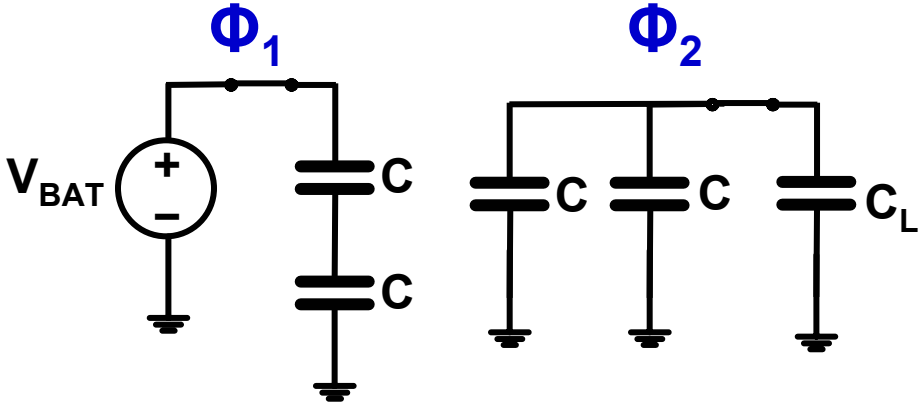


$$\eta_{BL} = \frac{V_{BAT} - \Delta V}{V_{BAT}} = \frac{V_L}{V_{NL}}$$

$C_L >> C$

$V_L = V_{BAT}/2 - \Delta V$

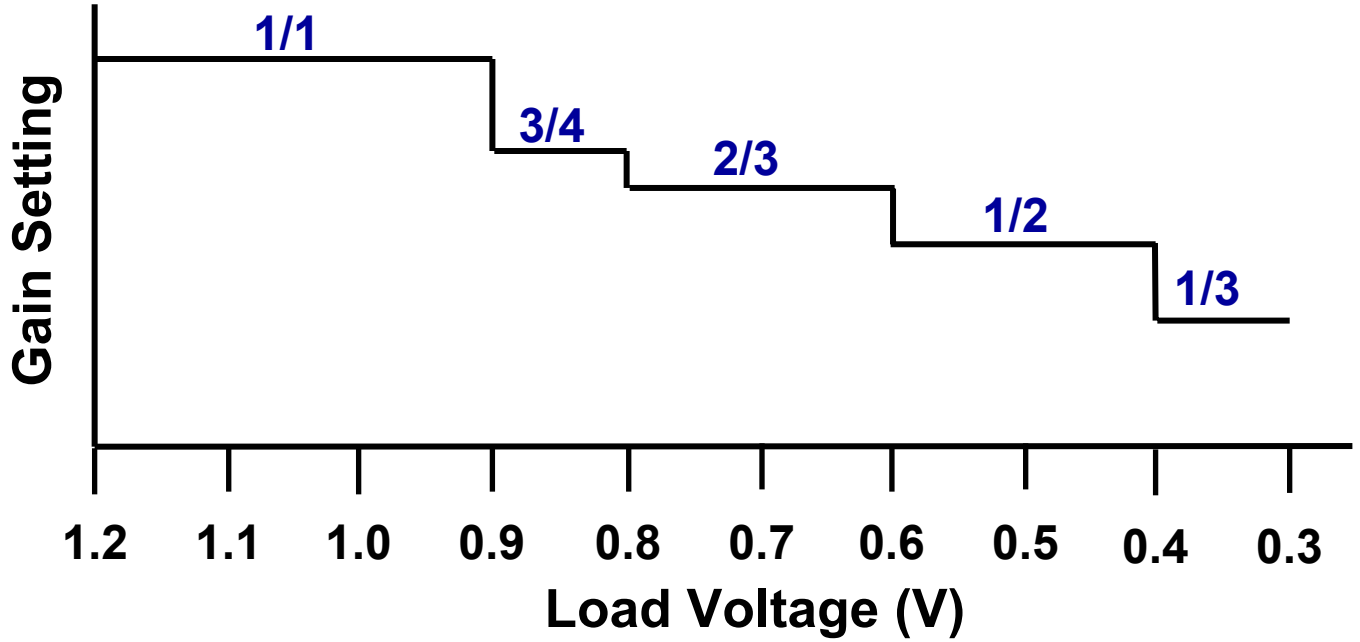
$$\eta_{BL} = \frac{V_{BAT} - \Delta V}{V_{BAT}} \cdot \frac{V_{BAT}/2 - \Delta V}{V_{BAT}/2 - \Delta V/2}$$



$$\eta_{BL} = \frac{V_{BAT}/2 - \Delta V}{V_{BAT}/2} = \frac{V_L}{V_{NL}}$$

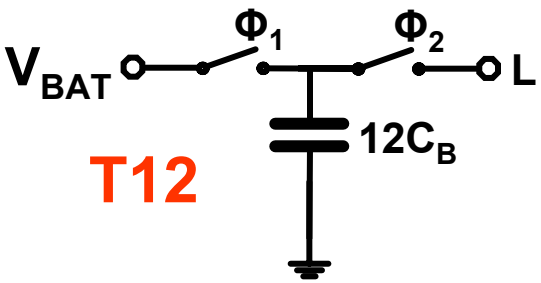
- **Linear drop in efficiency**

Need for different Topologies



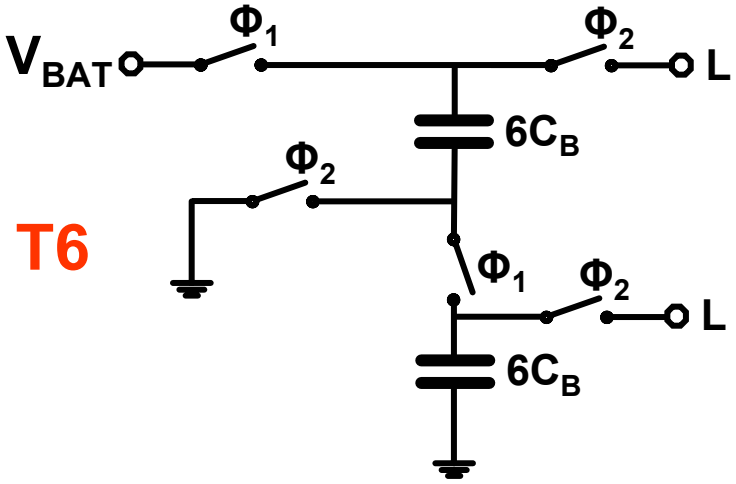
- Linear efficiency drop necessitates topologies with V_{NL} close to the load voltage desired
- Practical ratios: p/q; q<5 and p<q for buck converters
- Ratios used: 1/1, 1/2, 1/3, 2/3 and 3/4

Scalable Voltage Generation



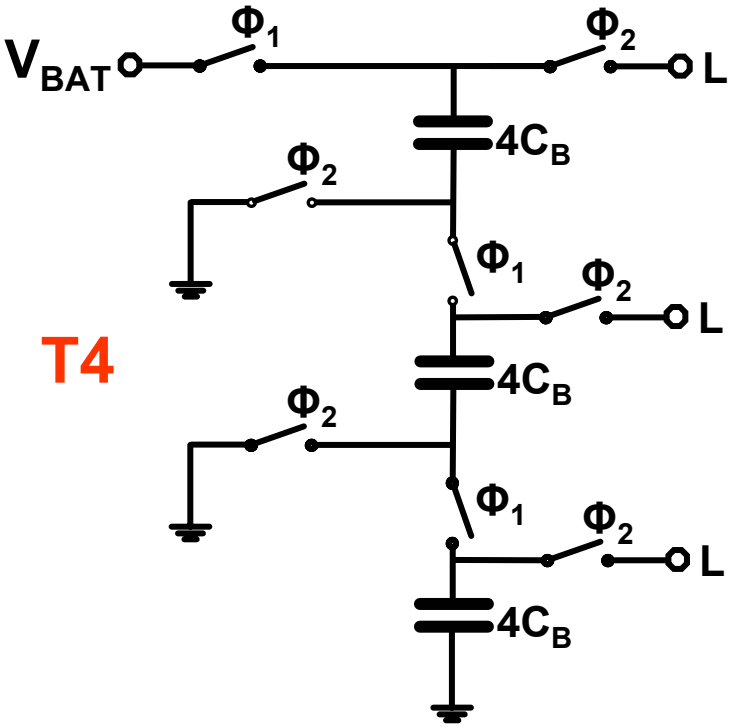
T12

Ratio: 1/1



T6

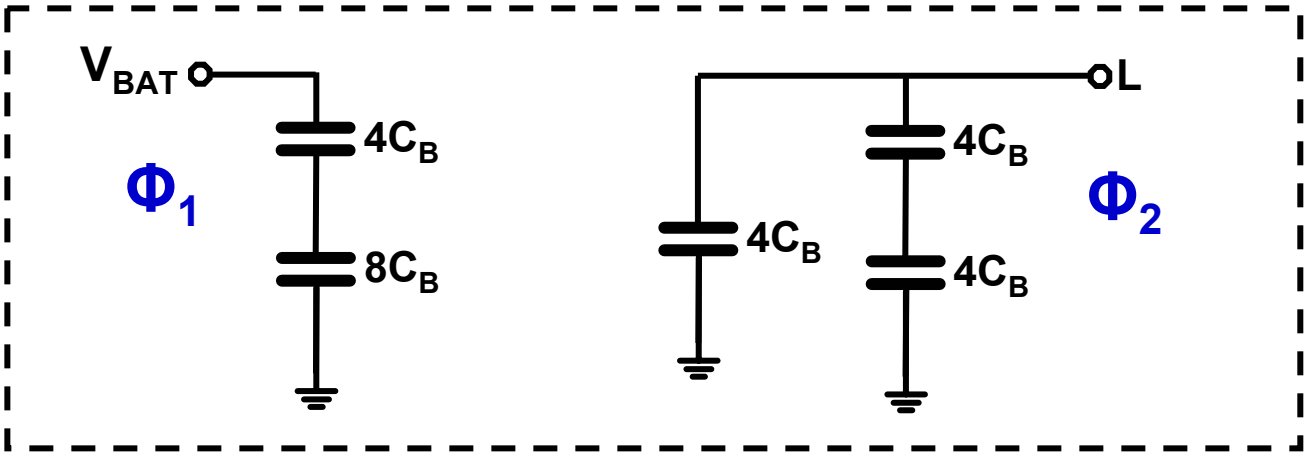
Ratio: 1/2

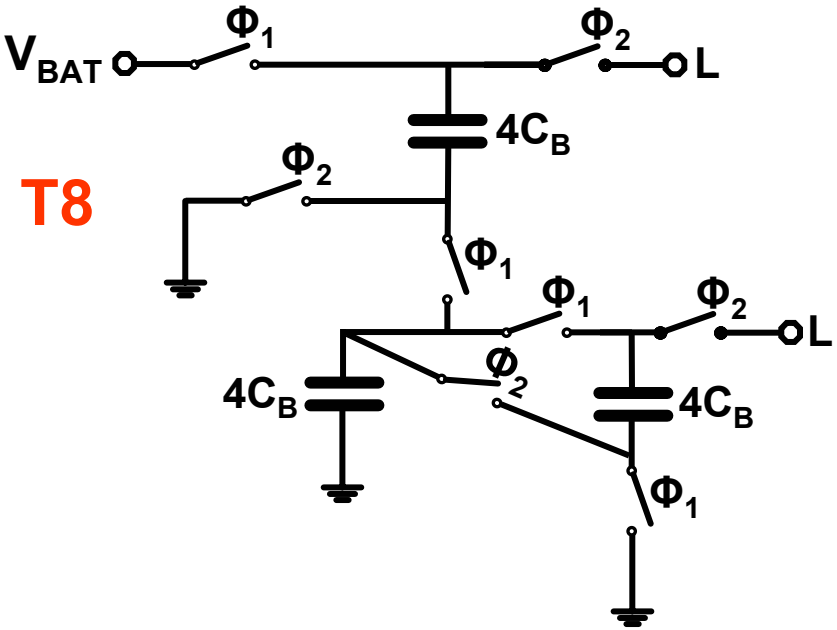


T4

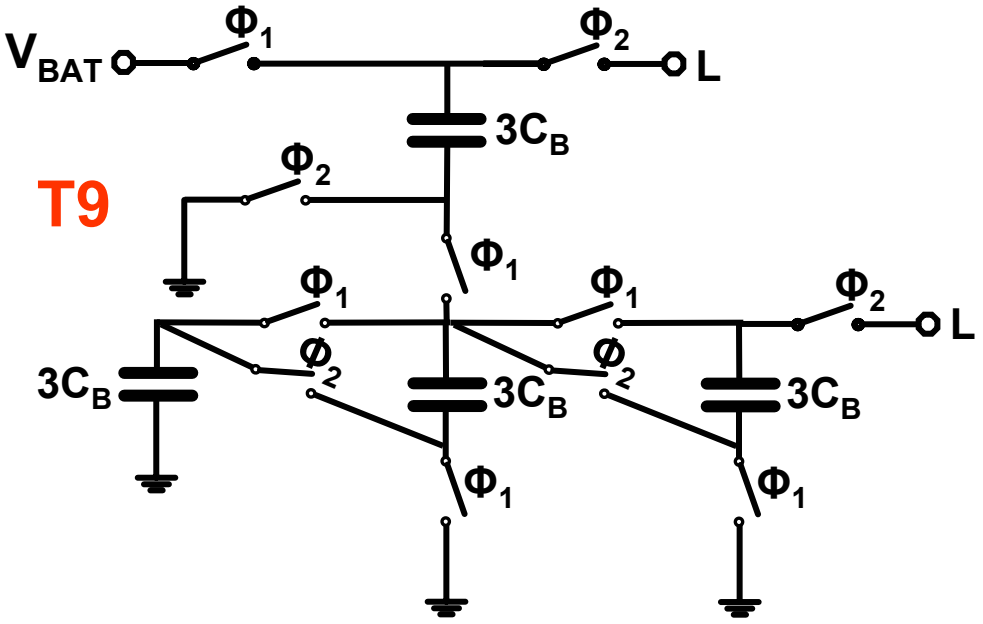
Ratio: 1/3

Scalable Voltage Generation



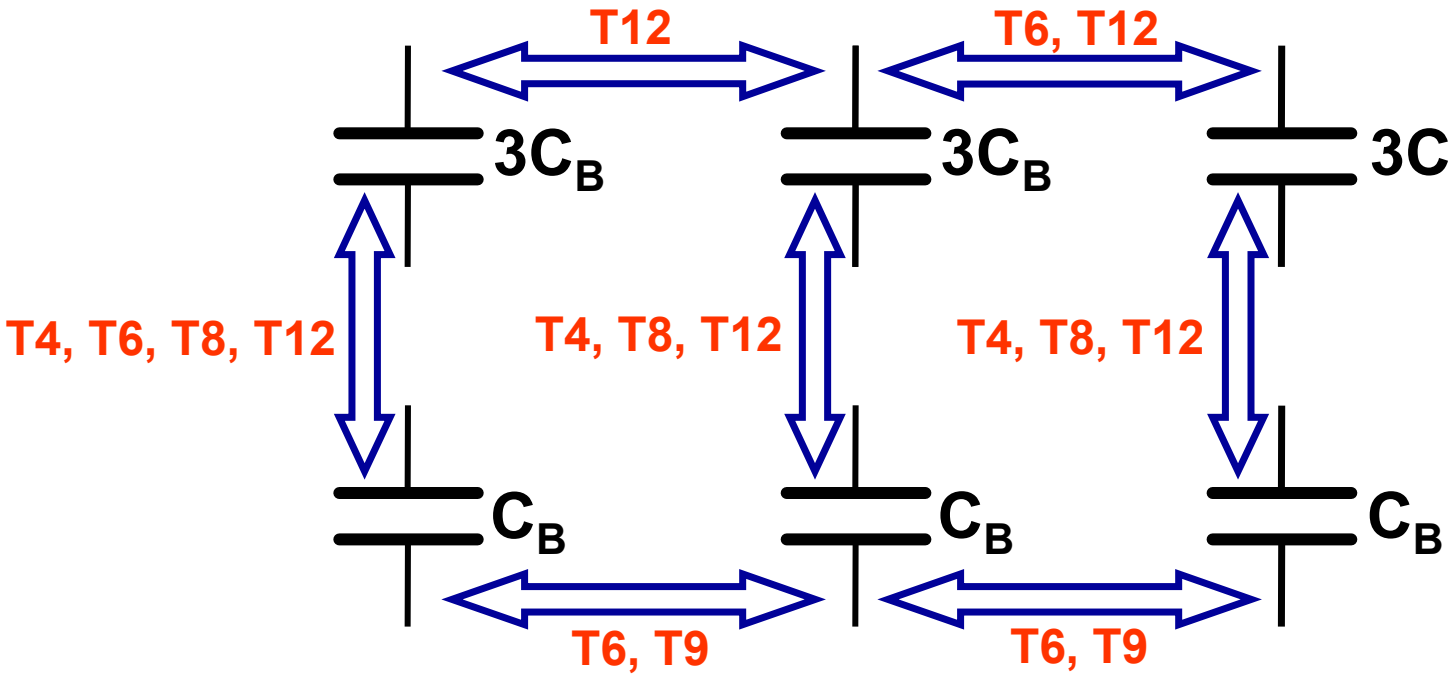


Ratio: 2/3



Ratio: 3/4

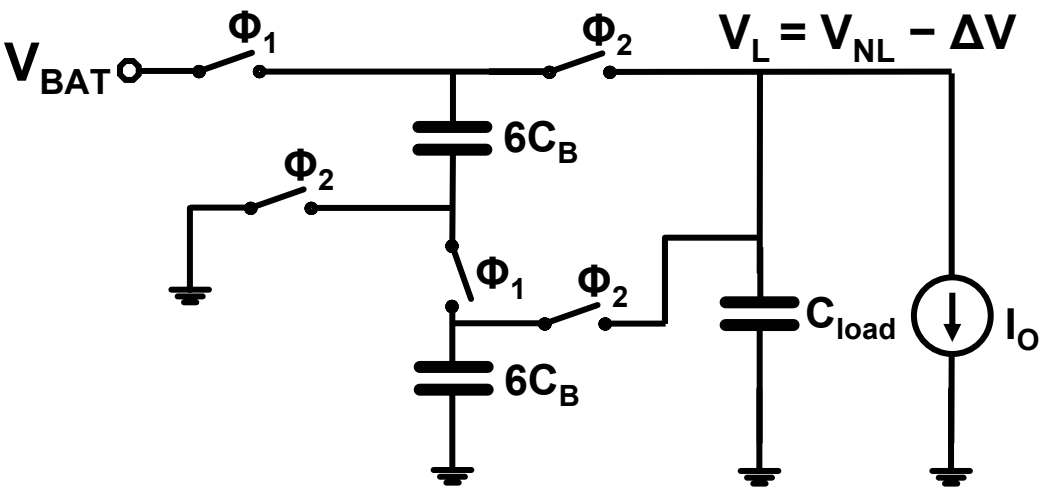
Topology Switches

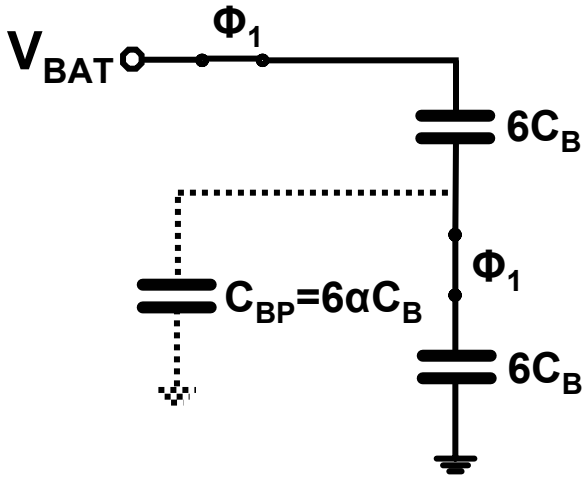


	TOP	MID	BOT	X
T12	$12C_B$	–	–	–
T9	$3C_B$	$3C_B$	$3C_B$	$3C_B$
T8	$4C_B$	$4C_B$	$4C_B$	–
T6	$6C_B$	–	$6C_B$	–
T4	$4C_B$	$4C_B$	$4C_B$	–

- Capacitor Budget = $12C_B$
- No steady-state power

Bottom Plate Parasitic Loss





$$E_B = 6C_B V_{BAT} \Delta V$$

$$E_{BP} = 6\alpha C_B \frac{V_{BAT}^2}{4}$$

$$K_p \frac{V_{BAT}}{\Delta V} = \frac{E_{BP}}{E_B} = 0.25\alpha \frac{V_{BAT}}{\Delta V}$$

Topology Dependent

Technology Dependent

Switching and Control Loss

$$E_{SW} = nC_{ox}WLV_{BAT}^2$$

$$W \sim C_B, f_s$$

$$E_{SW} = n\gamma C_B f_s V_{BAT}^2$$

$$K_s f_s \frac{V_{BAT}}{\Delta V} = \frac{E_{SW}}{E_B} = n\gamma f_s \frac{V_{BAT}}{\Delta V}$$

Topology Dependent

Technology Dependent

- γ depends on C_{ox}, μ, V_T and L (minimum channel length)

$$E_{CONT} = K_c V_{BAT}^2 + I_{leak} V_{BAT} T_{SW}$$

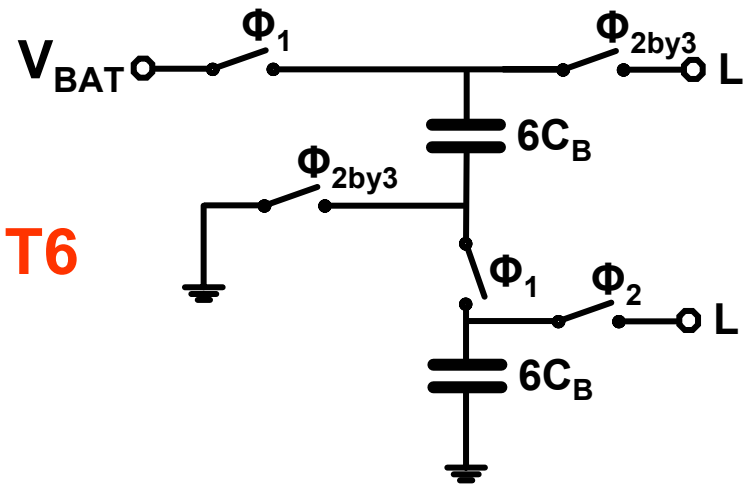
- Control loss includes switching and leakage loss in the control circuitry

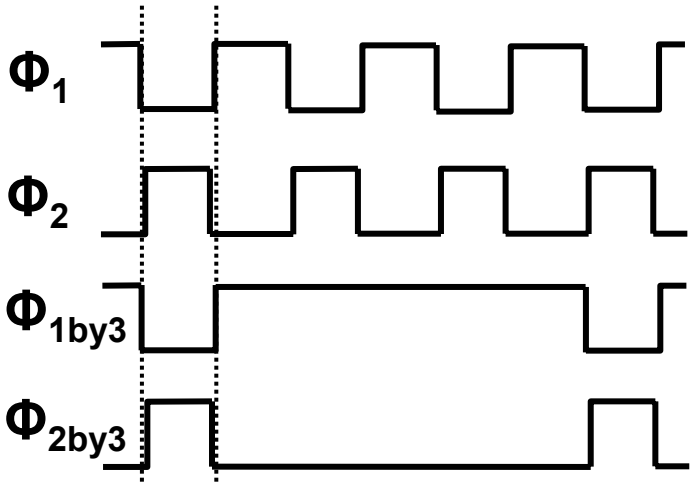
Efficiency

$$\eta_{ov} = \frac{E_L}{E_B + E_{BP} + E_{SW} + E_{CONT}} = \left(1 - \frac{\Delta V}{V_{NL}}\right)\left(\frac{1}{1 + K_p \frac{V_{BAT}}{\Delta V} + K_s f_s \frac{V_{BAT}}{\Delta V} + K_c \frac{V_{BAT}}{C_B \Delta V} + \frac{I_{leak} T_{SW}}{C_B \Delta V}}\right)$$

- Pre-factor is due to linear efficiency loss
- Contribution of other losses decrease as ΔV goes up
- There is an optimum ΔV for any given topology
- Larger C_B (more area) improves efficiency

Divide-by-3 Switching





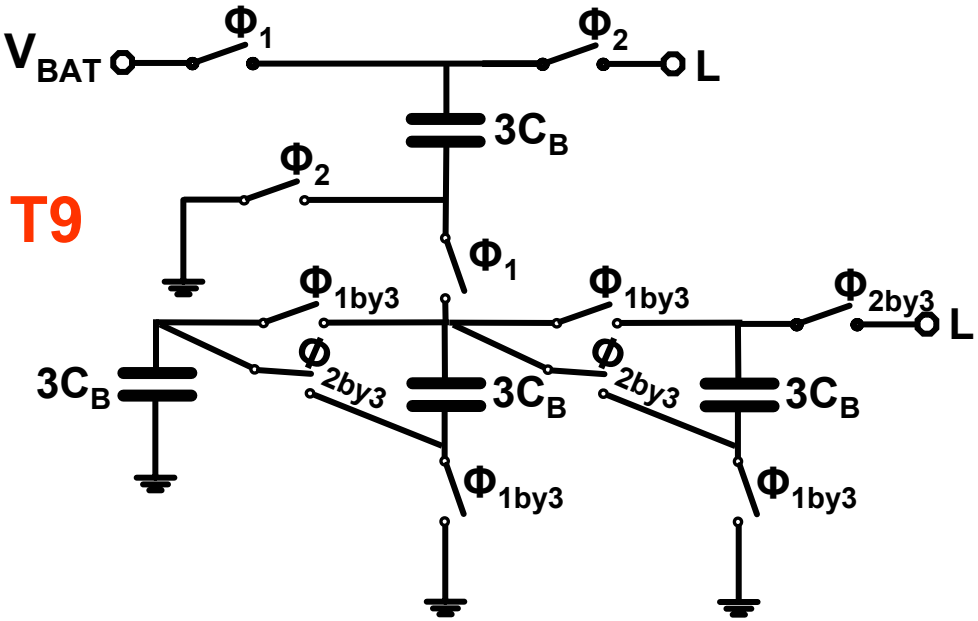
$$E_{B,3} = 6C_B V_{BAT}\left(\Delta V + \frac{\Delta V}{2} + \frac{\Delta V}{4}\right) = 6C_B V_{BAT} * 1.75\Delta V$$

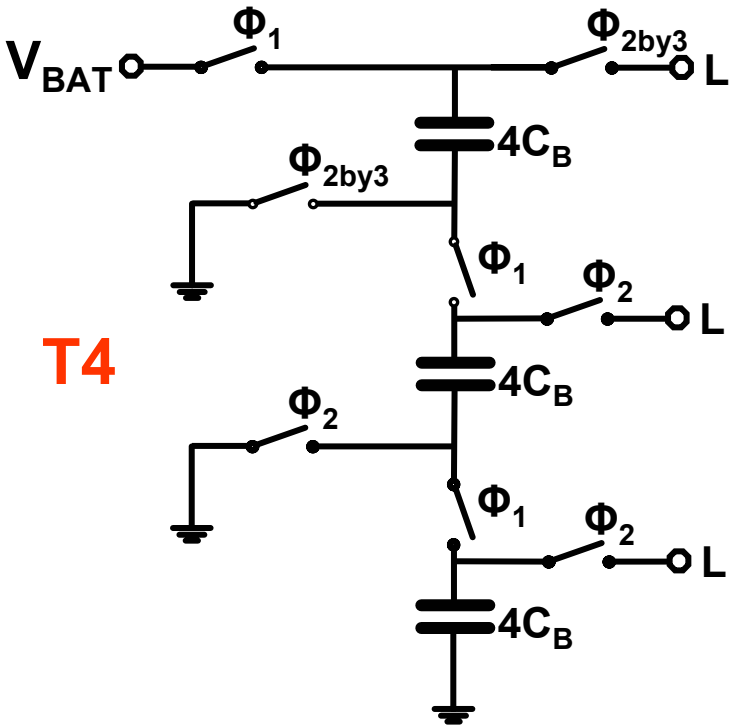
$$E_{BP,3} = \frac{6\alpha C_B V_{BAT}^{\ 2}}{4}$$

$$K_p = \frac{\alpha}{7}$$

1.75X improvement

Divide-by-3 Switching

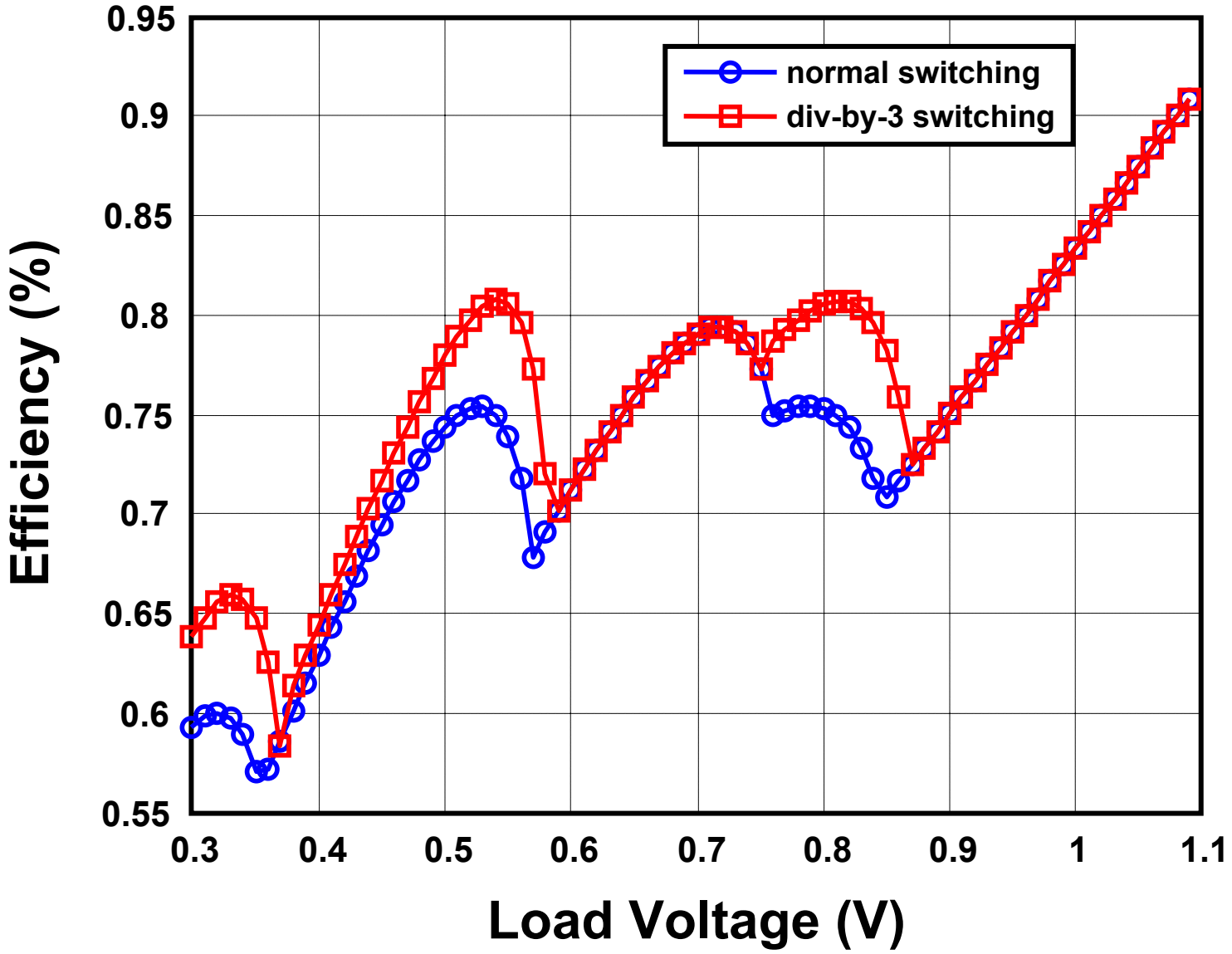




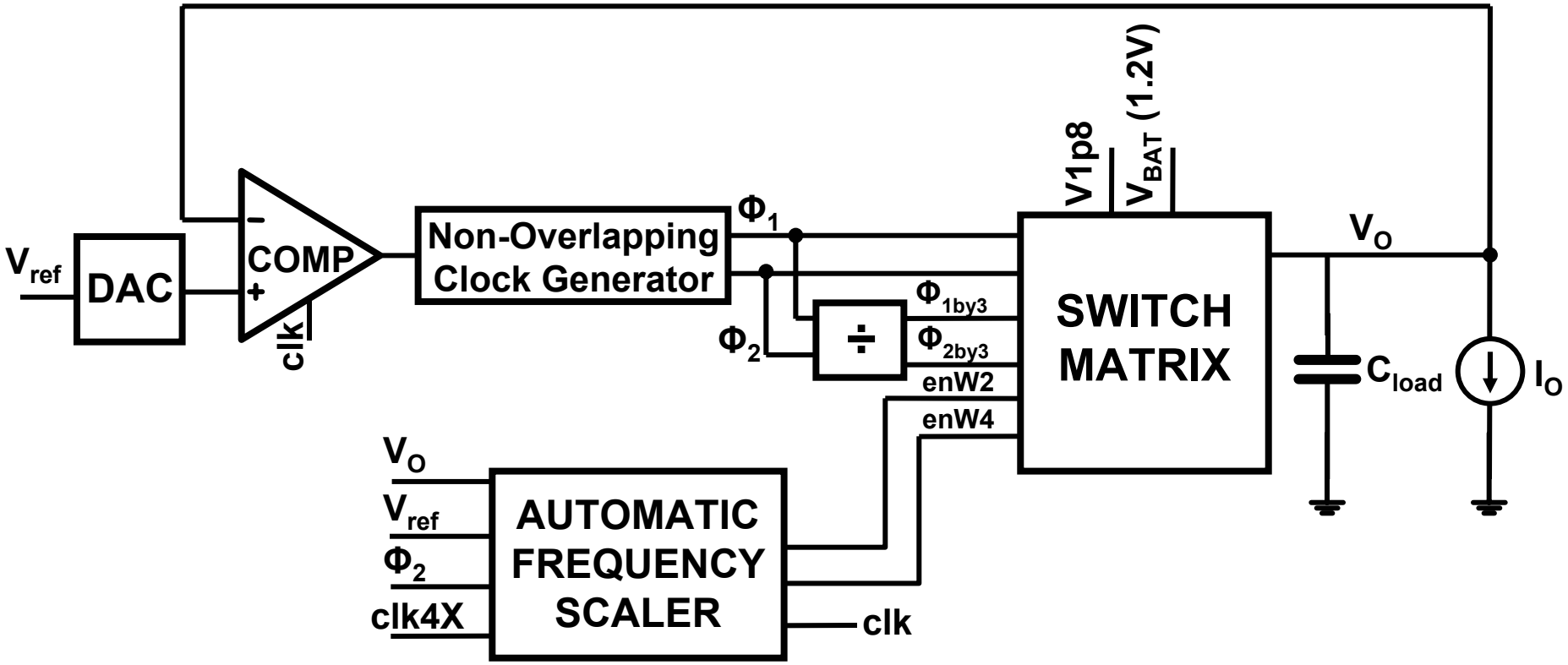
K_p improvement

Topology	K_p	K_p, divby3	Ratio	E_B	E_B, divby3
T9	0.375 α	0.216 α	1.74X	$3C_BV_{BAT}\Delta V$	$2.3C_BV_{BAT}\Delta V$
T6	0.25 α	0.141 α	1.75X	$6C_BV_{BAT}\Delta V$	$3.5C_BV_{BAT}\Delta V$
T4	0.555 α	0.368 α	1.51X	$4C_BV_{BAT}\Delta V$	$2.8C_BV_{BAT}\Delta V$

Efficiency Improvement

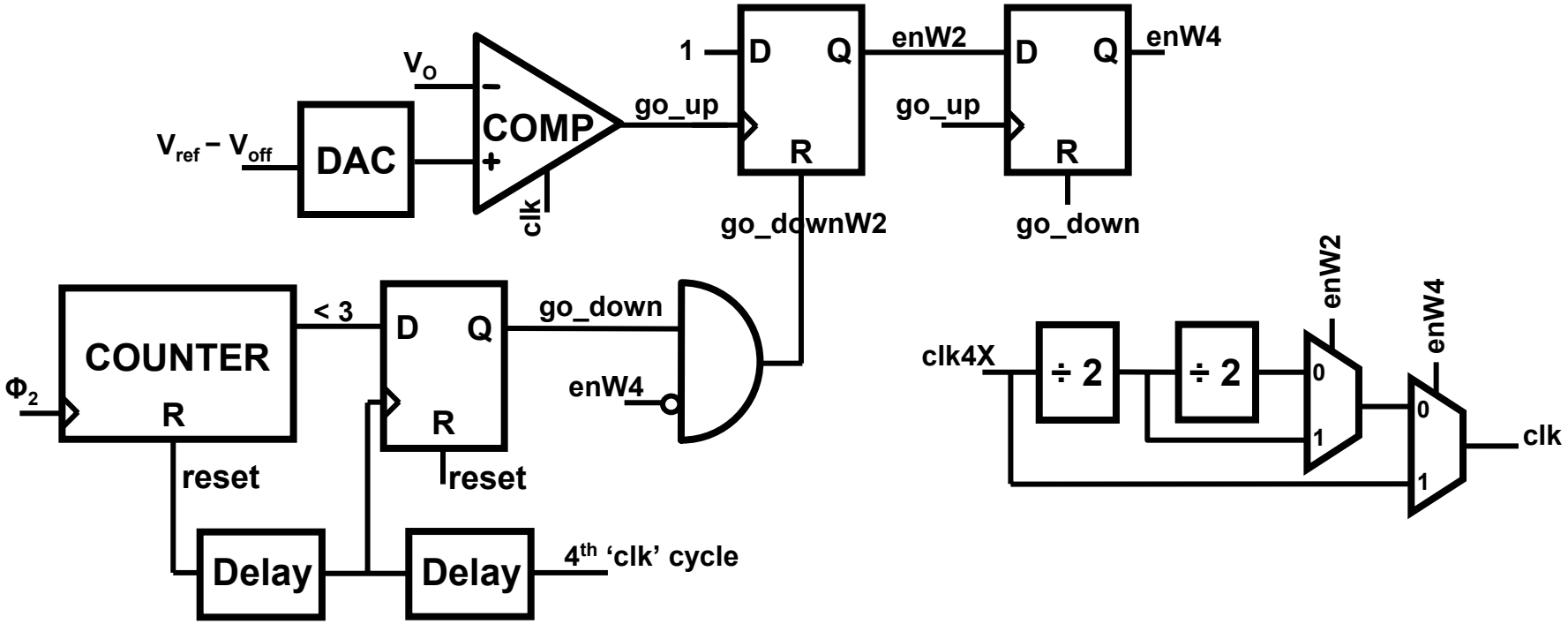


Architecture



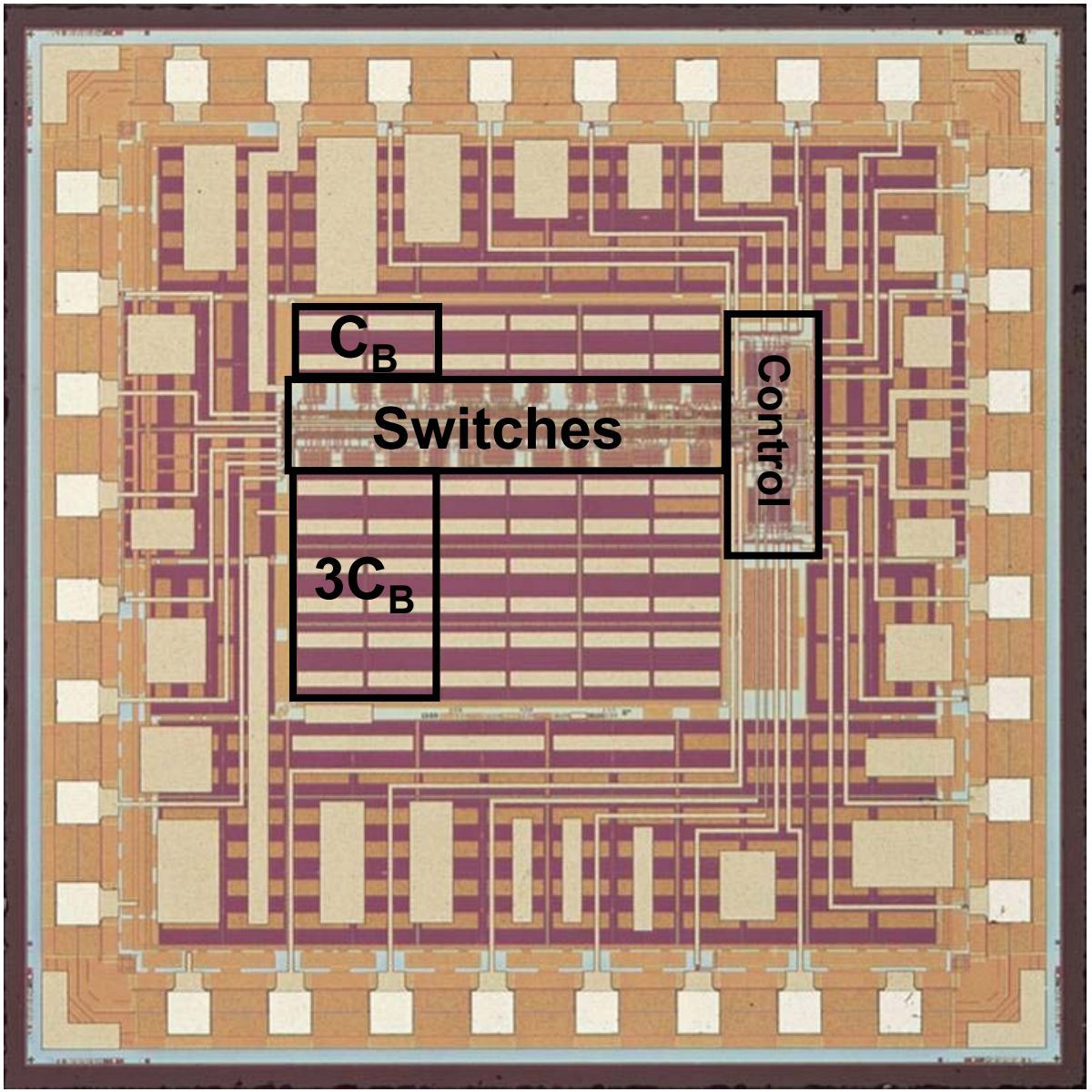
- ON-OFF mode control. V_{ref} is set digitally
- No static power loss
- Completely on-chip except for C_{load}

Automatic Frequency Scaling



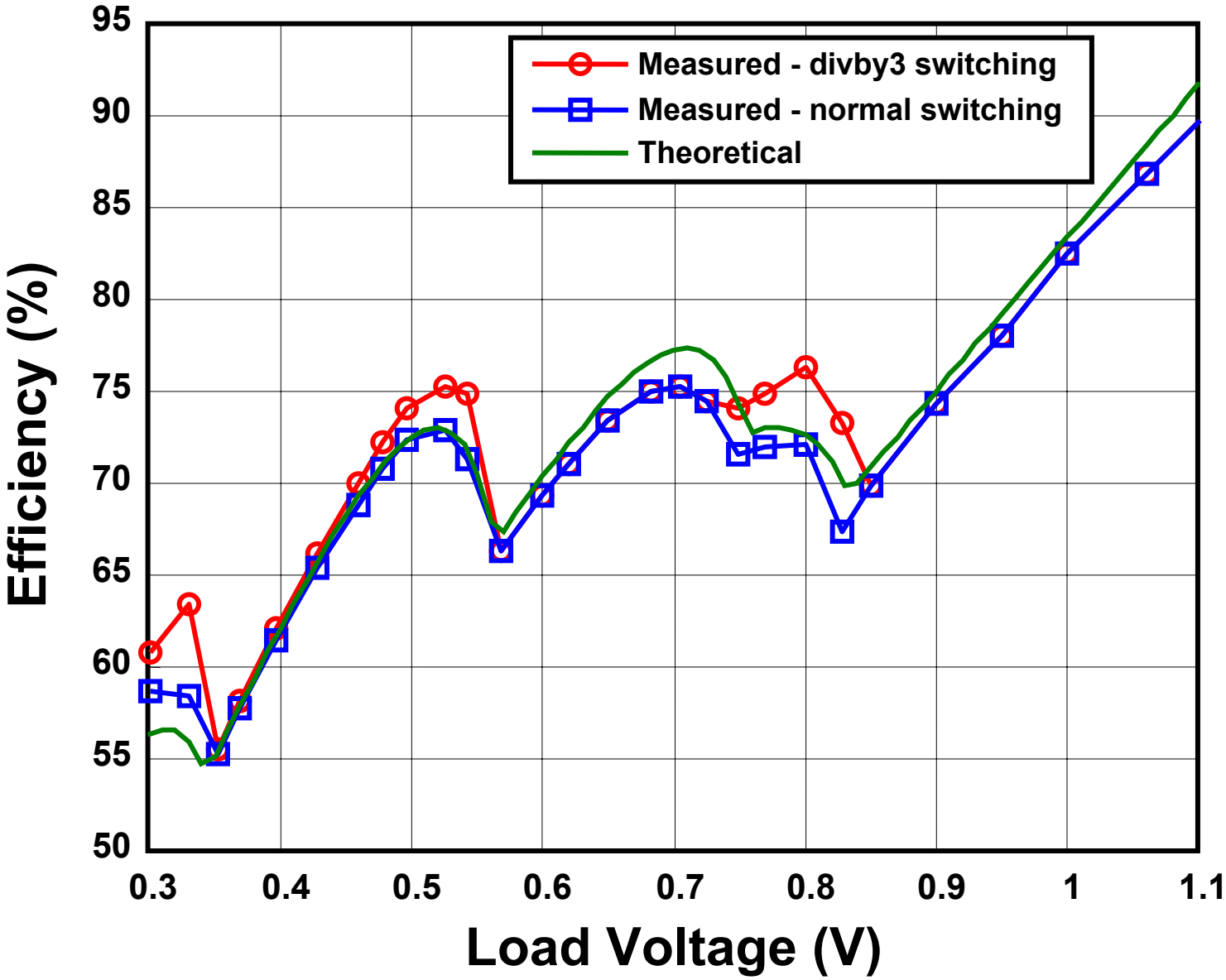
- Overload comparator is used to increase switching frequency at higher loads
- At low load, switching frequency is halved using a counter mechanism
- enW2 and enW4 determine switching frequency

Die Photo



- Die area – 1.6mm x 1.6mm
- Circuit active area – 0.57 mm^2
- Gate-oxide capacitors are used
- Total capacitance – 2.4nF

Efficiency Measurements



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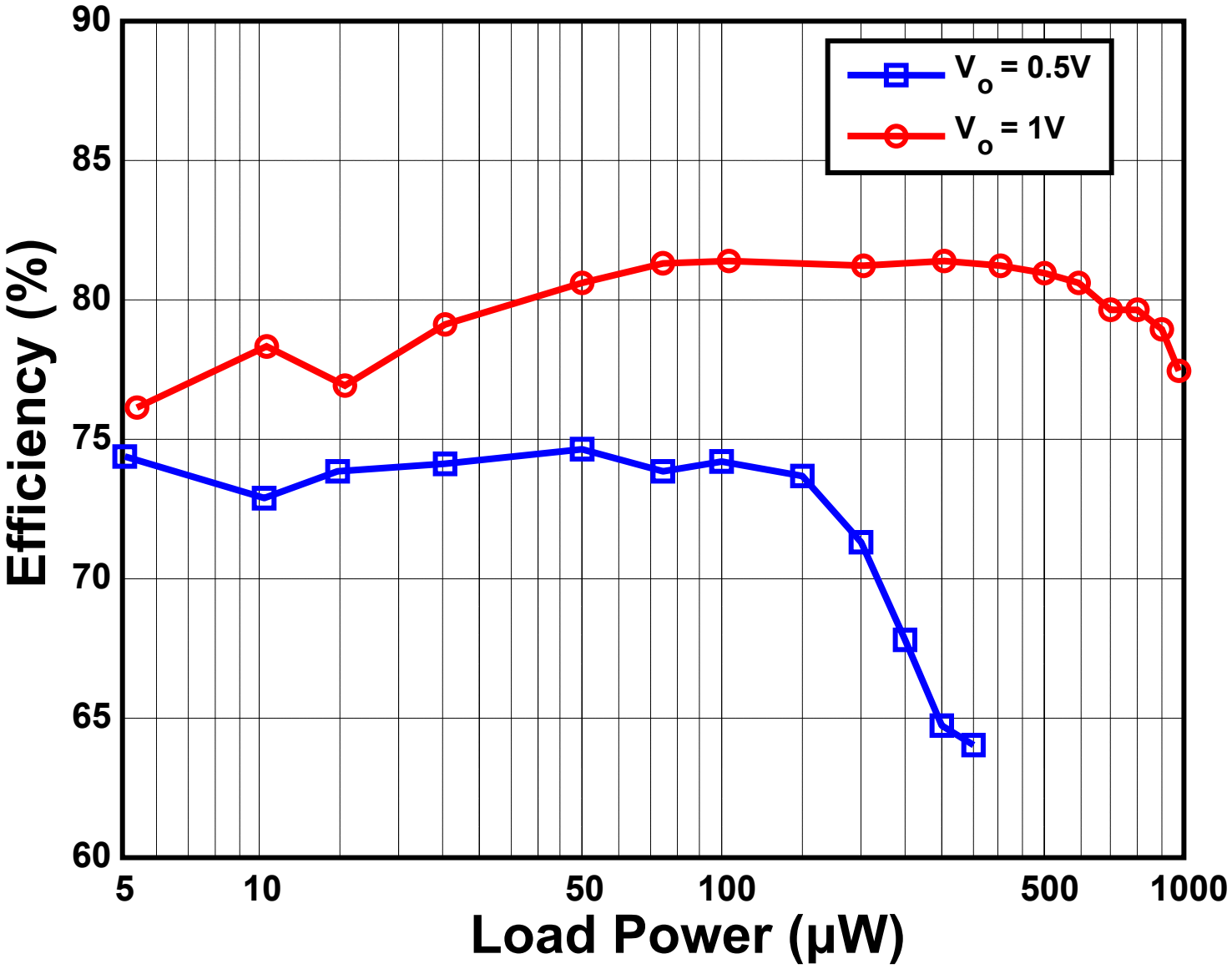
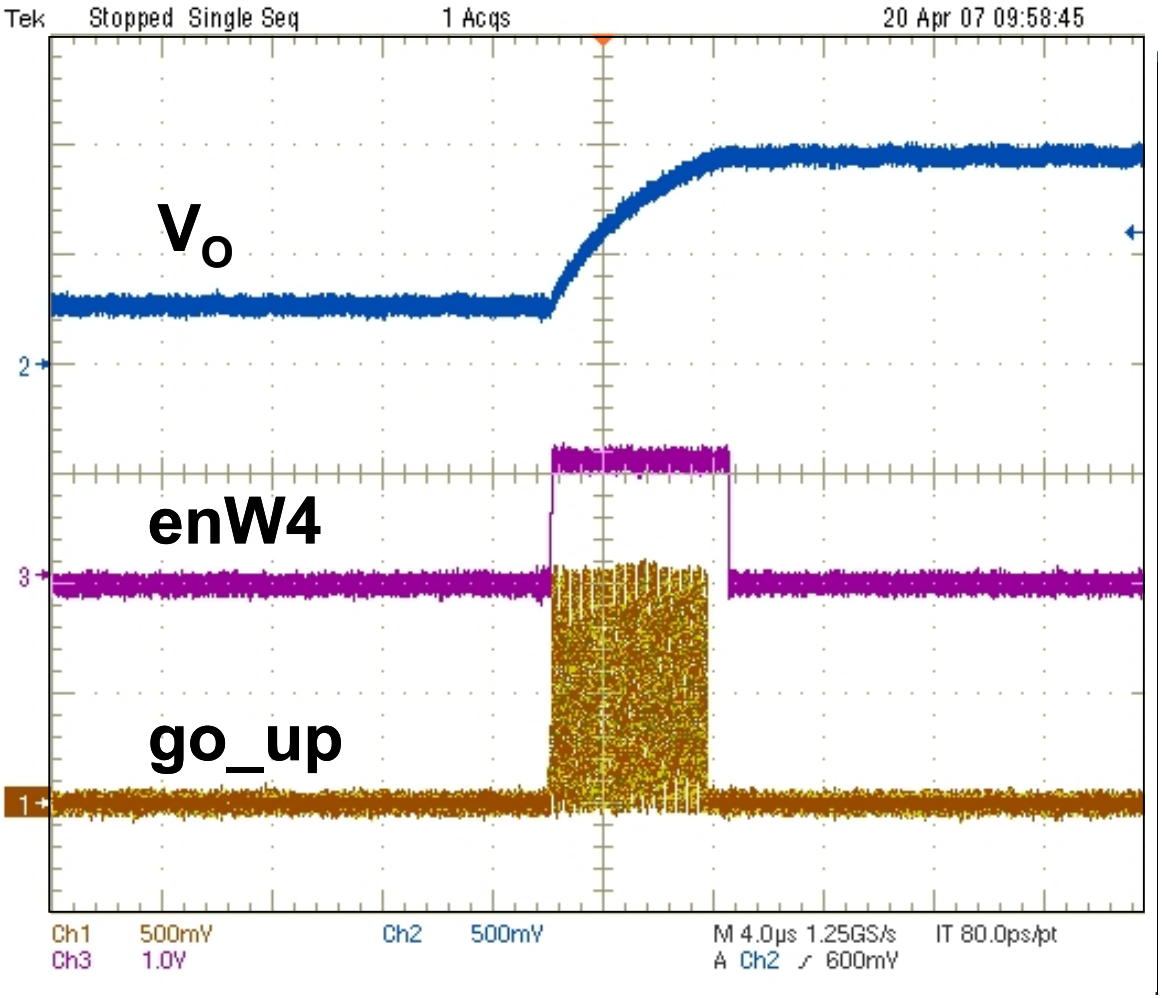


Transient Measurements



- 100 µA load, 0.3V –> 1V in 6µs
- Dead-beat transient response

Conclusions

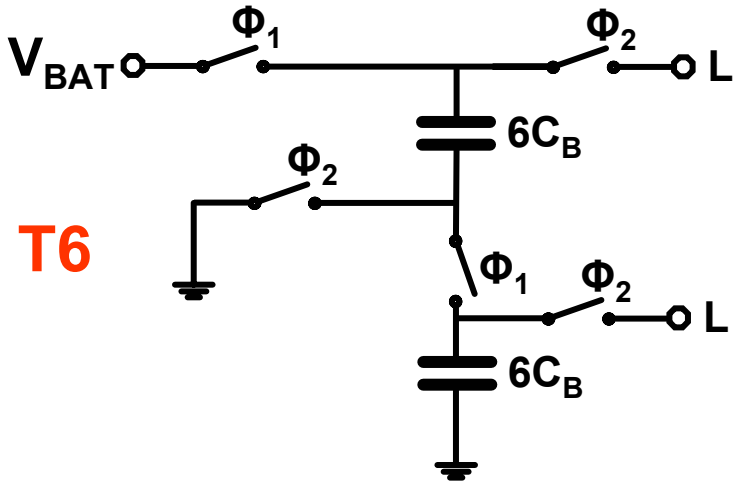
- A voltage-scalable switched capacitor DC-DC converter with on-chip charge transfer capacitors has been presented
- A new divide-by-3 switching scheme has been proposed to address bottom-plate parasitic loss
- Completely digital control with very little control power overhead
- A very scalable system that can be changed to meet the load voltage and power needs

Acknowledgements: Funding provided by DARPA,

Chip fabrication provided by National Semiconductor

Power Delivery

$V_L = V_{BAT}/2 - \Delta V$



$$E_B = 6C_B V_{BAT} \Delta V$$

$$E_L = E_B \frac{V_{NL} - \Delta V}{V_{NL}} = 12C_B V_L \Delta V$$

$$P_L = 12C_B V_L \Delta V f_s = E_B f_s \eta_{lin}$$

- Larger ΔV –> Higher power delivery
- Power delivered to the load depends on the topology and load voltage

Topology	E_B	η_{lin}
T12	$12C_B V_{BAT} \Delta V$	V_L / 1.2
T9	$3C_B V_{BAT} \Delta V$	V_L / 0.9
T8	$4C_B V_{BAT} \Delta V$	V_L / 0.8
T6	$6C_B V_{BAT} \Delta V$	V_L / 0.6
T4	$4C_B V_{BAT} \Delta V$	V_L / 0.4