

JouleTrack - A Web Based Tool for Software Energy Profiling

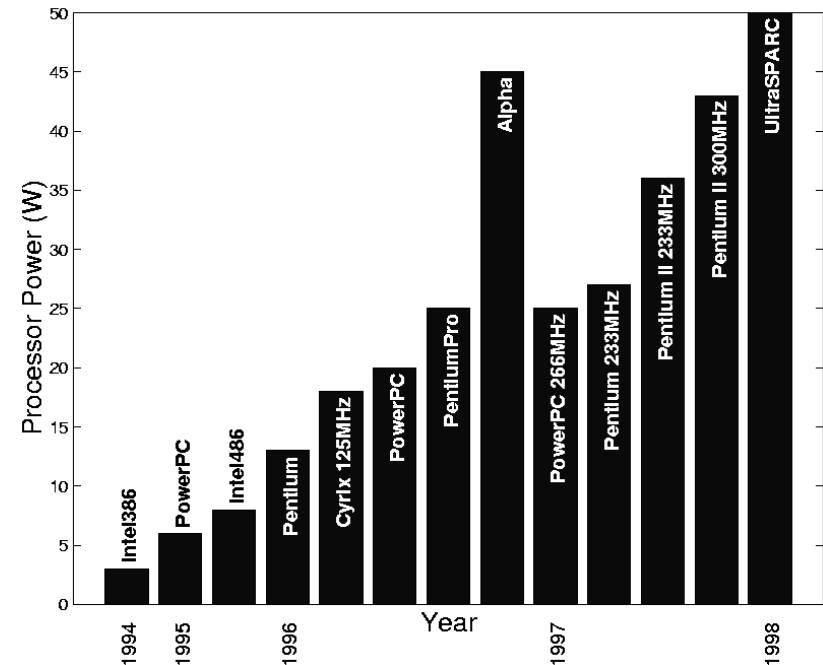
**Amit Sinha and Anantha Chandrakasan
Massachusetts Institute of Technology**

June 19, 2001

Outline

- **Motivation for fast software energy profiling**
- **Experimental setup – StrongARM and SH-4**
- **Current profiling measurements and implications**
 - ◆ **Instruction level**
 - ◆ **Program level**
 - ◆ **Models**
- **Leakage energy estimation methodology**
 - ◆ **Processor leakage model**
 - ◆ **Leakage vs. switching**
- **JouleTrack design**
- **Conclusions**

Motivation

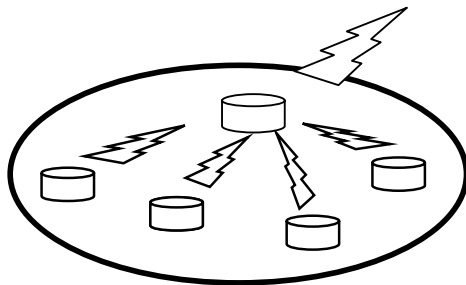


- Proliferation of portable devices
 - ◆ 50X increase in μ P power vs. 4X in battery life
 - ◆ Battery technology lags behind
- Programmable solutions preferred
 - ◆ Fast software profiling techniques required

Scenarios



- Portable devices downloading apps
- Predictive energy estimation

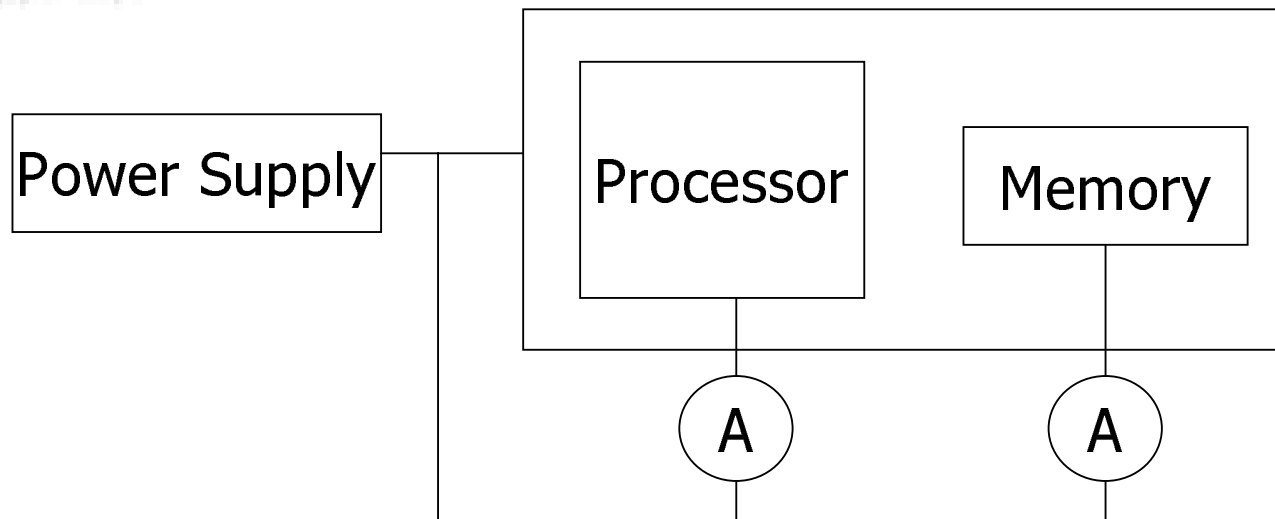


- Wireless sensor networks
- Lifetime estimation
- Energy-Quality tradeoffs



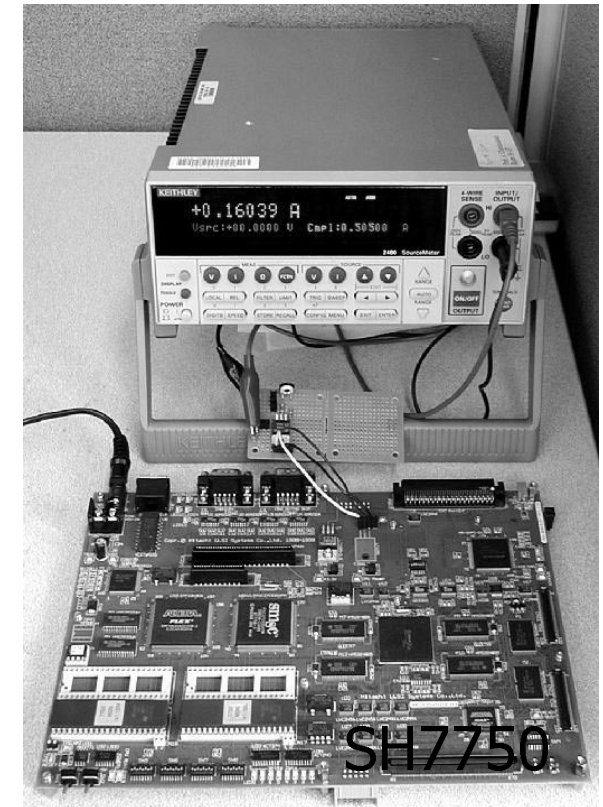
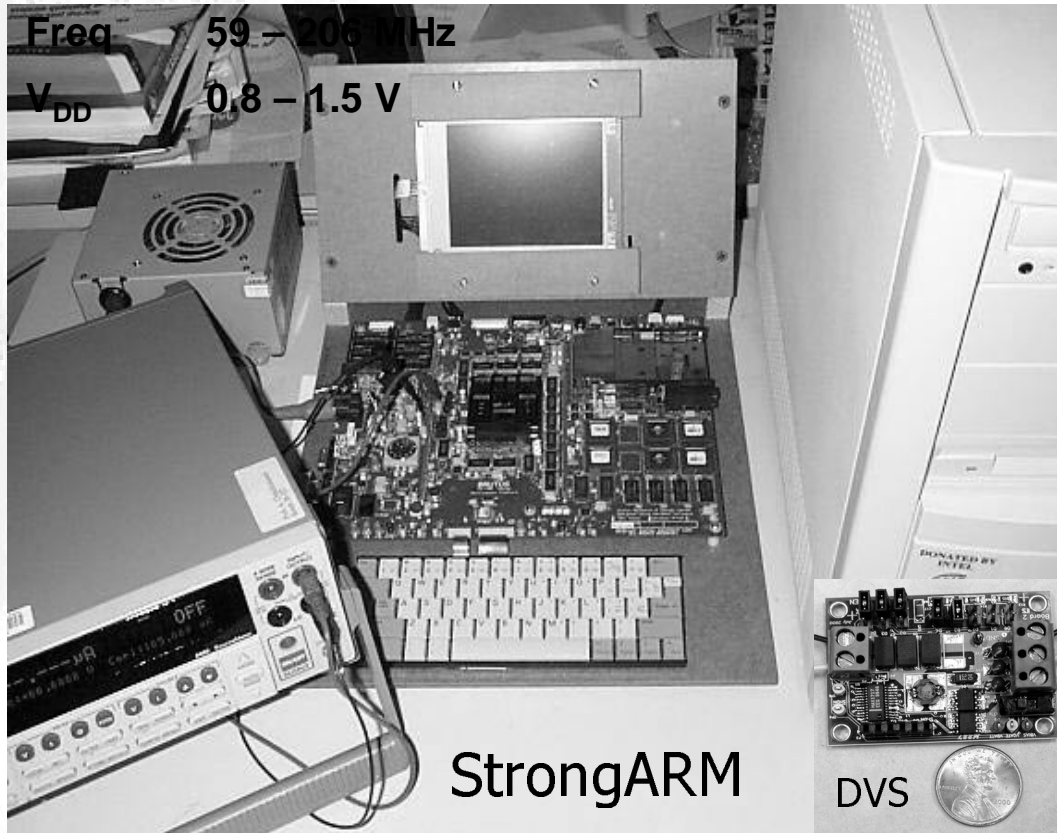
- Integrated Development Environments
- Energy aware software

Software Energy Estimation



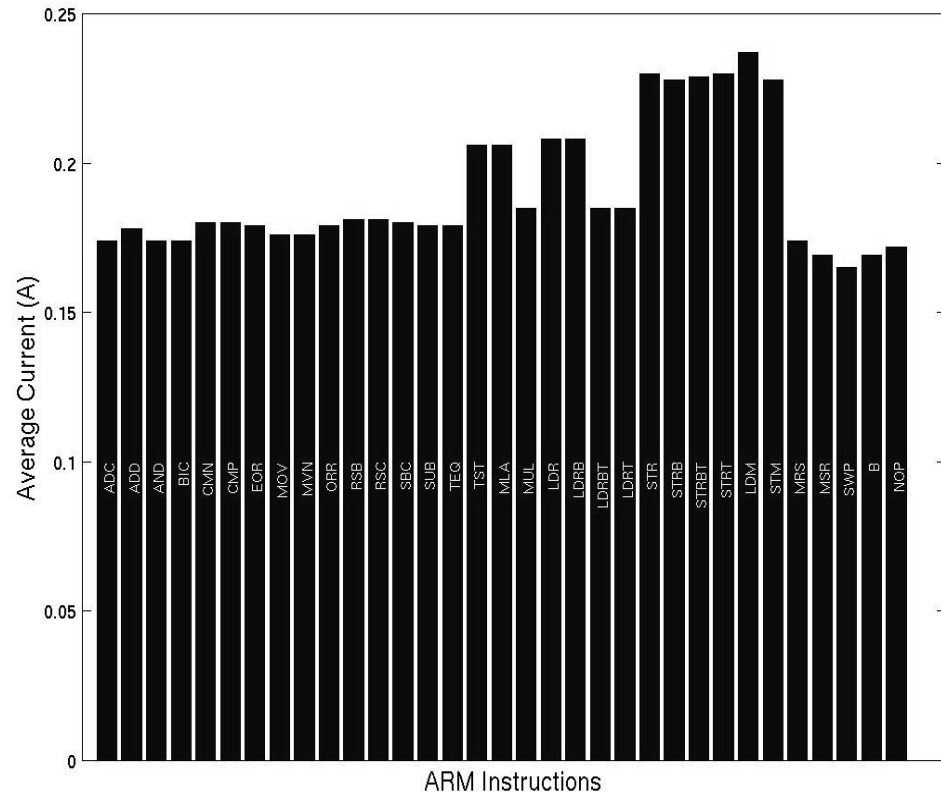
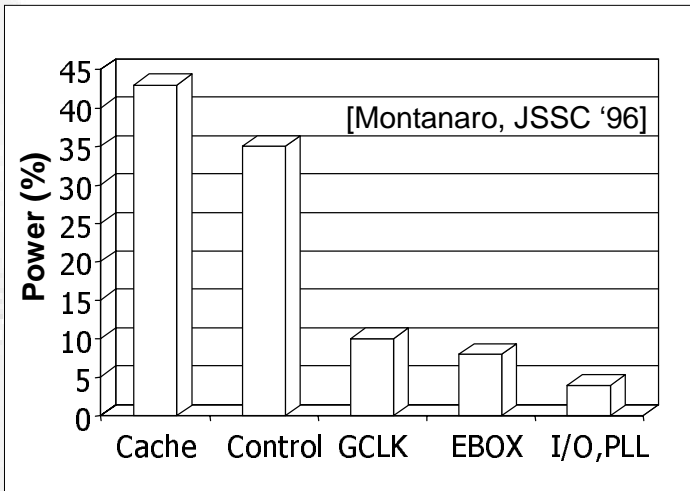
- **[Tiwari96] proposed instruction level analysis**
- **Disadvantages**
 - ◆ **Tedious instruction level analysis**
 - ◆ **Large simulation time and storage requirement**
 - ◆ **Very fine grained**
- **Macro-estimation?**

Experimental Setup



- Intel StrongARM SA-1100 Brutus platform
- Hitachi SH-4 based SH7750 platform

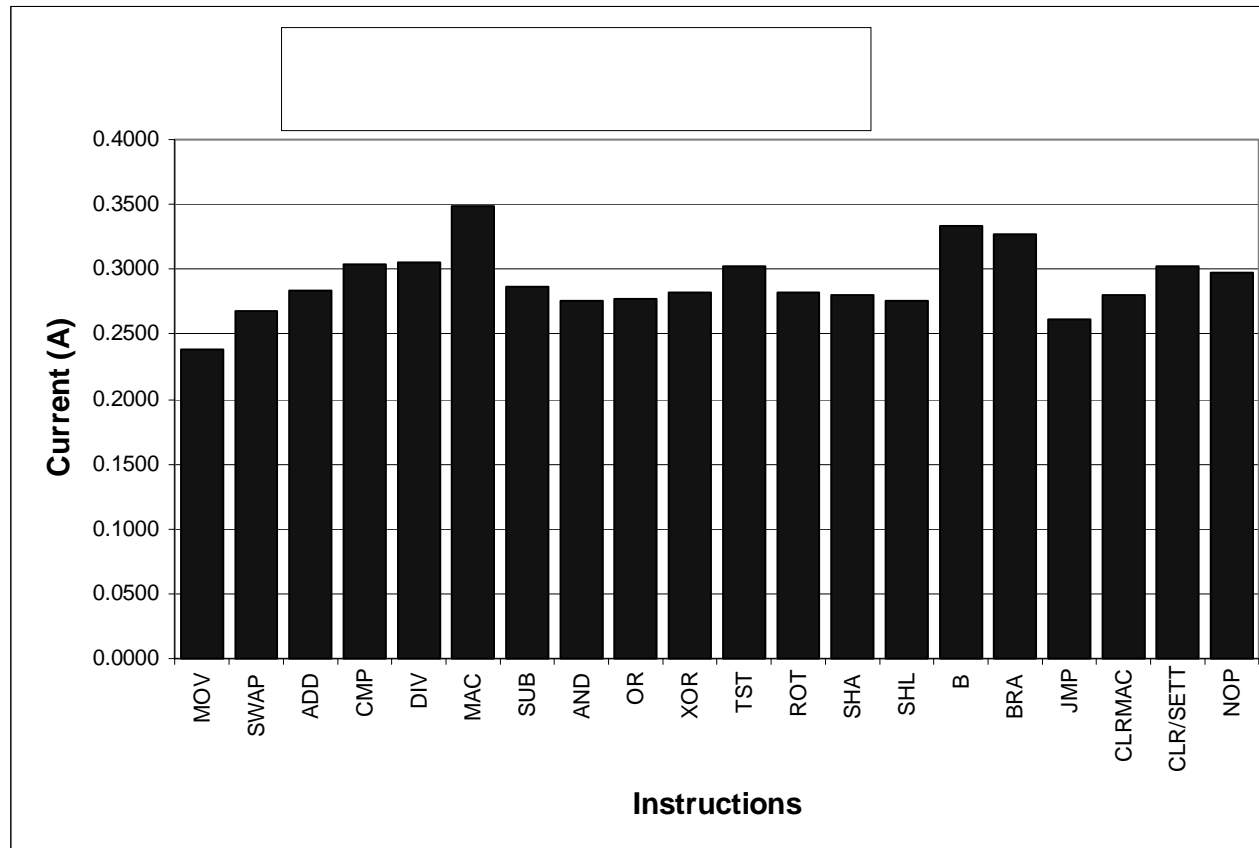
SA-1100 Instruction Current



Supply V_{DD} **1.5 V**
Frequency **206 MHz**
Load/Store **0.196 A**
ALU **0.178 A**

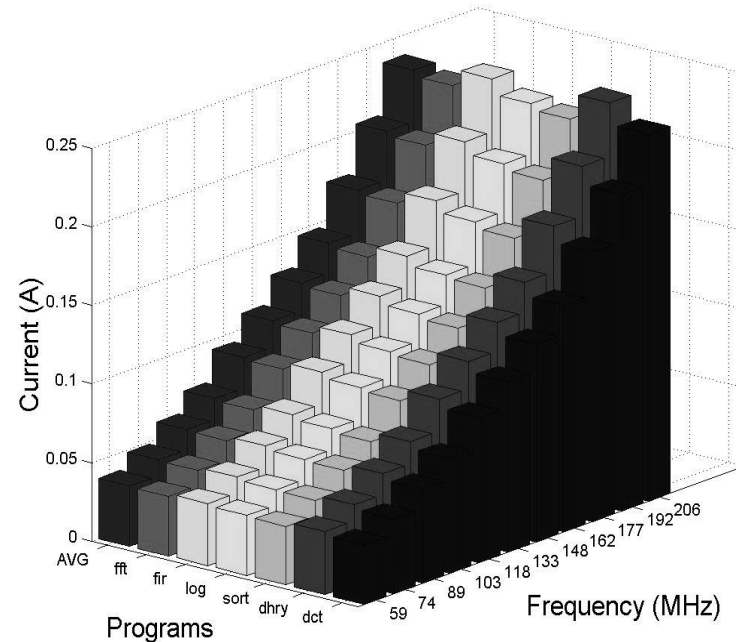
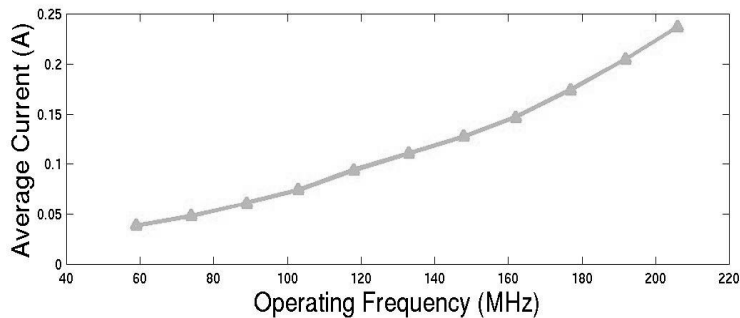
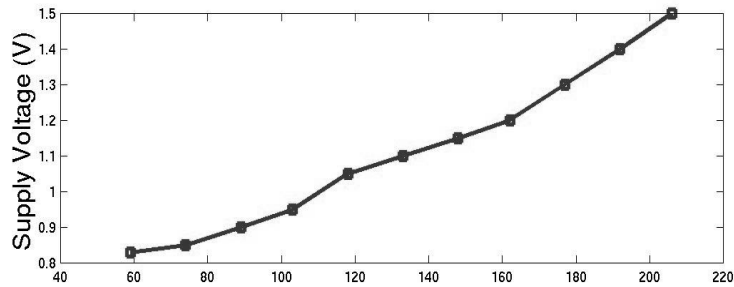
■ Little variation in instruction currents!

SH-4 Instruction Currents



- **Similar variation with MACs and Branches consuming more current**

Program Current for SA-1100



- **Current almost independent of program!**
- **First order model, $I = f(V_{DD}, \text{frequency})$**

Second Order Estimation

- Determine *energy differentiated instruction classes* and weights for those classes

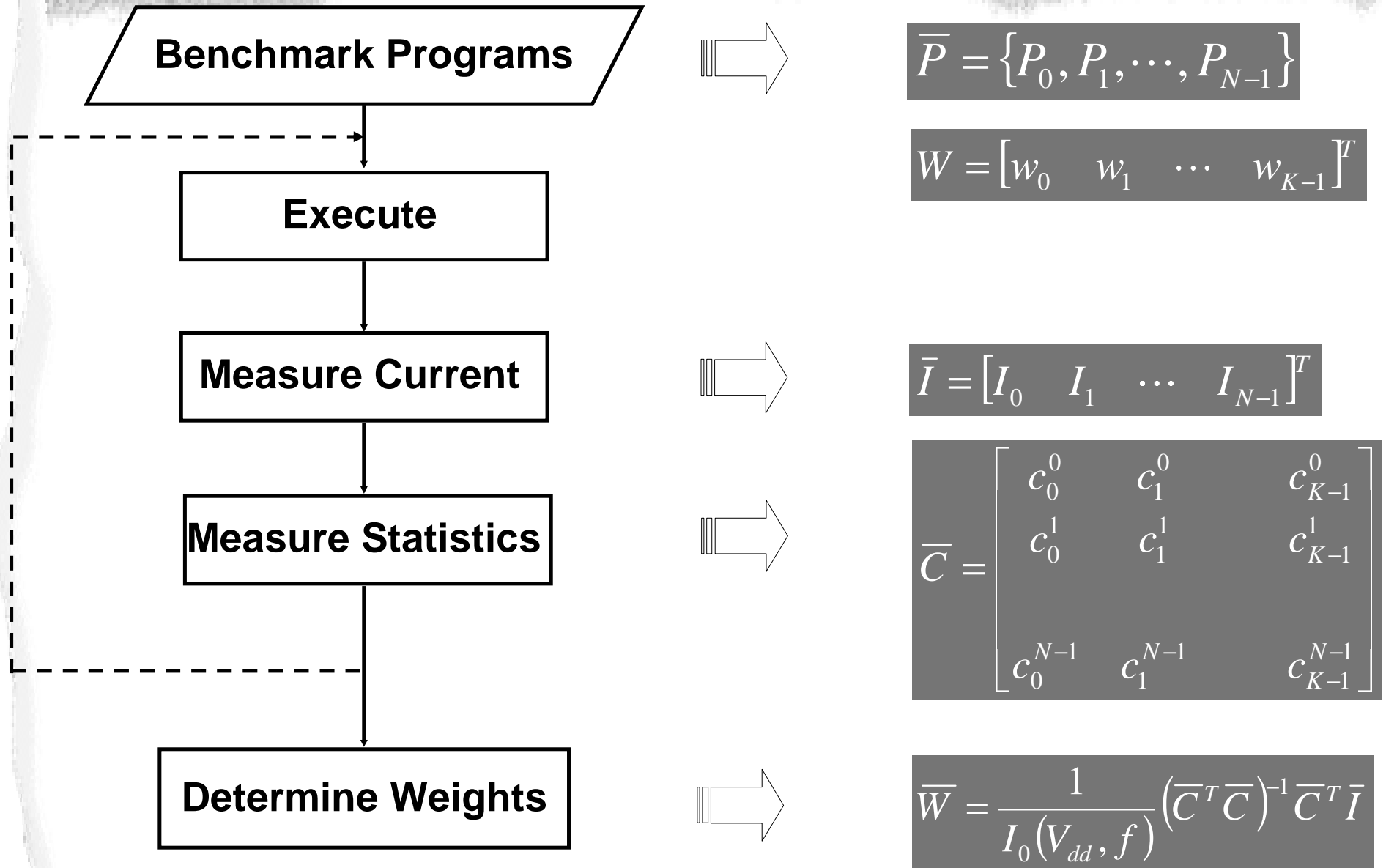
SA-1100 Example

Class	Weight
Instruction	2.17
Sequential Memory access	0.03
Non-sequential Memory access	1.24
Internal	0.84

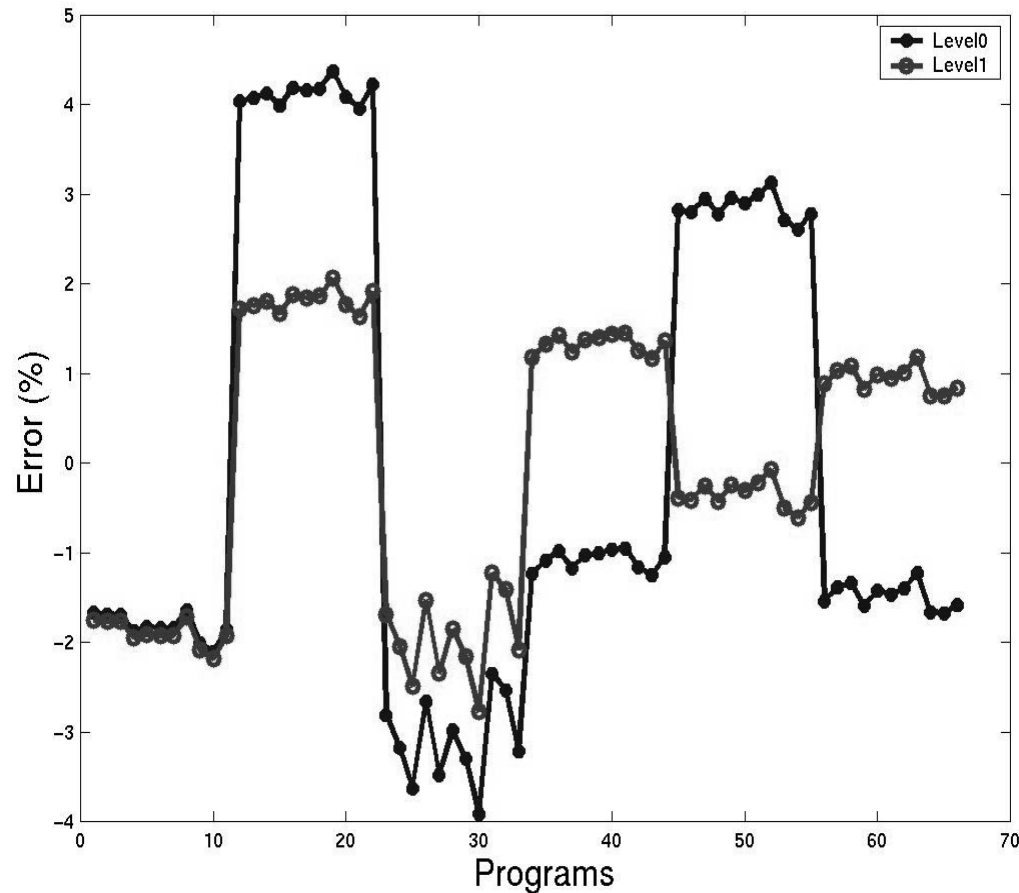
$$I(V_{DD}, f) = I_0(V_{DD}, f) \sum_{k=0}^{K-1} w_k C_k$$

- Measure statistics for those classes at runtime
- Program current = Weighted average
- Error < 3%

Model Calibration

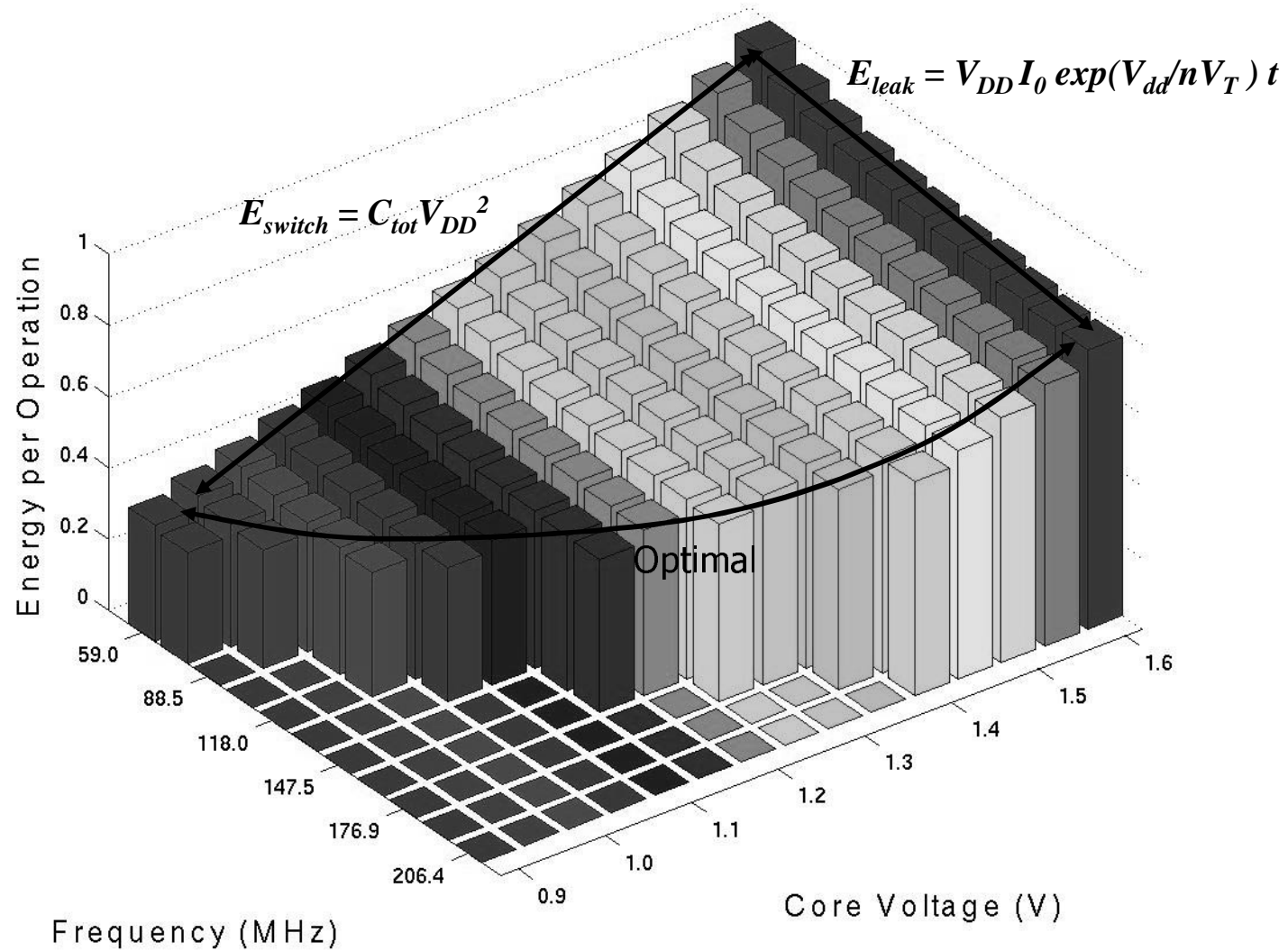


First and Second Order Models

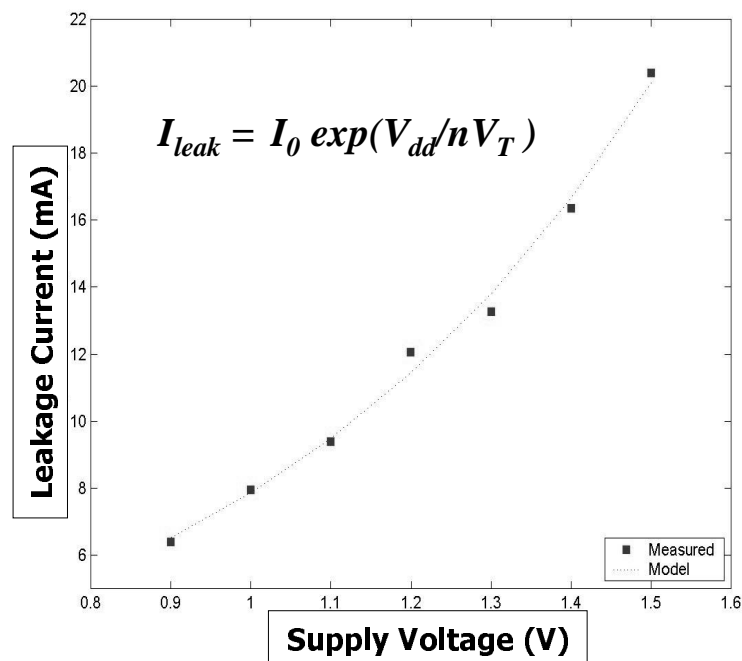
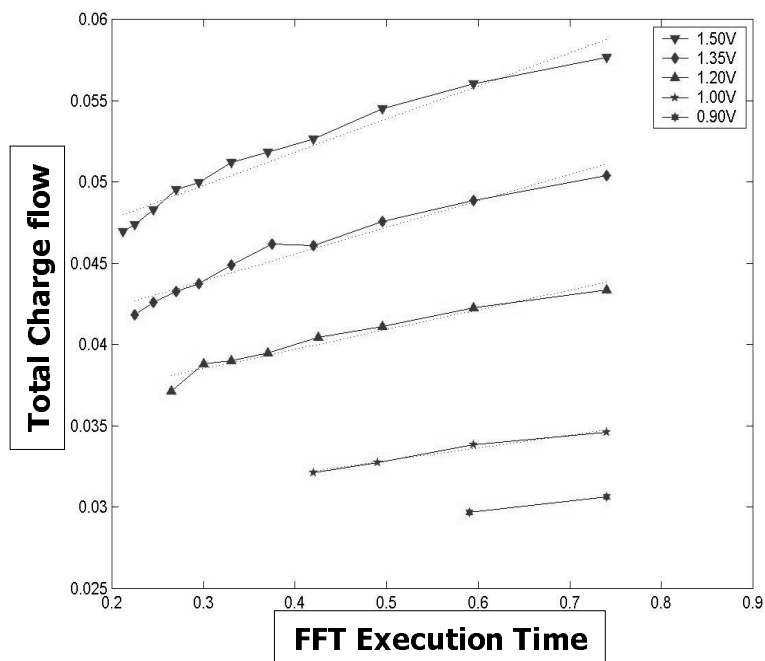


- Second order model reduces average error to 2.8% (based on 66 test programs)

Voltage Frequency Variation



Leakage Model



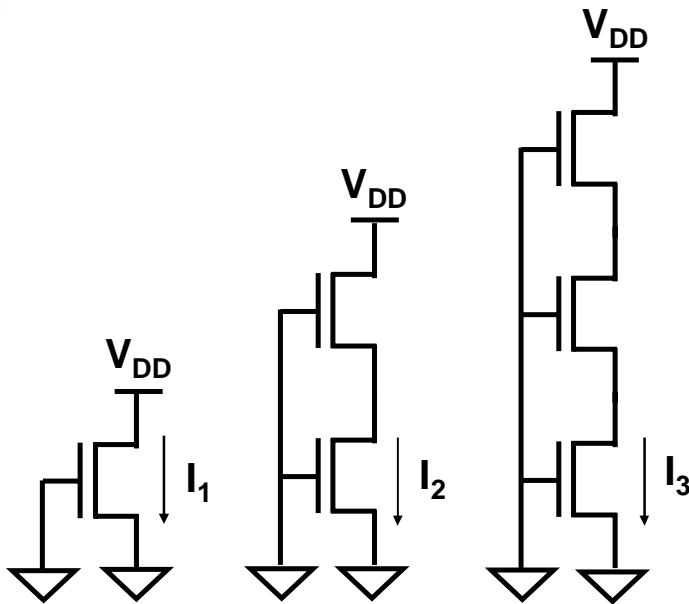
- Leakage currents account for 10% of energy dissipation
- Leakage behavior is exponential with supply voltage
- $I_0 = 1.2\text{mA}$, $n = 21.3$ for the StrongARM

Explanation of Exponential Model

$$I = A e^{\frac{(V_{GS} - V_{th0} - \gamma V_S - \eta V_{DS})}{nV_T}} \left(1 - e^{-\frac{V_{DS}}{V_T}} \right)$$

$$A = \mu_0 C_{ox} \frac{W_{eff}}{L_{eff}} V_T^2 e^{1.8}$$

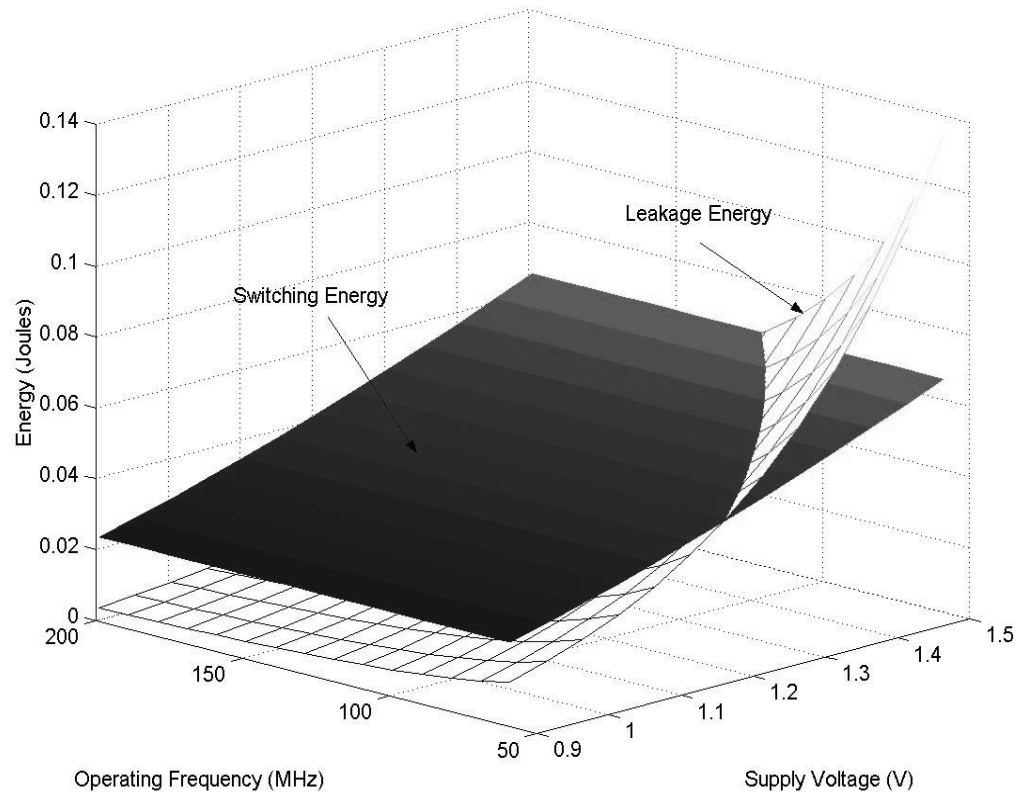
Vdd (V)	I _{leak} (mA)		Error (%)
	Measured	Model	
1.5	20.41	20.10	1.5
1.4	16.35	16.65	-1.8
1.3	13.26	13.80	-4.0
1.2	12.07	11.43	5.3
1.1	9.39	9.47	-0.9
1.0	7.96	7.85	1.4
0.9	6.39	6.53	-1.7



- Processor leakage model can be explained from transistor subthreshold leakage model
- Model error < 6%

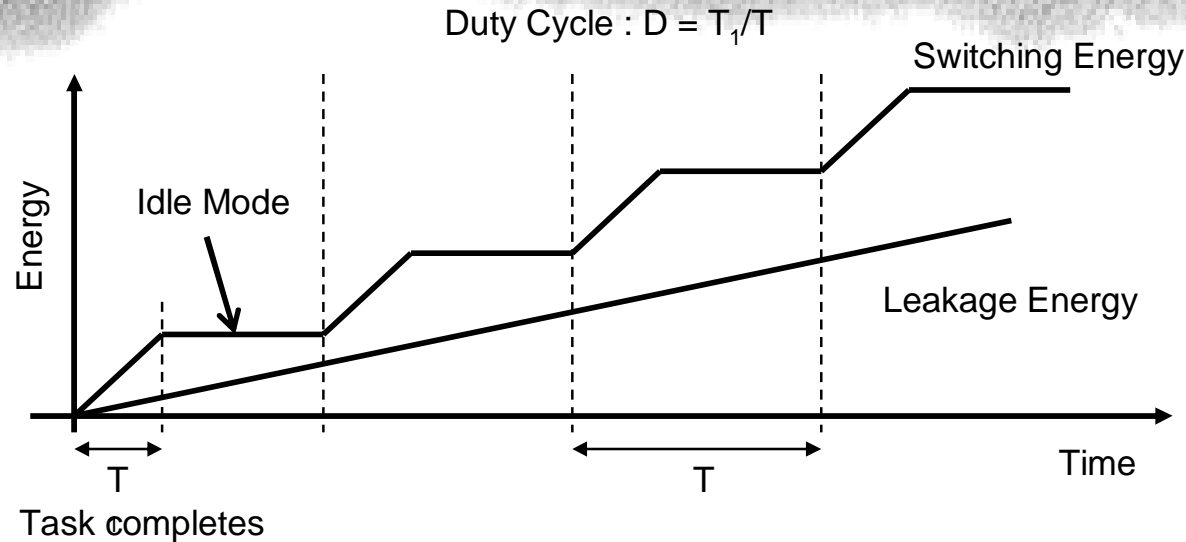
$$I_1 : I_2 : I_3 = 1.8 e^{\frac{\eta V_{DD}}{nV_T}} : 1.8 : 1 \quad [\text{Gu96}]$$

Isolating Leakage Energy

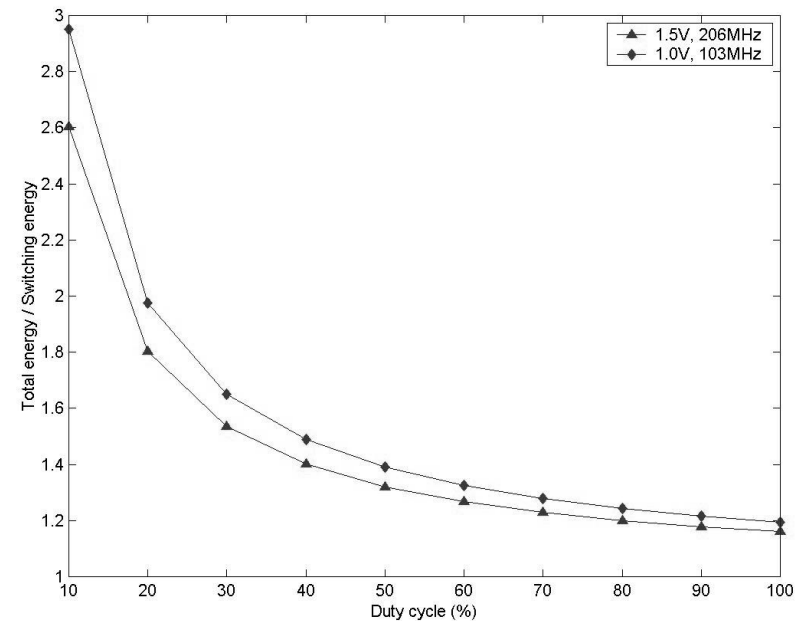


- Leakage energy component can dominate switching energy for high supply voltage operation!

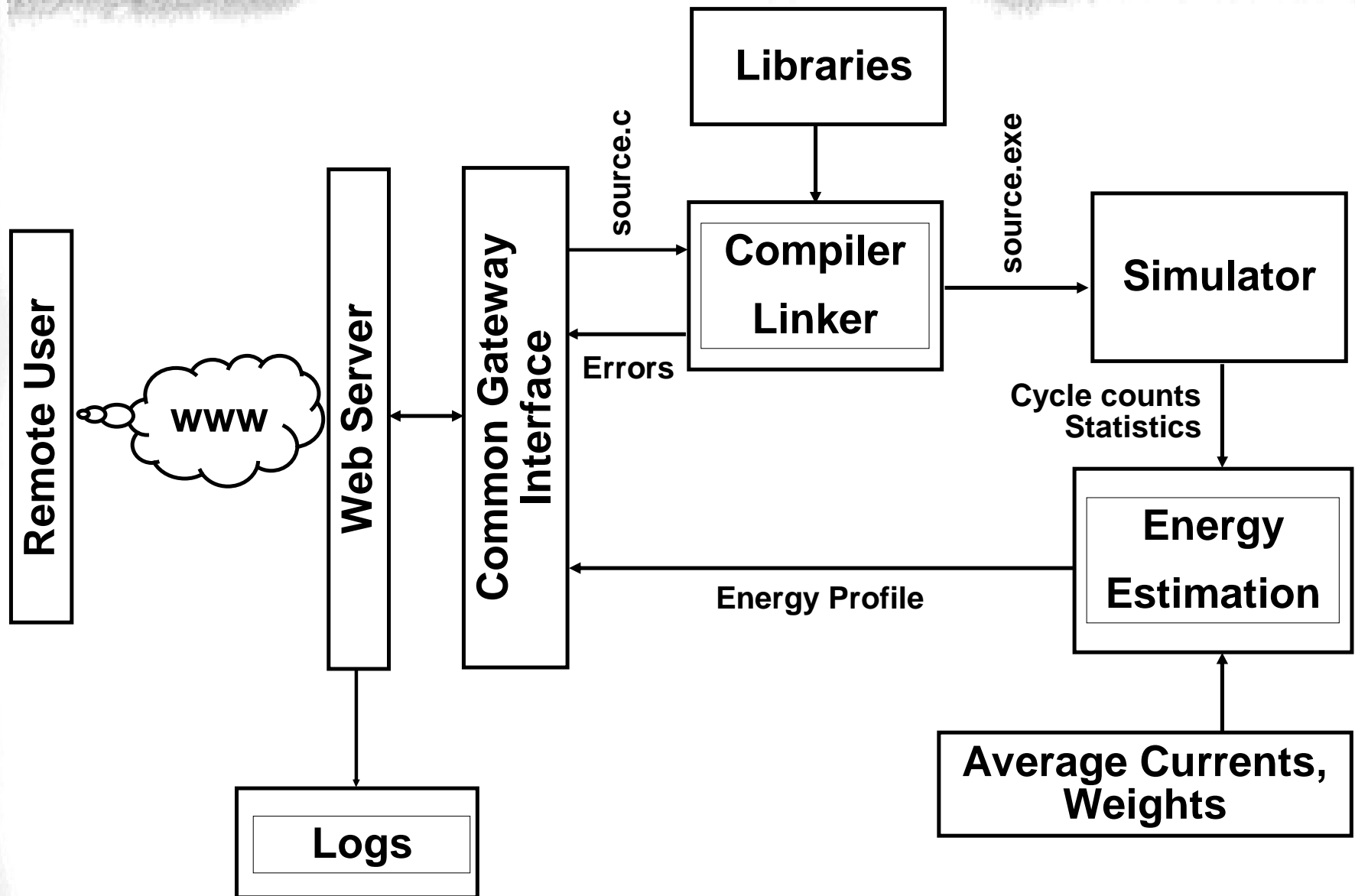
Low Duty Cycle Effects



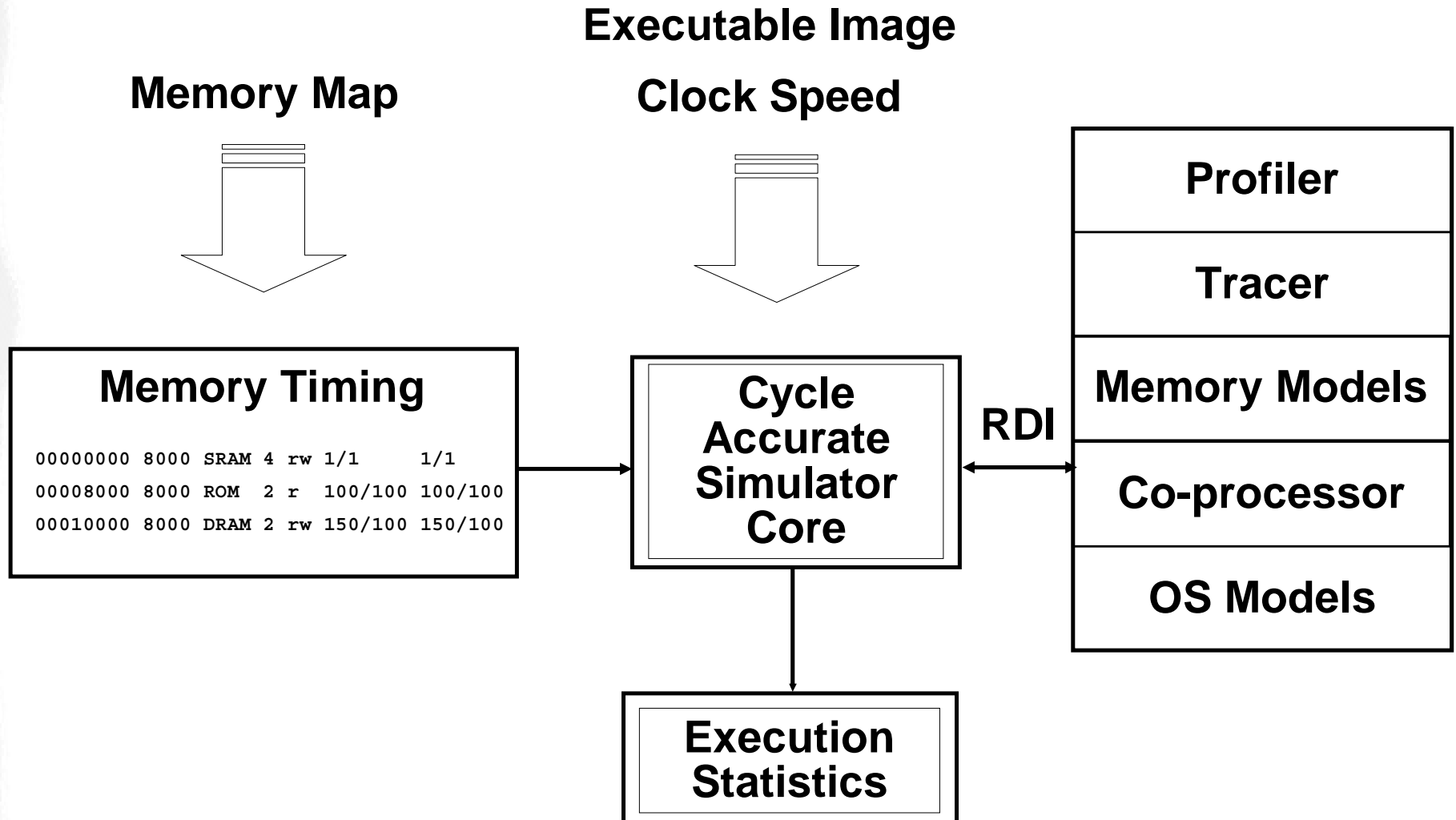
- **Leakage occurs at all times!**
 - $D = 100\% \Rightarrow$ Leakage is 10%
 - $D = 10\% \Rightarrow$ Leakage $> 50\%$
- **Just in time processing will reduce leakage energy**



JouleTrack Design



Timing Estimation Engine



JouleTrack Snapshot

The screenshot shows the Netscape browser window with the title "JouleTrack : A web based software energy profiling tool - Netscape". The address bar shows the URL "http://dry-martini.mit.edu/JouleTrack/arm/". The main content area displays the tool's interface for "StrongARM SA-1100 profiling". It includes a "C Source File" field with the path "E:\sinha\TEMP\dct.c" and a "Browse..." button. Below this are options for "Optimize For" (Memory Size and Performance), a "Command Line Arguments" field, a "StrongARM Operating Frequency" dropdown set to "206MHz", and a "Simulation Complexity" dropdown set to "Level 2". A "Simulate" button is at the bottom of the form. A footer note says "Comments about the tool? Email sinha@mit.edu".

<http://dry-martini.mit.edu/JouleTrack>
4000 hits since Sept-2000

The screenshot shows the "StrongARM SA-1100 Energy Profiling Results" page. It features a table of simulation parameters and two pie charts. The table lists: Source file (E:\sinha\TEMP\dct.c), Operating frequency (206MHz), Operating voltage (1.5 Volts), Simulation level (2), and Execution time (44344 µsecs). The "Cyclewise Breakdown" pie chart shows four categories: Instruction, Seq Mem Access, Non-Seq Mem Access, and Internal. The "Switching vs Leakage" pie chart shows two categories: Switching and Leakage. A final table at the bottom provides current and energy values: Switching current (0.2048 Amps), Leakage current (0.0330 Amps), Total current (0.2378 Amps), and Total energy (15815.4 µJoules).

Parameter	Value
Source file	E:\sinha\TEMP\dct.c
Operating frequency	206MHz
Operating voltage	1.5 Volts
Simulation level	2
Execution time	44344 µsecs

Category	Value
Switching current	0.2048 Amps
Leakage current	0.0330 Amps
Total current	0.2378 Amps
Total energy	15815.4 µJoules

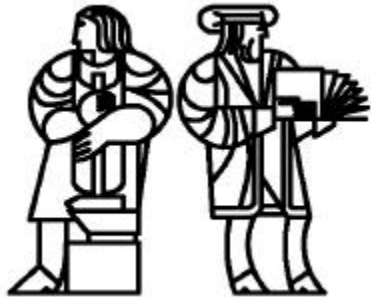
Conclusions

- **Fast macro-level program current estimation demonstrated**
 - ◆ No need for elaborate trace profiling
 - ◆ Can be incorporated in an energy aware application development environment
- **Very little instruction current variation because of common overheads**
- **Leakage currents becoming significant**
 - ◆ 10% at 100% duty cycle on StrongARM
 - ◆ Leakage measurement technique presented

MIT μ AMPS Project

SA-1100 Instruction Current Profiling Experiment

09/01/2000



Data-Processing Instructions Addressing Mode 1

ADC	T _{inst} (sec)	E _{inst} (J)	T _{run} (sec)	N _{inst}	N _{iter}	Current (A)	Voltage (V)	Currents (A)
Immediate and Register ADC Rm, 0x<immediate>,Rs	1.080E-08	2.917E-09	108	100	1E+08	0.185	1.460	0.185
Arithmetic Shift Right by Register ADC Rm, Rd, Rs, ASR Rn	1.180E-08	2.952E-09	118	100	1E+08	0.171	1.463	0.171
Immediate and Immediate ADC Rm, 0x<immediate>, 0x<immediate>	1.080E-08	2.870E-09	108	100	1E+08	0.182	1.460	0.182
Rotate Right by Register ADC Rm, Rd, Rs, ROR Rn	1.070E-08	2.693E-09	107	100	1E+08	0.172	1.463	0.172
Logical Shift Left by register ADC Rm, Rd, Rs, LSL Rn	1.080E-08	2.670E-09	108	100	1E+08	0.169	1.463	0.169
Logical Shift Right by Register ADC Rm, Rd, Rs, LSR Rn	1.070E-08	2.646E-09	107	100	1E+08	0.169	1.463	0.169
Rotate Right by Immediate ADC Rm, Rd, Rs, ROR #<immediate>	5.600E-09	1.433E-09	56	100	1E+08	0.175	1.462	0.175
Rotate Right with extend ADC Rm, Rd, Rs, RRX	5.600E-09	1.433E-09	56	100	1E+08	0.175	1.462	0.175
Logical Shift Right by Immediate ADC Rm, Rd, Rs, LSR #<immediate>	5.600E-09	1.433E-09	56	100	1E+08	0.175	1.462	0.175
Arithmetic Shift Right by Immediate ADC Rm, Rd, Rs, ASR #<immediate>	5.500E-09	1.407E-09	55	100	1E+08	0.175	1.462	0.175
Logical Shift Left by immediate ADC Rm, Rd, Rs, LSL #<immediate>	5.500E-09	1.399E-09	55	100	1E+08	0.174	1.462	0.174
Register and Register ADC Rm, Rd, Rs	5.600E-09	1.393E-09	56	100	1E+08	0.17	1.463	0.17
Register and Immediate ADC Rm, Rs, 0x<immediate>	5.500E-09	1.377E-09	55	100	1E+08	0.171	1.464	0.171
								0.174

ADD	T _{inst} (sec)	E _{inst} (J)	T _{run} (sec)	N _{inst}	N _{iter}	Current (A)	Voltage (V)	Currents (A)
Logical Shift Left by register ADD Rm, Rd, Rs, LSL Rn	1.290E-08	3.272E-09	129	100	1E+08	0.173	1.466	0.173
Immediate and Register ADD Rm, 0x<immediate>,Rs	1.080E-08	3.000E-09	108	100	1E+08	0.19	1.462	0.19
Logical Shift Right by Register ADD Rm, Rd, Rs, LSR Rn	1.180E-08	2.993E-09	118	100	1E+08	0.173	1.466	0.173
Immediate and Immediate ADD Rm, 0x<immediate>, 0x<immediate>	1.080E-08	2.968E-09	108	100	1E+08	0.188	1.462	0.188
Rotate Right by Register ADD Rm, Rd, Rs, ROR Rn	1.070E-08	2.743E-09	107	100	1E+08	0.175	1.465	0.175

Arithmetic Shift Right by Register ADC Rm, Rd, Rs, ASR Rn	1.080E-08	2.714E-09	108	100	1E+08	0.172	1.461
Logical Shift Right by Immediate ADD Rm, Rd, Rs, LSR #<immediate>	6.700E-09	1.746E-09	67	100	1E+08	0.178	1.464
Rotate Right by Immediate ADD Rm, Rd, Rs, ROR #<immediate>	6.000E-09	1.564E-09	60	100	1E+08	0.178	1.464
Arithmetic Shift Right by Immediate ADD Rm, Rd, Rs, ASR #<immediate>	5.600E-09	1.459E-09	56	100	1E+08	0.178	1.464
Rotate Right with extend ADD Rm, Rd, Rs, RRX	5.500E-09	1.433E-09	55	100	1E+08	0.178	1.464
Logical Shift Left by immediate ADD Rm, Rd, Rs, LSL #<immediate>	5.500E-09	1.433E-09	55	100	1E+08	0.178	1.464
Register and Register ADD Rm, Rd, Rs	5.500E-09	1.410E-09	55	100	1E+08	0.175	1.465
Register and Immediate ADD Rm, Rs, 0x<immediate>	5.500E-09	1.395E-09	55	100	1E+08	0.173	1.466
AND	T_{inst} (sec)	E_{inst} (J)	T_{run} (sec)	N_{inst}	N_{iter}	Current (A)	Voltage (V)
Immediate and Immediate AND Rm, 0x<immediate>, 0x<immediate>	1.180E-08	3.036E-09	118	100	1E+08	0.176	1.462
Immediate and Register AND Rm, 0x<immediate>, Rs	1.070E-08	2.857E-09	107	100	1E+08	0.183	1.459
Arithmetic Shift Right by Register AND Rm, Rd, Rs, ASR Rn	1.080E-08	2.714E-09	108	100	1E+08	0.172	1.461
Logical Shift Left by register AND Rm, Rd, Rs, LSL Rn	1.080E-08	2.684E-09	108	100	1E+08	0.17	1.462
Rotate Right by Register AND Rm, Rd, Rs, ROR Rn	1.070E-08	2.689E-09	107	100	1E+08	0.172	1.461
Logical Shift Right by Register AND Rm, Rd, Rs, LSR Rn	1.070E-08	2.673E-09	107	100	1E+08	0.171	1.461
Rotate Right by Immediate AND Rm, Rd, Rs, ROR #<immediate>	5.600E-09	1.439E-09	56	100	1E+08	0.176	1.460
Logical Shift Right by Immediate AND Rm, Rd, Rs, LSR #<immediate>	5.500E-09	1.413E-09	55	100	1E+08	0.176	1.460
Arithmetic Shift Right by Immediate AND Rm, Rd, Rs, ASR #<immediate>	5.500E-09	1.413E-09	55	100	1E+08	0.176	1.460
Rotate Right with extend AND Rm, Rd, Rs, RRX	5.500E-09	1.413E-09	55	100	1E+08	0.176	1.460
Logical Shift Left by immediate AND Rm, Rd, Rs, LSL #<immediate>	5.500E-09	1.406E-09	55	100	1E+08	0.175	1.461
Register and Register AND Rm, Rd, Rs	5.500E-09	1.367E-09	55	100	1E+08	0.17	1.462
Register and Immediate AND Rm, Rs, 0x<immediate>	5.500E-09	1.367E-09	55	100	1E+08	0.17	1.462

0.172
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0.175
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0.17
0.174

BIC	T_{inst} (sec)	E_{inst} (J)	T_{run} (sec)	N_{inst}	N_{iter}	Current (A)	Voltage (V)
Immediate and Immediate BIC Rm, 0x<immediate>, 0x<immediate>	1.180E-08	2.987E-09	118	100	1E+08	0.173	1.463
Immediate and Register BIC Rm, 0x<immediate>,Rs	1.070E-08	2.857E-09	107	100	1E+08	0.183	1.459
Logical Shift Left by register BIC Rm, Rd, Rs, LSL Rn	1.070E-08	2.675E-09	107	100	1E+08	0.171	1.462
Arithmetic Shift Right by Register BIC Rm, Rd, Rs, ASR Rn	1.070E-08	2.689E-09	107	100	1E+08	0.172	1.461
Rotate Right by Register BIC Rm, Rd, Rs, ROR Rn	1.070E-08	2.675E-09	107	100	1E+08	0.171	1.462
Logical Shift Right by Register BIC Rm, Rd, Rs, LSR Rn	1.080E-08	2.684E-09	108	100	1E+08	0.17	1.462
Rotate Right by Immediate BIC Rm, Rd, Rs, ROR #<immediate>	5.500E-09	1.413E-09	55	100	1E+08	0.176	1.460
Logical Shift Right by Immediate BIC Rm, Rd, Rs, LSR #<immediate>	5.600E-09	1.440E-09	56	100	1E+08	0.176	1.461
Arithmetic Shift Right by Immediate BIC Rm, Rd, Rs, ASR #<immediate>	5.500E-09	1.413E-09	55	100	1E+08	0.176	1.460
Rotate Right with extend BIC Rm, Rd, Rs, RRX	5.600E-09	1.432E-09	56	100	1E+08	0.175	1.461
Logical Shift Left by immediate BIC Rm, Rd, Rs, LSL #<immediate>	5.600E-09	1.439E-09	56	100	1E+08	0.176	1.460
Register and Register BIC Rm, Rd, Rs	5.500E-09	1.374E-09	55	100	1E+08	0.171	1.461
Register and Immediate BIC Rm, Rs, 0x<immediate>	5.600E-09	1.391E-09	56	100	1E+08	0.17	1.461

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0.171
0.17

0.174

CMN	T_{inst} (sec)	E_{inst} (J)	T_{run} (sec)	N_{inst}	N_{iter}	Current (A)	Voltage (V)
Immediate CMN Rm, 0x<immediate>	1.610E-08	4.916E-09	161	100	1E+08	0.21	1.454
Arithmetic Shift Right by Register CMN Rm, Rs, ASR Rn	1.070E-08	2.736E-09	107	100	1E+08	0.175	1.461
Rotate Right by Register CMN Rm, Rs, ROR Rn	1.070E-08	2.736E-09	107	100	1E+08	0.175	1.461
Logical Shift Left by register CMN Rm, Rs, LSL Rn	1.070E-08	2.706E-09	107	100	1E+08	0.173	1.462

0.21
0.175
0.175
0.173

Logical Shift Right by Register CMN Rm, Rs, LSR Rn	1.070E-08	2.706E-09	107	100	1E+08	0.173	1.462
Logical Shift Left by immediate CMN Rm, Rs, LSL #<immediate>	6.100E-09	1.586E-09	61	100	1E+08	0.178	1.461
Logical Shift Right by Immediate CMN Rm, Rs, LSR #<immediate>	5.600E-09	1.465E-09	56	100	1E+08	0.179	1.461
Arithmetic Shift Right by Immediate CMN Rm, Rs, ASR #<immediate>	5.600E-09	1.465E-09	56	100	1E+08	0.179	1.461
Rotate Right by Immediate CMN Rm, Rs, ROR #<immediate>	5.600E-09	1.464E-09	56	100	1E+08	0.179	1.460
Rotate Right with extend CMN Rm, Rs, RRX	5.600E-09	1.464E-09	56	100	1E+08	0.179	1.460
Register CMN Rm, Rs	5.500E-09	1.414E-09	55	100	1E+08	0.176	1.461

0.173
0.178
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0.179
0.179
0.179
0.176

0.180

CMP	T_{inst} (sec)	E_{inst} (J)	T_{run} (sec)	N_{inst}	N_{iter}	Current (A)	Voltage (V)
Immediate CMP Rm, 0x<immediate>	1.610E-08	4.959E-09	161	100	1E+08	0.212	1.453
Arithmetic Shift Right by Register CMP Rm, Rs, ASR Rn	1.070E-08	2.736E-09	107	100	1E+08	0.175	1.461
Rotate Right by Register CMP Rm, Rs, ROR Rn	1.070E-08	2.736E-09	107	100	1E+08	0.175	1.461
Logical Shift Left by register CMP Rm, Rs, LSL Rn	1.070E-08	2.706E-09	107	100	1E+08	0.173	1.462
Logical Shift Right by Register CMP Rm, Rs, LSR Rn	1.070E-08	2.706E-09	107	100	1E+08	0.173	1.462
Logical Shift Left by immediate CMP Rm, Rs, LSL #<immediate>	6.100E-09	1.586E-09	61	100	1E+08	0.178	1.461
Rotate Right with extend CMP Rm, Rs, RRX	5.600E-09	1.488E-09	56	100	1E+08	0.182	1.460
Logical Shift Right by Immediate CMP Rm, Rs, LSR #<immediate>	5.600E-09	1.464E-09	56	100	1E+08	0.179	1.460
Arithmetic Shift Right by Immediate CMP Rm, Rs, ASR #<immediate>	5.600E-09	1.464E-09	56	100	1E+08	0.179	1.460
Rotate Right by Immediate CMP Rm, Rs, ROR #<immediate>	5.600E-09	1.464E-09	56	100	1E+08	0.179	1.460
Register CMP Rm, Rs	5.500E-09	1.406E-09	55	100	1E+08	0.175	1.461

0.212
0.175
0.175
0.173
0.173
0.178
0.182
0.179
0.179
0.179
0.175

0.18

EOR	T_{inst} (sec)	E_{inst} (J)	T_{run} (sec)	N_{inst}	N_{iter}	Current (A)	Voltage (V)
Immediate and Immediate EOR Rm, 0x<immediate>, 0x<immediate>	1.190E-08	3.262E-09	119	100	1E+08	0.188	1.458
Immediate and Register EOR Rm, 0x<immediate>,Rs	1.070E-08	2.949E-09	107	100	1E+08	0.189	1.458
Arithmetic Shift Right by Register EOR Rm, Rd, Rs, ASR Rn	1.080E-08	2.777E-09	108	100	1E+08	0.176	1.461
Rotate Right by Register EOR Rm, Rd, Rs, ROR Rn	1.080E-08	2.777E-09	108	100	1E+08	0.176	1.461
Logical Shift Left by register EOR Rm, Rd, Rs, LSL Rn	1.080E-08	2.746E-09	108	100	1E+08	0.174	1.461
Logical Shift Right by Register EOR Rm, Rd, Rs, LSR Rn	1.080E-08	2.746E-09	108	100	1E+08	0.174	1.461
Rotate Right by Immediate EOR Rm, Rd, Rs, ROR #<immediate>	5.500E-09	1.445E-09	55	100	1E+08	0.18	1.460
Rotate Right with extend EOR Rm, Rd, Rs, RRX	5.500E-09	1.445E-09	55	100	1E+08	0.18	1.460
Logical Shift Right by Immediate EOR Rm, Rd, Rs, LSR #<immediate>	5.500E-09	1.445E-09	55	100	1E+08	0.18	1.460
Arithmetic Shift Right by Immediate EOR Rm, Rd, Rs, ASR #<immediate>	5.500E-09	1.445E-09	55	100	1E+08	0.18	1.460
Logical Shift Left by immediate EOR Rm, Rd, Rs, LSL #<immediate>	5.500E-09	1.445E-09	55	100	1E+08	0.18	1.460
Register and Register EOR Rm, Rd, Rs	5.500E-09	1.406E-09	55	100	1E+08	0.175	1.461
Register and Immediate EOR Rm, Rs, 0x<immediate>	5.500E-09	1.398E-09	55	100	1E+08	0.174	1.461

0.188
0.189
0.176
0.176
0.174
0.174
0.18
0.18
0.18
0.18
0.18
0.175
0.174

0.179

MOV	T_{inst} (sec)	E_{inst} (J)	T_{run} (sec)	N_{inst}	N_{iter}	Current (A)	Voltage (V)
Arithmetic Shift Right by Register MOVm, Rs, ASR Rn	1.070E-08	2.736E-09	107	100	1E+08	0.175	1.461
Rotate Right by Register MOV Rm, Rs, ROR Rn	1.070E-08	2.736E-09	107	100	1E+08	0.175	1.461
Logical Shift Left by register MOV Rm, Rs, LSL Rn	1.070E-08	2.706E-09	107	100	1E+08	0.173	1.462
Logical Shift Right by Register MOV Rm, Rs, LSR Rn	1.070E-08	2.704E-09	107	100	1E+08	0.173	1.461

0.175
0.175
0.173
0.173

Logical Shift Left by immediate MOV Rm, Rs, LSL #<immediate>	6.100E-09	1.585E-09	61	100	1E+08	0.178	1.460
Rotate Right by Immediate MOV Rm, Rs, ROR #<immediate>	5.600E-09	1.464E-09	56	100	1E+08	0.179	1.460
Rotate Right with extend MOV Rm, Rs, RRX	5.600E-09	1.464E-09	56	100	1E+08	0.179	1.460
Immediate MOV Rm, 0x<immediate>	5.600E-09	1.440E-09	56	100	1E+08	0.176	1.461
Logical Shift Right by Immediate MOV Rm, Rs, LSR #<immediate>	5.500E-09	1.437E-09	55	100	1E+08	0.179	1.460
Arithmetic Shift Right by Immediate MOV Rm, Rs, ASR #<immediate>	5.500E-09	1.429E-09	55	100	1E+08	0.178	1.460
Register MOV Rm, Rs	5.500E-09	1.398E-09	55	100	1E+08	0.174	1.461

0.178
0.179
0.179
0.176
0.179
0.178
0.174

0.176

MVN	T_{inst} (sec)	E_{inst} (J)	T_{run} (sec)	N_{inst}	N_{iter}	Current (A)	Voltage (V)
Arithmetic Shift Right by Register MVNm, Rs, ASR Rn	1.080E-08	2.761E-09	108	100	1E+08	0.175	1.461
Rotate Right by Register MVN Rm, Rs, ROR Rn	1.080E-08	2.761E-09	108	100	1E+08	0.175	1.461
Logical Shift Left by register MVN Rm, Rs, LSL Rn	1.080E-08	2.730E-09	108	100	1E+08	0.173	1.461
Logical Shift Right by Register MVN Rm, Rs, LSR Rn	1.080E-08	2.730E-09	108	100	1E+08	0.173	1.461
Logical Shift Left by immediate MVN Rm, Rs, LSL #<immediate>	6.000E-09	1.559E-09	60	100	1E+08	0.178	1.460
Logical Shift Right by Immediate MVN Rm, Rs, LSR #<immediate>	5.500E-09	1.437E-09	55	100	1E+08	0.179	1.460
Arithmetic Shift Right by Immediate MVN Rm, Rs, ASR #<immediate>	5.500E-09	1.437E-09	55	100	1E+08	0.179	1.460
Rotate Right by Immediate MVN Rm, Rs, ROR #<immediate>	5.500E-09	1.437E-09	55	100	1E+08	0.179	1.460
Rotate Right with extend MVN Rm, Rs, RRX	5.500E-09	1.437E-09	55	100	1E+08	0.179	1.460
Register MVN Rm, Rs	5.600E-09	1.424E-09	56	100	1E+08	0.174	1.461
Immediate MVN Rm, 0x<immediate>	5.600E-09	1.407E-09	56	100	1E+08	0.172	1.461

0.175
0.175
0.173
0.173
0.178
0.179
0.179
0.179
0.179
0.179
0.174
0.172

0.176

ORR	T_{inst} (sec)	E_{inst} (J)	T_{run} (sec)	N_{inst}	N_{iter}	Current (A)	Voltage (V)
Immediate and Immediate ORR Rm, 0x<immediate>, 0x<immediate>	1.180E-08	3.234E-09	118	100	1E+08	0.188	1.458
Immediate and Register ORR Rm, 0x<immediate>,Rs	1.080E-08	2.960E-09	108	100	1E+08	0.188	1.458
Arithmetic Shift Right by Register ORR Rm, Rd, Rs, ASR Rn	1.080E-08	2.777E-09	108	100	1E+08	0.176	1.461
Rotate Right by Register ORR Rm, Rd, Rs, ROR Rn	1.080E-08	2.777E-09	108	100	1E+08	0.176	1.461
Logical Shift Left by register ORR Rm, Rd, Rs, LSL Rn	1.070E-08	2.720E-09	107	100	1E+08	0.174	1.461
Logical Shift Right by Register ORR Rm, Rd, Rs, LSR Rn	1.080E-08	2.746E-09	108	100	1E+08	0.174	1.461
Rotate Right by Immediate ORR Rm, Rd, Rs, ROR #<immediate>	5.500E-09	1.445E-09	55	100	1E+08	0.18	1.460
Rotate Right with extend ORR Rm, Rd, Rs, RRX	5.500E-09	1.445E-09	55	100	1E+08	0.18	1.460
Logical Shift Right by Immediate ORR Rm, Rd, Rs, LSR #<immediate>	5.500E-09	1.445E-09	55	100	1E+08	0.18	1.460
Arithmetic Shift Right by Immediate ORR Rm, Rd, Rs, ASR #<immediate>	5.500E-09	1.445E-09	55	100	1E+08	0.18	1.460
Logical Shift Left by immediate ORR Rm, Rd, Rs, LSL #<immediate>	5.500E-09	1.444E-09	55	100	1E+08	0.18	1.459
Register and Register ORR Rm, Rd, Rs	5.600E-09	1.432E-09	56	100	1E+08	0.175	1.461
Register and Immediate ORR Rm, Rs, 0x<immediate>	5.600E-09	1.424E-09	56	100	1E+08	0.174	1.461

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0.188
0.176
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0.174
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0.18
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0.18
0.18
0.18
0.175
0.174

0.179

RSB	T_{inst} (sec)	E_{inst} (J)	T_{run} (sec)	N_{inst}	N_{iter}	Current (A)	Voltage (V)
Immediate and Immediate RSB Rm, 0x<immediate>, 0x<immediate>	1.190E-08	3.599E-09	119	100	1E+08	0.208	1.454
Immediate and Register RSB Rm, 0x<immediate>,Rs	1.090E-08	3.204E-09	109	100	1E+08	0.202	1.455
Arithmetic Shift Right by Register RSB Rm, Rd, Rs, ASR Rn	1.070E-08	2.751E-09	107	100	1E+08	0.176	1.461
Rotate Right by Register RSB Rm, Rd, Rs, ROR Rn	1.070E-08	2.751E-09	107	100	1E+08	0.176	1.461
Logical Shift Left by register RSB Rm, Rd, Rs, LSL Rn	1.070E-08	2.720E-09	107	100	1E+08	0.174	1.461

0.208
0.202
0.176
0.176
0.174

Register and Immediate RSC Rm, Rs, 0x<immediate>	5.600E-09	1.424E-09	56	100	1E+08	0.174	1.461
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0.174

0.181

SBC	T_{inst} (sec)	E_{inst} (J)	T_{run} (sec)	N_{inst}	N_{iter}	Current (A)	Voltage (V)
Immediate and Immediate SBC Rm, 0x<immediate>, 0x<immediate>	1.180E-08	3.434E-09	118	100	1E+08	0.2	1.455
Immediate and Register SBC Rm, 0x<immediate>,Rs	1.090E-08	3.111E-09	109	100	1E+08	0.196	1.456
Rotate Right by Register SBC Rm, Rd, Rs, ROR Rn	1.080E-08	2.777E-09	108	100	1E+08	0.176	1.461
Arithmetic Shift Right by Register SBC Rm, Rd, Rs, ASR Rn	1.060E-08	2.726E-09	106	100	1E+08	0.176	1.461
Logical Shift Left by register SBC Rm, Rd, Rs, LSL Rn	1.070E-08	2.720E-09	107	100	1E+08	0.174	1.461
Logical Shift Right by Register SBC Rm, Rd, Rs, LSR Rn	1.070E-08	2.720E-09	107	100	1E+08	0.174	1.461
Logical Shift Left by immediate SBC Rm, Rd, Rs, LSL #<immediate>	5.600E-09	1.472E-09	56	100	1E+08	0.18	1.460
Logical Shift Right by Immediate SBC Rm, Rd, Rs, LSR #<immediate>	5.600E-09	1.472E-09	56	100	1E+08	0.18	1.460
Arithmetic Shift Right by Immediate RSC Rm, Rd, Rs, ASR #<immediate>	5.600E-09	1.472E-09	56	100	1E+08	0.18	1.460
Rotate Right by Immediate SBC Rm, Rd, Rs, ROR #<immediate>	5.500E-09	1.445E-09	55	100	1E+08	0.18	1.460
Rotate Right with extend SBC Rm, Rd, Rs, RRX	5.500E-09	1.445E-09	55	100	1E+08	0.18	1.460
Register and Register SBC Rm, Rd, Rs	5.500E-09	1.406E-09	55	100	1E+08	0.175	1.461
Register and Immediate SBC Rm, Rs, 0x<immediate>	5.500E-09	1.398E-09	55	100	1E+08	0.174	1.461

0.2

0.196

0.176

0.176

0.174

0.174

0.18

0.18

0.18

0.18

0.18

0.175

0.174

0.180

SUB	T_{inst} (sec)	E_{inst} (J)	T_{run} (sec)	N_{inst}	N_{iter}	Current (A)	Voltage (V)
Immediate and Immediate SUB Rm, 0x<immediate>, 0x<immediate>	1.180E-08	3.468E-09	118	100	1E+08	0.202	1.455
Rotate Right by Register SUB Rm, Rd, Rs, ROR Rn	1.070E-08	2.751E-09	107	100	1E+08	0.176	1.461
Arithmetic Shift Right by Register SUB Rm, Rd, Rs, ASR Rn	1.070E-08	2.751E-09	107	100	1E+08	0.176	1.461
Logical Shift Left by register SUB Rm, Rd, Rs, LSL Rn	1.080E-08	2.746E-09	108	100	1E+08	0.174	1.461

0.202

0.176

0.176

0.174

Logical Shift Right by Register SUB Rm, Rd, Rs, LSR Rn	1.070E-08	2.720E-09	107	100	1E+08	0.174	1.461
Rotate Right with extend SUB Rm, Rd, Rs, RRX	5.600E-09	1.472E-09	56	100	1E+08	0.18	1.460
Logical Shift Right by Immediate SUB Rm, Rd, Rs, LSR #<immediate>	5.500E-09	1.445E-09	55	100	1E+08	0.18	1.460
Arithmetic Shift Right by Immediate SUB Rm, Rd, Rs, ASR #<immediate>	5.500E-09	1.445E-09	55	100	1E+08	0.18	1.460
Rotate Right by Immediate SUB Rm, Rd, Rs, ROR #<immediate>	5.500E-09	1.445E-09	55	100	1E+08	0.18	1.460
Logical Shift Left by immediate SUB Rm, Rd, Rs, LSL #<immediate>	5.500E-09	1.441E-09	55	100	1E+08	0.1794	1.460
Register and Register SUB Rm, Rd, Rs	5.600E-09	1.424E-09	56	100	1E+08	0.174	1.461
Register and Immediate SUB Rm, Rs, 0x<immediate>	5.600E-09	1.424E-09	56	100	1E+08	0.174	1.461
Immediate and Register SUB Rm, 0x<immediate>,Rs	5.500E-09	1.398E-09	55	100	1E+08	0.174	1.461

0.174
0.18
0.18
0.18
0.18
0.1794
0.174
0.174
0.174

0.179

TEQ	T_{inst} (sec)	E_{inst} (J)	T_{run} (sec)	N_{inst}	N_{iter}	Current (A)	Voltage (V)
Immediate TEQ Rm, 0x<immediate>	1.070E-08	2.980E-09	107	100	1E+08	0.191	1.458
Arithmetic Shift Right by Register TEQ Rm, Rs, ASR Rn	1.070E-08	2.751E-09	107	100	1E+08	0.176	1.461
Rotate Right by Register TEQ Rm, Rs, ROR Rn	1.070E-08	2.751E-09	107	100	1E+08	0.176	1.461
Logical Shift Left by register TEQ Rm, Rs, LSL Rn	1.070E-08	2.720E-09	107	100	1E+08	0.174	1.461
Logical Shift Right by Register TEQ Rm, Rs, LSR Rn	1.070E-08	2.720E-09	107	100	1E+08	0.174	1.461
Logical Shift Left by immediate TEQ Rm, Rs, LSL #<immediate>	6.100E-09	1.594E-09	61	100	1E+08	0.179	1.460
Rotate Right with extend TEQ Rm, Rs, RRX	5.500E-09	1.437E-09	55	100	1E+08	0.179	1.460
Logical Shift Right by Immediate TEQ Rm, Rs, LSR #<immediate>	5.600E-09	1.472E-09	56	100	1E+08	0.18	1.460
Arithmetic Shift Right by Immediate TEQ Rm, Rs, ASR #<immediate>	5.600E-09	1.472E-09	56	100	1E+08	0.18	1.460
Rotate Right by Immediate TEQ Rm, Rs, ROR #<immediate>	5.600E-09	1.472E-09	56	100	1E+08	0.18	1.460

0.191
0.176
0.176
0.174
0.174
0.179
0.179
0.18
0.18
0.18

Register TEQ Rm, Rs	5.600E-09	1.448E-09	56	100	1E+08	0.177	1.461
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0.177 0.179

TST	T_{inst} (sec)	E_{inst} (J)	T_{run} (sec)	N_{inst}	N_{iter}	Current (A)	Voltage (V)
Immediate TST Rm, 0x<immediate>	1.610E-08	4.727E-09	161	100	1E+08	0.2015	1.457
Arithmetic Shift Right by Register TST Rm, Rs, ASR Rn	1.080E-08	2.761E-09	108	100	1E+08	0.175	1.461
Rotate Right by Register TST Rm, Rs, ROR Rn	1.080E-08	2.777E-09	108	100	1E+08	0.176	1.461
Logical Shift Left by register TST Rm, Rs, LSL Rn	1.080E-08	2.747E-09	108	100	1E+08	0.174	1.462
Logical Shift Right by Register TST Rm, Rs, LSR Rn	1.080E-08	2.747E-09	108	100	1E+08	0.174	1.462
Logical Shift Left by immediate TST Rm, Rs, LSL #<immediate>	6.000E-09	1.569E-09	60	100	1E+08	0.179	1.461
Rotate Right with extend TST Rm, Rs, RRX	5.500E-09	1.437E-09	55	100	1E+08	0.179	1.460
Logical Shift Right by Immediate TST Rm, Rs, LSR #<immediate>	5.500E-09	1.437E-09	55	100	1E+08	0.179	1.460
Arithmetic Shift Right by Immediate TST Rm, Rs, ASR #<immediate>	5.500E-09	1.437E-09	55	100	1E+08	0.179	1.460
Rotate Right by Immediate TST Rm, Rs, ROR #<immediate>	5.500E-09	1.445E-09	55	100	1E+08	0.18	1.460
Register TST Rm, Rs	5.500E-09	1.415E-09	55	100	1E+08	0.176	1.462

0.2015
0.175
0.176
0.174
0.174
0.179
0.179
0.179
0.179
0.18
0.176
0.179

Multiply Instructions

MLA	T_{inst} (sec)	E_{inst} (J)	T_{run} (sec)	N_{inst}	N_{iter}	Current (A)	Voltage (V)
Immediate, Register, Immediate MLA Rd, 0x<immediate>, Rs, 0x<immediate>	2.660E-08	7.591E-09	266	100	1E+08	0.196	1.456

0.196

Immediate, Immediate, Immediate MLA Rd, 0x<immediate>, 0x<immediate>, 0x<immediate>	2.130E-08	6.229E-09	213	100	1E+08	0.201	1.455
Immediate, Immediate, Register MLA Rd, 0x<immediate>, 0x<immediate>, Rn	1.770E-08	5.551E-09	177	100	1E+08	0.216	1.452
Register, Immediate, Immediate MLA Rd, Rm, 0x<immediate>, 0x<immediate>	1.610E-08	4.959E-09	161	100	1E+08	0.212	1.453
Immediate, Register, Register MLA Rd, 0x<immediate>, Rs, Rn	1.180E-08	3.607E-09	118	100	1E+08	0.2104	1.453
Register, Immediate, Register MLA Rd, Rm, 0x<immediate>, Rn	1.080E-08	3.356E-09	108	100	1E+08	0.214	1.452
Register, Register, Immediate MLA Rd, Rm, Rs, 0x<immediate>	1.080E-08	3.356E-09	108	100	1E+08	0.214	1.452
Register, Register, Register MLA Rd, Rm, Rs, Rn	1.060E-08	2.906E-09	106	100	1E+08	0.188	1.458

0.201
0.216
0.212
0.2104
0.214
0.214
0.188

0.206

MUL	T_{inst} (sec)	E_{inst} (J)	T_{run} (sec)	N_{inst}	N_{iter}	Current (A)	Voltage (V)
Immediate, Register MUL Rd, 0x<immediate>, Rn	2.080E-08	6.053E-09	208	100	1E+08	0.2	1.455
Register, Register MUL Rd, Rs, Rn	2.070E-08	5.644E-09	207	100	1E+08	0.187	1.458
Immediate, Immediate MUL Rd, 0x<immediate>, 0x<immediate>	1.180E-08	3.067E-09	118	100	1E+08	0.178	1.460
Register, Immediate MUL Rd, Rm, 0x<immediate>	5.600E-09	1.424E-09	56	100	1E+08	0.174	1.461

0.2
0.187
0.178
0.174

0.185

SMLAL	N/A
SMULL	N/A
UMLAL	N/A
UMULL	N/A

Load and Store Word or Unsigned Byte Instructions: Addressing Mode 2

LDR	T_{inst} (sec)	E_{inst} (J)	T_{run} (sec)	N_{inst}	N_{iter}	Current (A)	Voltage (V)
Immediate Offset LDR Rd, [Rn, # +/-<12 bit offset>]	5.600E-09	2.039E-09	56	100	1E+08	0.252	1.445
Register Offset LDR Rd, [Rn, +/-Rm]	2.900E-08	1.048E-08	29	10	1E+08	0.25	1.445
Scaled register offsets LDR Rd, [Rn, +/-Rm, <shift> #<shift imm>]	5.600E-09	2.047E-09	56	100	1E+08	0.253	1.445
Immediate pre-indexed LDR Rd, [Rn, # +/-<12 bit offset>]!	2.150E-07	1.649E-08	43	20	1E+07	0.0515	1.489
Register pre-indexed LDR Rd, [Rn, +/-Rm]!	5.800E-09	2.104E-09	29	50	1E+08	0.251	1.445
Scaled register pre-indexed LDR Rd, [Rn, +/-Rm, LSL #<shift imm>]!	5.500E-09	2.025E-09	55	100	1E+08	0.255	1.444
Immediate post-indexed LDR Rd, [Rn], # +/-<12 bit offset>	1.750E-07	1.342E-08	7	40	1E+06	0.0515	1.489
Register post-indexed LDR Rd, [Rn], +/-Rm	6.000E-09	2.168E-09	30	50	1E+08	0.25	1.445
Scaled register post-indexed LDR Rd, [Rn], +/-Rm, LSL #<shift imm>	5.500E-09	2.017E-09	55	100	1E+08	0.254	1.444

0.252
0.25
0.253
0.0515
0.251
0.255
0.0515
0.25
0.254

0.208

LDRB	T_{inst} (sec)	E_{inst} (J)	T_{run} (sec)	N_{inst}	N_{iter}	Current (A)	Voltage (V)
Immediate Offset LDRB Rd, [Rn, # +/-<12 bit offset>]	5.500E-09	2.000E-09	55	100	1E+08	0.2516	1.445
Register Offset LDRB Rd, [Rn, +/-Rm]	3.000E-08	1.088E-08	30	10	1E+08	0.251	1.445
Scaled register offsets LDRB Rd, [Rn, +/-Rm, <shift> #<shift imm>]	5.600E-09	2.047E-09	56	100	1E+08	0.253	1.445

0.2516
0.251
0.253

Immediate pre-indexed LDRB Rd, [Rn, # +/-<12 bit offset>]!	2.100E-07	1.610E-08	42	20	1E+07	0.0515	1.489
Register pre-indexed LDRB Rd, [Rn, +/-Rm]!	6.000E-09	2.176E-09	30	50	1E+08	0.251	1.445
Scaled register pre-indexed LDRB Rd, [Rn, +/-Rm, LSL #<shift imm>]!	5.500E-09	2.025E-09	55	100	1E+08	0.255	1.444
Immediate post-indexed LDRB Rd, [Rn], # +/-<12 bit offset>	1.750E-07	1.345E-08	7	40	1E+06	0.0516	1.489
Register post-indexed LDRB Rd, [Rn], +/-Rm	5.600E-09	2.031E-09	28	50	1E+08	0.251	1.445
Scaled register post-indexed LDRB Rd, [Rn], +/-Rm, LSL #<shift imm>	5.600E-09	2.062E-09	56	100	1E+08	0.255	1.444

0.0515
0.251
0.255
0.0516
0.251
0.255

0.208

LDRBT	T_{inst} (sec)	E_{inst} (J)	T_{run} (sec)	N_{inst}	N_{iter}	Current (A)	Voltage (V)
Immediate Offset LDRBT Rd, [Rn, # +/-<12 bit offset>]	N/A						
Register Offset LDRBT Rd, [Rn, +/-Rm]	N/A						
Scaled register offsets LDRBT Rd, [Rn, +/-Rm, <shift> #<shift imm>]	N/A						
Immediate pre-indexed LDRBT Rd, [Rn, # +/-<12 bit offset>]!	N/A						
Register pre-indexed LDRBT Rd, [Rn, +/-Rm]!	N/A						
Scaled register pre-indexed LDRBT Rd, [Rn, +/-Rm, LSL #<shift imm>]!	N/A						
Immediate post-indexed LDRBT Rd, [Rn], # +/-<12 bit offset>	1.750E-07	1.329E-08	7	40	1E+06	0.051	1.489
Register post-indexed LDRBT Rd, [Rn], +/-Rm	5.800E-09	2.104E-09	29	50	1E+08	0.251	1.445

0.051
0.251

Scaled register post-indexed LDRBT Rd, [Rn], +/-Rm, LSL #<shift imm>	5.700E-09	2.091E-09	57	100	1E+08	0.254	1.444
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0.254 0.185

LDRT	T_{inst} (sec)	E_{inst} (J)	T_{run} (sec)	N_{inst}	N_{iter}	Current (A)	Voltage (V)
Immediate Offset LDRT Rd, [Rn, # +/-<12 bit offset>]	N/A						
Register Offset LDRT Rd, [Rn, +/-Rm]	N/A						
Scaled register offsets LDRT Rd, [Rn, +/-Rm, <shift> #<shift imm>]	N/A						
Immediate pre-indexed LDRT Rd, [Rn, # +/-<12 bit offset>]!	N/A						
Register pre-indexed LDRT Rd, [Rn, +/-Rm]!	N/A						
Scaled register pre-indexed LDRT Rd, [Rn, +/-Rm, LSL #<shift imm>]!	N/A						
Immediate post-indexed LDRT Rd, [Rn], # +/-<12 bit offset>	2.000E-07	1.516E-08	8	40	1E+06	0.0509	1.489
Register post-indexed LDRT Rd, [Rn], +/-Rm	5.800E-09	2.104E-09	29	50	1E+08	0.251	1.445
Scaled register post-indexed LDRT Rd, [Rn], +/-Rm, LSL #<shift imm>	5.600E-09	2.054E-09	56	100	1E+08	0.254	1.444

0.0509
0.251
0.254 0.185

STR	T_{inst} (sec)	E_{inst} (J)	T_{run} (sec)	N_{inst}	N_{iter}	Current (A)	Voltage (V)
Immediate Offset STR Rd, [Rn, # +/-<12 bit offset>]	1.260E-07	3.277E-08	126	10	1E+08	0.178	1.461

0.178

Register Offset STR Rd, [Rn, +/-Rm]	3.000E-08	1.097E-08	30	10	1E+08	0.253	1.445
Scaled register offsets STR Rd, [Rn, +/-Rm, <shift> #<shift imm>]	5.500E-09	2.033E-09	55	100	1E+08	0.256	1.444
Immediate pre-indexed STR Rd, [Rn, # +/-<12 bit offset>]!	1.250E-07	3.306E-08	50	4	1E+08	0.181	1.461
Register pre-indexed STR Rd, [Rn, +/-Rm]!	6.000E-09	2.194E-09	30	50	1E+08	0.253	1.445
Scaled register pre-indexed STR Rd, [Rn, +/-Rm, LSL #<shift imm>]!	5.500E-09	2.033E-09	55	100	1E+08	0.256	1.444
Immediate post-indexed STR Rd, [Rn], # +/-<12 bit offset>	1.275E-07	3.372E-08	51	4	1E+08	0.181	1.461
Register post-indexed STR Rd, [Rn], +/-Rm	5.800E-09	2.120E-09	29	50	1E+08	0.253	1.445
Scaled register post-indexed STR Rd, [Rn], +/-Rm, LSL #<shift imm>	5.500E-09	2.033E-09	55	100	1E+08	0.256	1.444

0.253
0.256
0.181
0.253
0.256
0.181
0.253
0.256

0.230

STRB	T_{inst} (sec)	E_{inst} (J)	T_{run} (sec)	N_{inst}	N_{iter}	Current (A)	Voltage (V)
Immediate Offset STRB Rd, [Rn, # +/-<12 bit offset>]	1.260E-07	3.277E-08	126	10	1E+08	0.178	1.461
Register Offset STRB Rd, [Rn, +/-Rm]	2.900E-08	1.052E-08	29	10	1E+08	0.251	1.445
Scaled register offsets STRB Rd, [Rn, +/-Rm, <shift> #<shift imm>]	5.500E-09	2.019E-09	55	100	1E+08	0.254	1.445
Immediate pre-indexed STRB Rd, [Rn, # +/-<12 bit offset>]!	1.275E-07	3.353E-08	51	4	1E+08	0.18	1.461
Register pre-indexed STRB Rd, [Rn, +/-Rm]!	5.800E-09	2.104E-09	29	50	1E+08	0.251	1.445
Scaled register pre-indexed STRB Rd, [Rn, +/-Rm, LSL #<shift imm>]!	5.600E-09	2.063E-09	56	100	1E+08	0.255	1.445
Immediate post-indexed STRB Rd, [Rn], # +/-<12 bit offset>	1.250E-07	3.306E-08	50	4	1E+08	0.181	1.461
Register post-indexed STRB Rd, [Rn], +/-Rm	6.200E-09	2.250E-09	31	50	1E+08	0.251	1.446
Scaled register post-indexed STRB Rd, [Rn], +/-Rm, LSL #<shift imm>	5.500E-09	2.027E-09	55	100	1E+08	0.255	1.445

0.178
0.251
0.254
0.18
0.251
0.255
0.181
0.251
0.255

0.228

STRBT	T_{inst} (sec)	E_{inst} (J)	T_{run} (sec)	N_{inst}	N_{iter}	Current (A)	Voltage (V)
Immediate Offset STRBT Rd, [Rn, # +/-<12 bit offset>]	N/A						
Register Offset STRBT Rd, [Rn, +/-Rm]	N/A						
Scaled register offsets STRBT Rd, [Rn, +/-Rm, <shift> #<shift imm>]	N/A						
Immediate pre-indexed STRBT Rd, [Rn, # +/-<12 bit offset>]!	N/A						
Register pre-indexed STRBT Rd, [Rn, +/-Rm]!	N/A						
Scaled register pre-indexed STRBT Rd, [Rn, +/-Rm, LSL #<shift imm>]!	N/A						
Immediate post-indexed STRBT Rd, [Rn], # +/-<12 bit offset>	1.250E-07	3.306E-08	50	4	1E+08	0.181	1.461
Register post-indexed STRBT Rd, [Rn], +/-Rm	6.000E-09	2.176E-09	30	50	1E+08	0.251	1.445
Scaled register post-indexed STRBT Rd, [Rn], +/-Rm, LSL #<shift imm>	5.500E-09	2.027E-09	55	100	1E+08	0.255	1.445

0.181
0.251
0.255

0.229

STRT	T_{inst} (sec)	E_{inst} (J)	T_{run} (sec)	N_{inst}	N_{iter}	Current (A)	Voltage (V)
Immediate Offset STRT Rd, [Rn, # +/-<12 bit offset>]	N/A						
Register Offset STRT Rd, [Rn, +/-Rm]	N/A						

Scaled register offsets STRT Rd, [Rn, +/-Rm, <shift> #<shift imm>]	N/A							
Immediate pre-indexed STRT Rd, [Rn, # +/-<12 bit offset>]!	N/A							
Register pre-indexed STRT Rd, [Rn, +/-Rm]!	N/A							
Scaled register pre-indexed STRT Rd, [Rn, +/-Rm, LSL #<shift imm>]!	N/A							
Immediate post-indexed STRT Rd, [Rn], # +/-<12 bit offset>	1.275E-07	3.390E-08	51	4	1E+08	0.182	1.461	0.182
Register post-indexed STRT Rd, [Rn], +/-Rm	5.800E-09	2.120E-09	29	50	1E+08	0.253	1.445	0.253
Scaled register post-indexed STRT Rd, [Rn], +/-Rm, LSL #<shift imm>	5.600E-09	2.072E-09	56	100	1E+08	0.256	1.445	0.256
								0.230

Load and Store Halfword and Load Signed Byte Instructions: Addressing Mode 3

LDRH	N/A
LDRSB	N/A
LDRSH	N/A
STRH	N/A

Load and Store Multiple Instructions: Addressing Mode 4

LDM	T _{inst} (sec)	E _{inst} (J)	T _{run} (sec)	N _{inst}	N _{iter}	Current (A)	Voltage (V)	
Increment After LDMIA	1.070E-08	3.993E-09	107	100	1E+08	0.259	1.441	0.259
Increment Before LDMIB	1.080E-08	3.943E-09	108	100	1E+08	0.253	1.443	0.253
Decrement After LDMDA	1.070E-08	3.465E-09	107	100	1E+08	0.2235	1.449	0.2235

Decrement Before LDMDB	1.080E-08	3.322E-09	108	100	1E+08	0.212	1.451
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0.212
0.237

STM	T_{inst} (sec)	E_{inst} (J)	T_{run} (sec)	N_{inst}	N_{iter}	Current (A)	Voltage (V)
Increment After STMIA	1.080E-08	3.948E-09	108	100	1E+08	0.2535	1.442
Increment Before STMIB	1.070E-08	3.963E-09	107	100	1E+08	0.257	1.441
Decrement After STMDA	1.080E-08	3.566E-09	108	100	1E+08	0.228	1.448
Decrement Before STMDB	1.270E-07	3.226E-08	127	10	1E+08	0.174	1.460

0.2535
0.257
0.228
0.174
0.228

Status Register Access Instructions

MRS	T_{inst} (sec)	E_{inst} (J)	T_{run} (sec)	N_{inst}	N_{iter}	Current (A)	Voltage (V)
MRS Rd, CPSR	5.600E-09	1.414E-09	56	100	1E+08	0.173	1.460
MRS Rd, SPSR	5.500E-09	1.397E-09	55	100	1E+08	0.174	1.460

0.173
0.174
0.174

MSR	T_{inst} (sec)	E_{inst} (J)	T_{run} (sec)	N_{inst}	N_{iter}	Current (A)	Voltage (V)
MSR CPSR_f, #32 BIT IMMEDIATE	1.620E-08	3.875E-09	81	50	1E+08	0.1636	1.462
MSR CPSR_<fields>, Rm	1.640E-08	3.956E-09	82	50	1E+08	0.165	1.462
MSR SPSR_f, #32 BIT IMMEDIATE	5.600E-09	1.414E-09	56	100	1E+08	0.173	1.460
MSR SPSR_<fields>, Rm	5.500E-09	1.405E-09	55	100	1E+08	0.175	1.460

0.1636
0.165
0.173
0.175
0.169

Semaphore Instructions

	T_{inst} (sec)	E_{inst} (J)	T_{run} (sec)	N_{inst}	N_{iter}	Current (A)	Voltage (V)
SWP	1.070E-08	3.982E-09	107	100	1E+08	0.257	1.448
SWPB	2.740E-07	2.974E-08	274	10	1E+08	0.073	1.487

0.257
0.073

Branch and NOP instructions

	T_{inst} (sec)	E_{inst} (J)	T_{run} (sec)	N_{inst}	N_{iter}	Current (A)	Voltage (V)
B	1.070E-08	2.653E-09	107	100	1E+08	0.169	1.467
NOP	5.500E-09	1.388E-09	55	100	1E+08	0.172	1.467

0.169
0.172
0.1705

1.779E-01 0.196 0.197

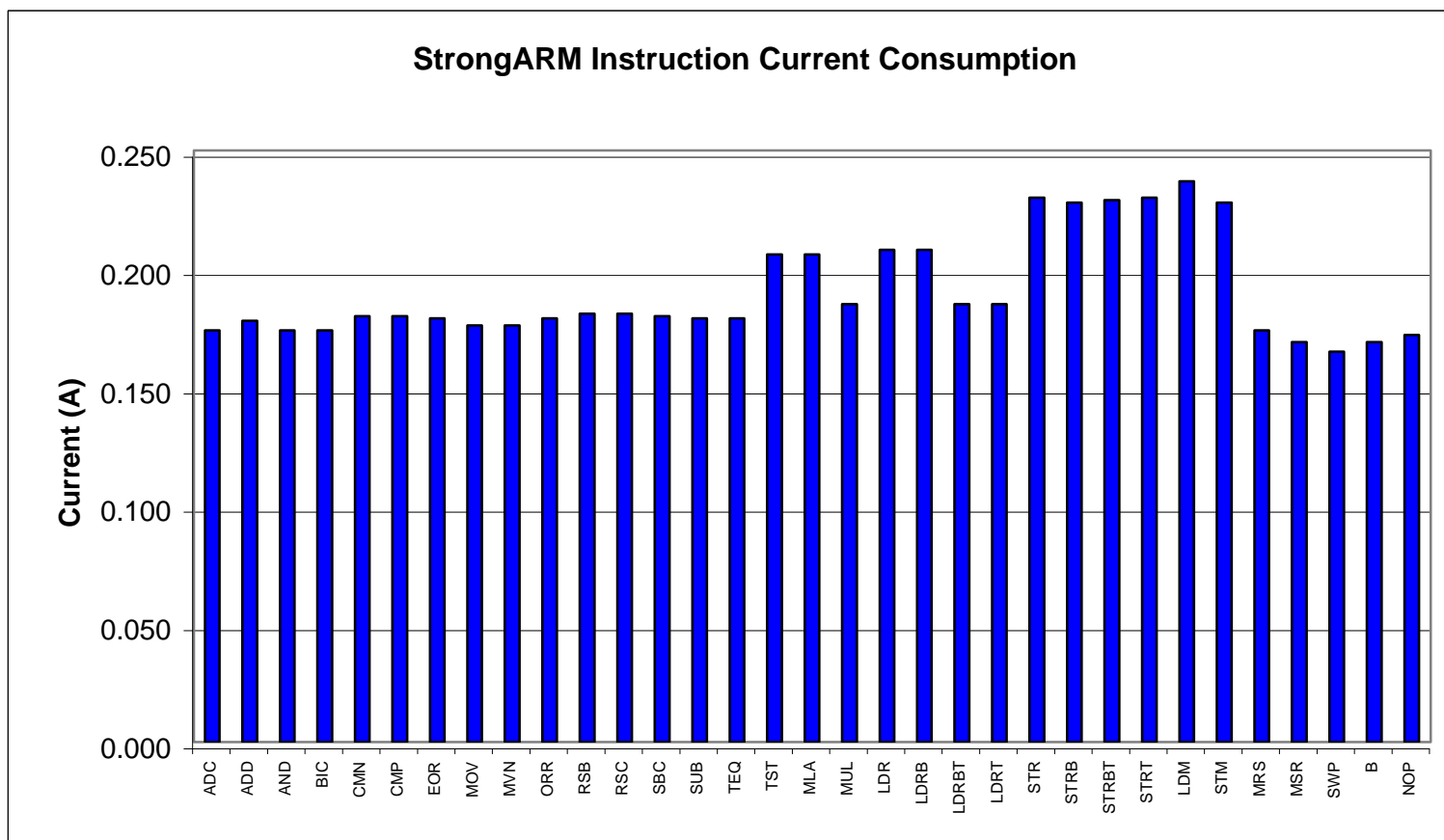
0.170

Instruction Current Consumption by Group

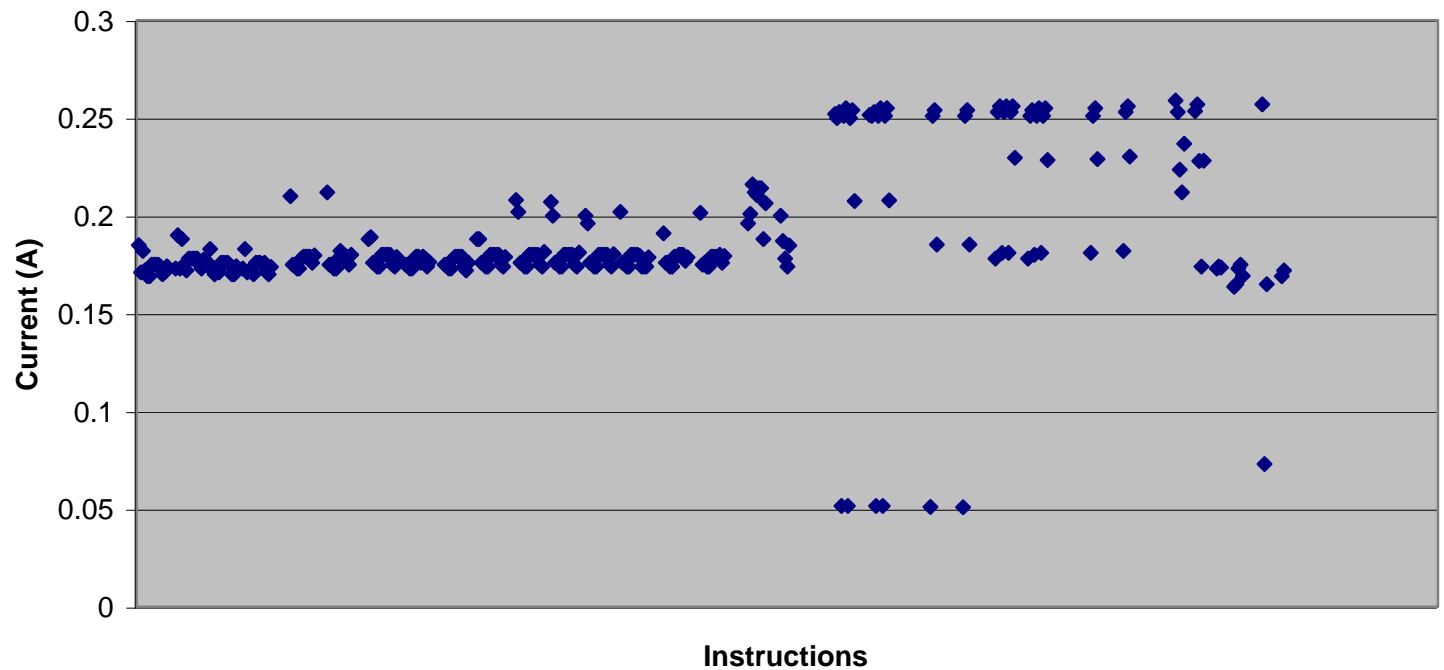
Instruction	Current (A)
ADC	0.174
ADD	0.178
AND	0.174
BIC	0.174
CMN	0.180
CMP	0.180
EOR	0.179
MOV	0.176
MVN	0.176
ORR	0.179
RSB	0.181
RSC	0.181
SBC	0.180
SUB	0.179
TEQ	0.179
TST	0.206
MLA	0.206
MUL	0.185
LDR	0.208
LDRB	0.208
LDRBT	0.185
LDRT	0.185
STR	0.230
STRB	0.228
STRBT	0.229
STRT	0.230

LDM	0.237
STM	0.228
MRS	0.174
MSR	0.169
SWP	0.165
B	0.169
NOP	0.172

Average	0.1904
Range (Max-Min)	0.0720
% Range over Average	37.810



StrongARM SA-1100 Instruction Current Consumption



	ADD	AND	MOV	MLA
	0.173	0.176	0.175	0.196
	0.19	0.183	0.175	0.201
	0.173	0.172	0.173	0.216
	0.188	0.170	0.173	0.212
	0.175	0.172	0.178	0.21
	0.172	0.171	0.179	0.214
	0.178	0.176	0.179	0.214
	0.178	0.176	0.179	0.188
	0.178	0.176	0.179	
	0.178	0.176	0.174	
	0.178	0.175	0.172	
	0.175	0.17		
	0.173	0.17		

