A 28nm High-Density 6T SRAM with Optimized Peripheral-Assist Circuits for Operation down to 0.6V

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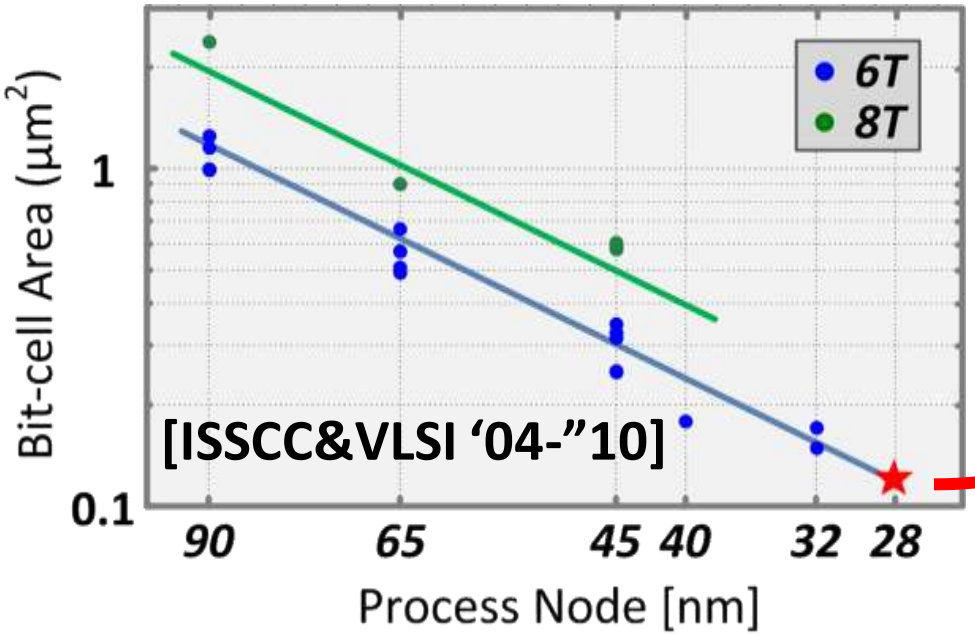
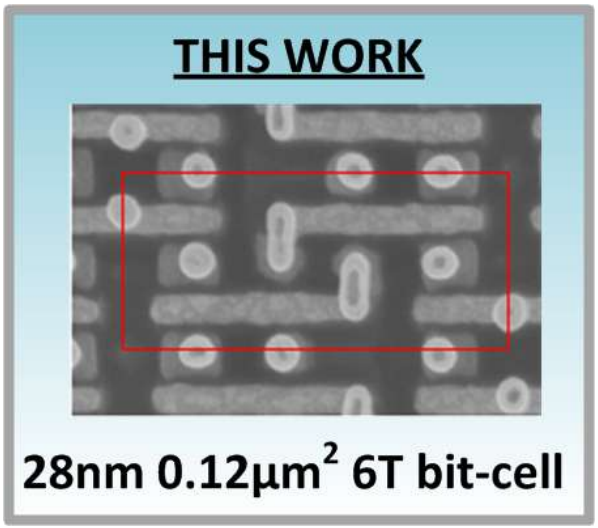
6T vs. 8T Bit-cell





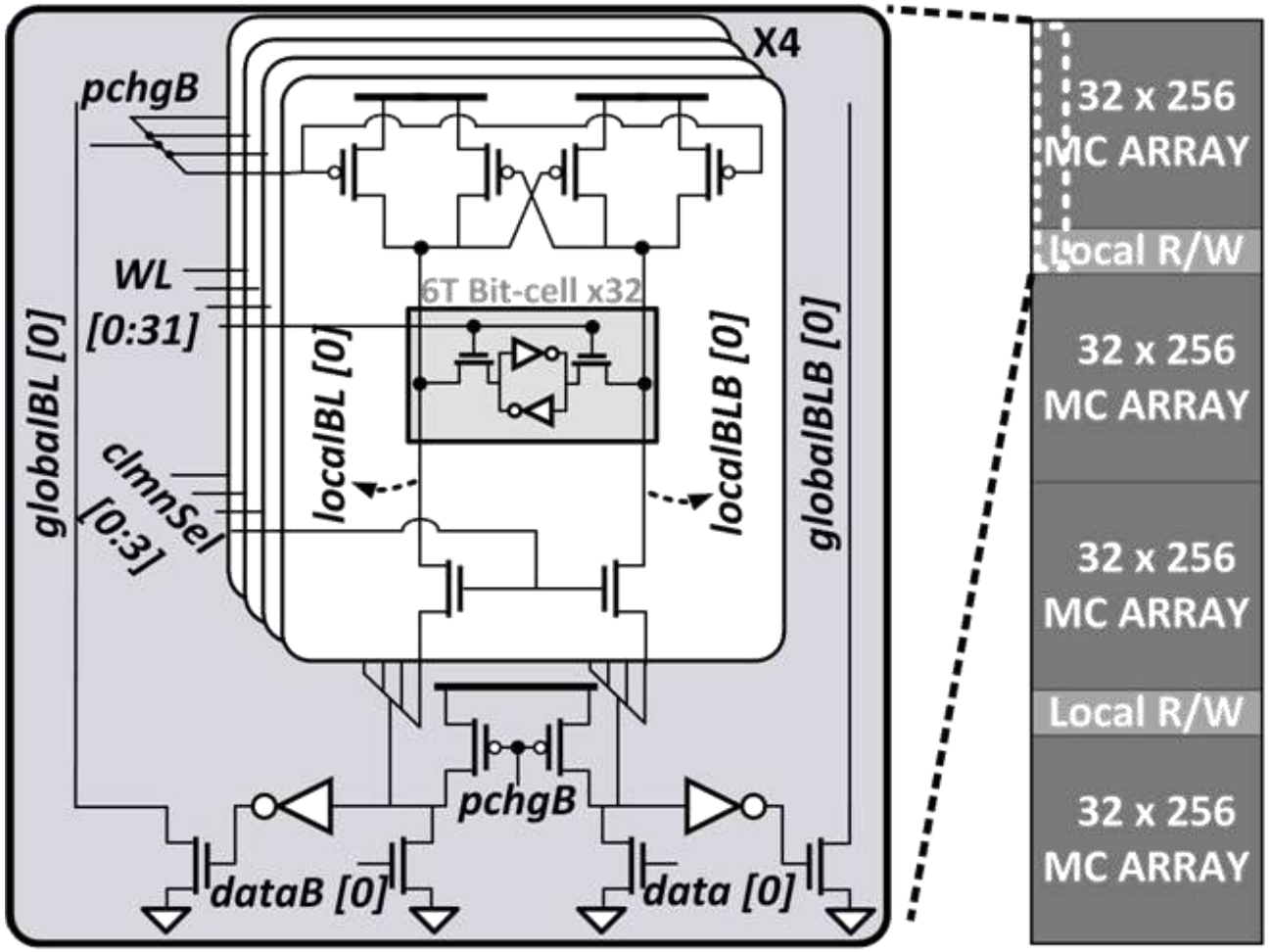
- **8T cell is a good low-voltage alternative at the expense of larger area**
  - *e.g. 40% larger cell area*

Goal: High-density standard 6T bit-cell with peripheral assist circuits for low-voltage operation

Outline

- Array architecture
- Peripheral assist circuits
- Test chip measurement results
- Conclusions

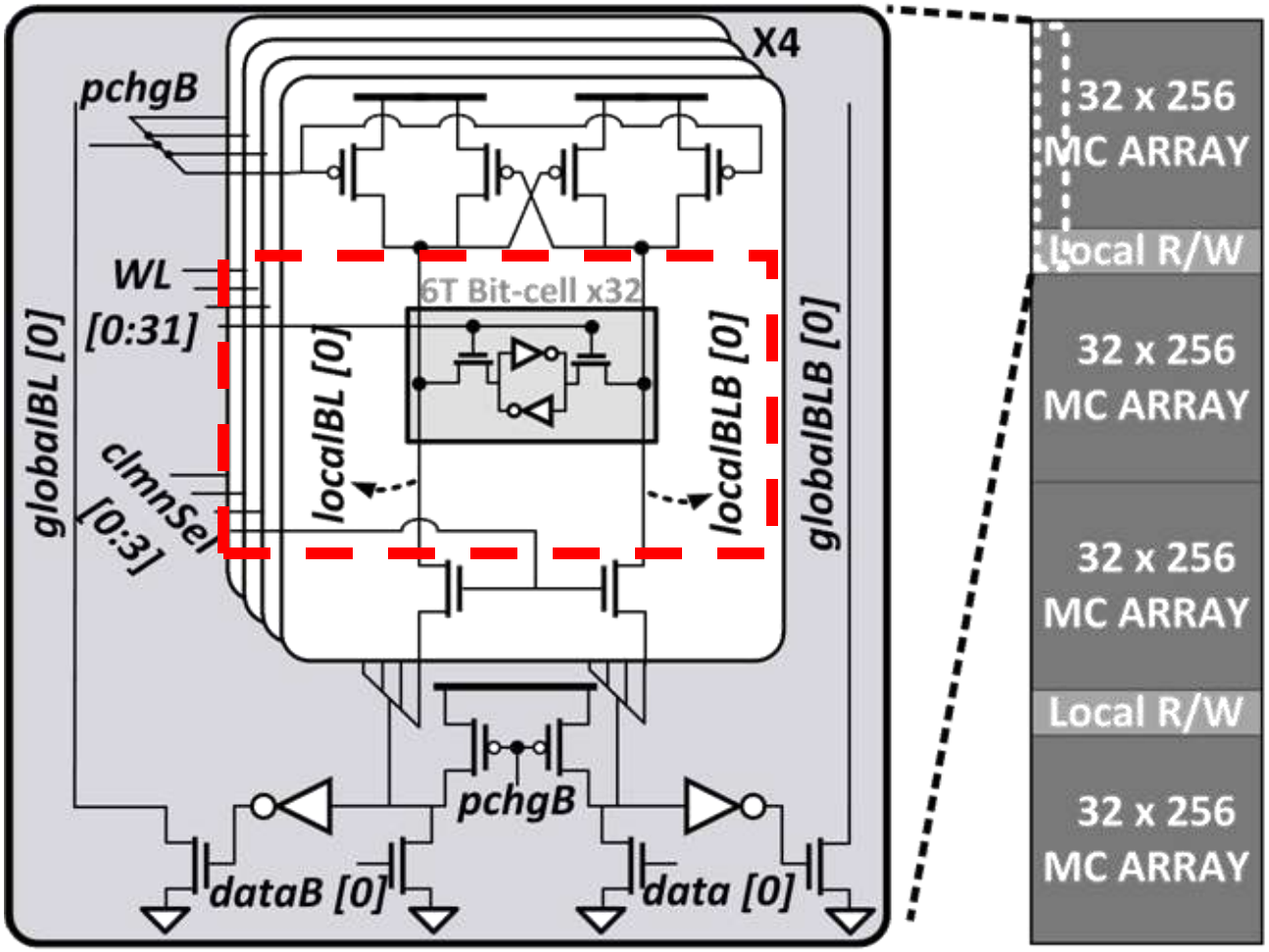
Array Architecture



Peripheral assist circuits enable low-voltage operation

Array Architecture

1) Short local bit-lines protect against read disturbs



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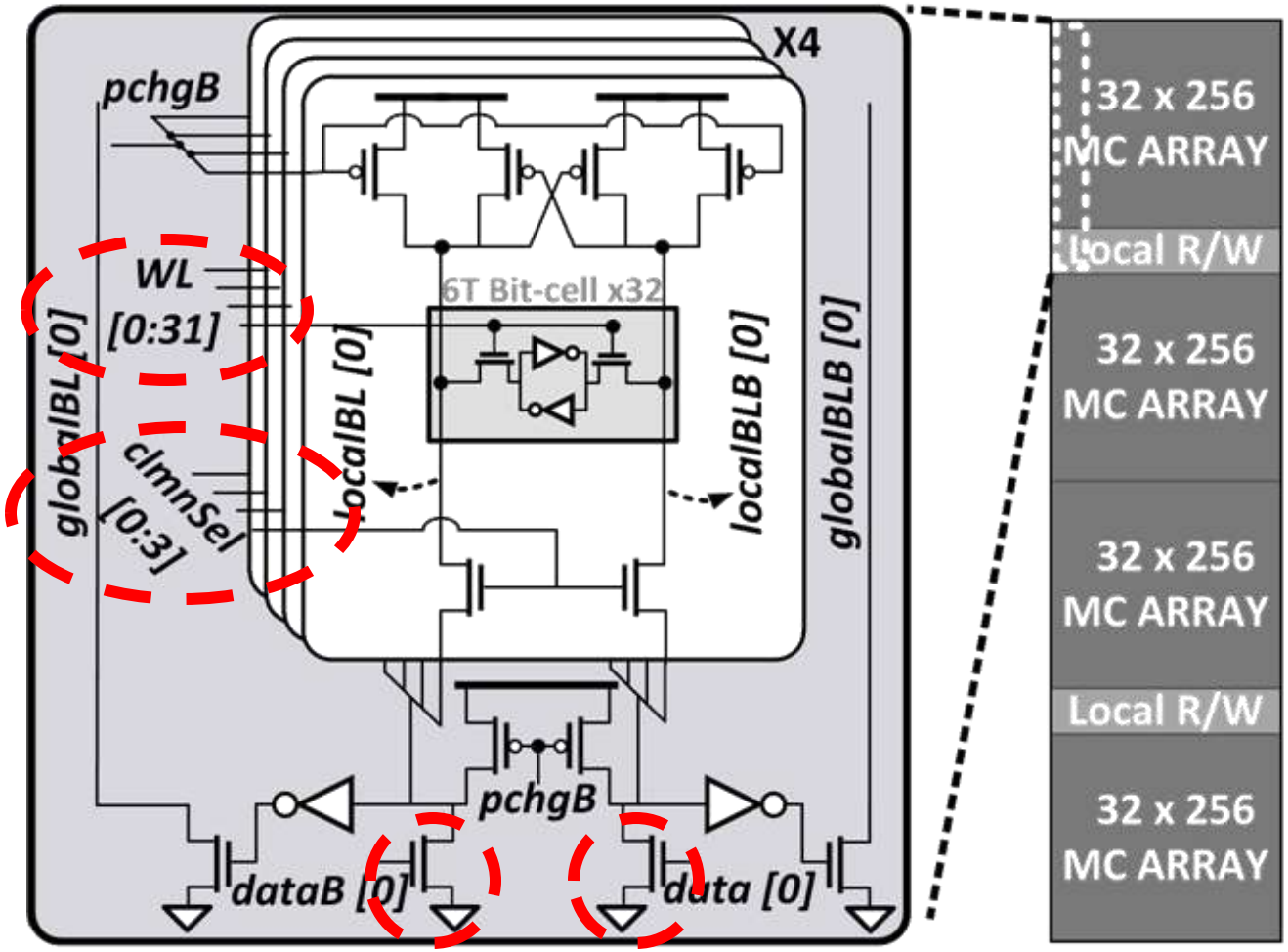
Array Architecture

1) Short local bit-lines protect against read disturbs

2) Voltage boosting for better write-ability



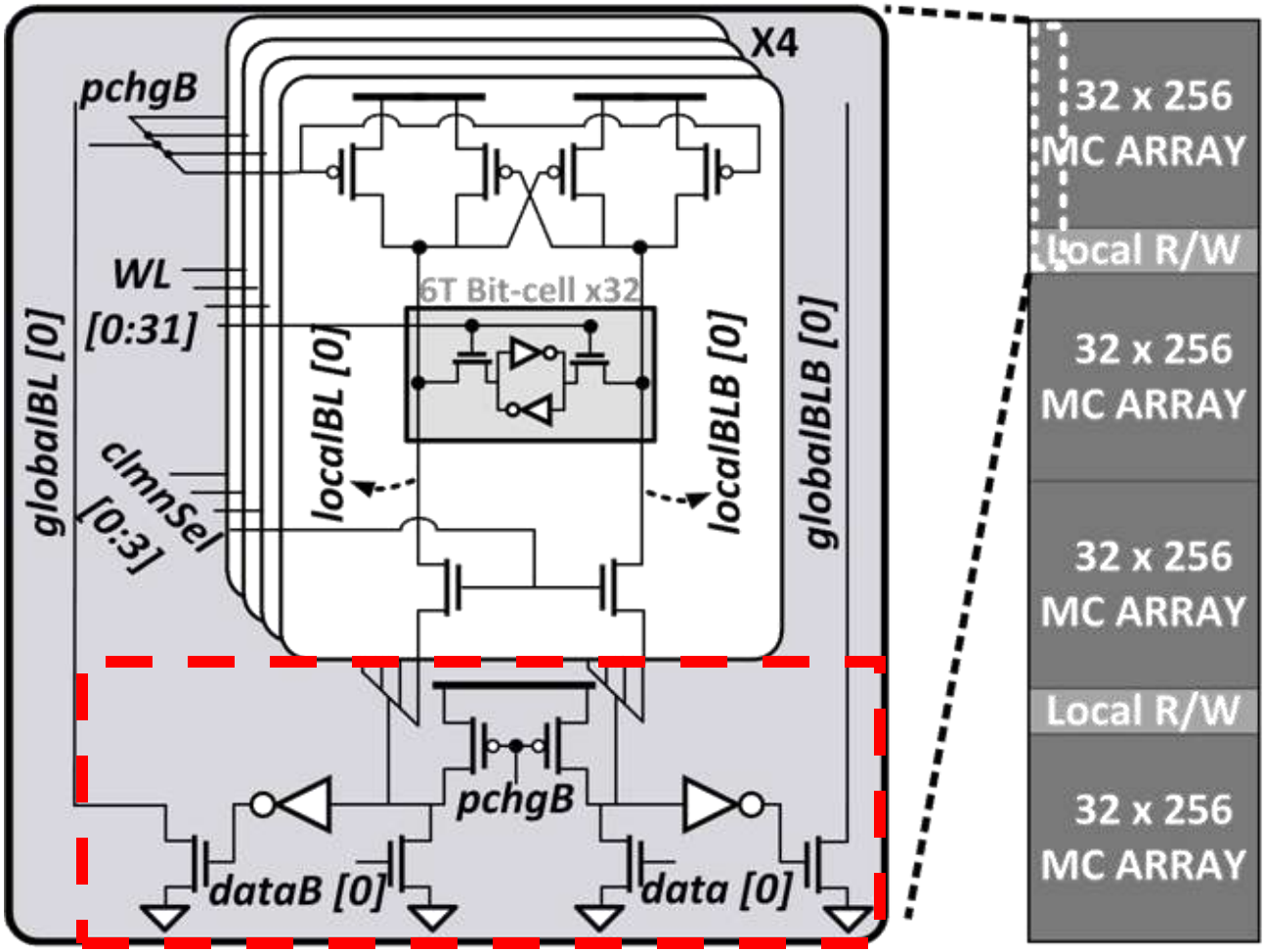
Peripheral assist circuits enable low-voltage operation

Array Architecture

1) Short local bit-lines protect against read disturbs

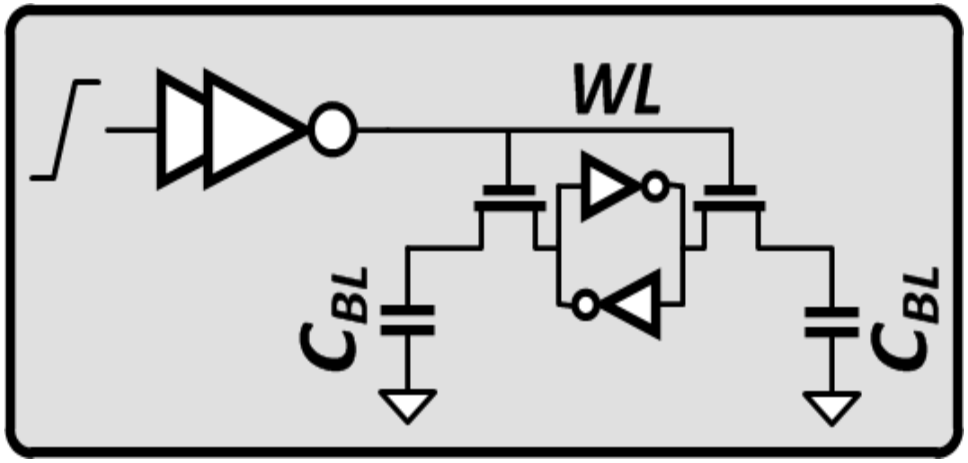
2) Voltage boosting for better write-ability

3) Large-signal local sensing for area efficiency



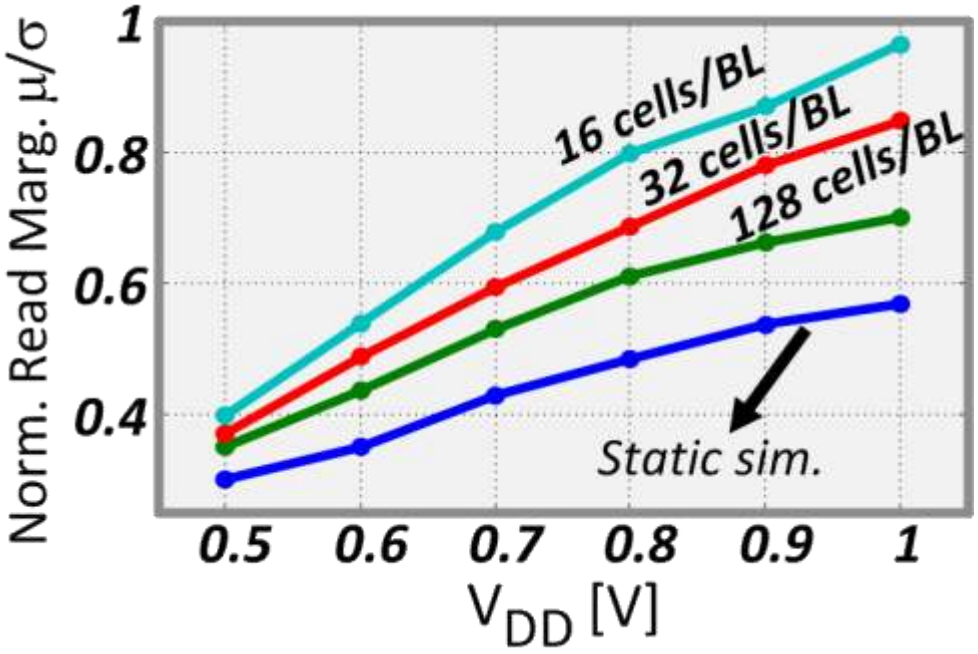
Peripheral assist circuits enable low-voltage operation

Short BLs for Read Disturb



TRANSIENT READ MARGIN SIMULATION

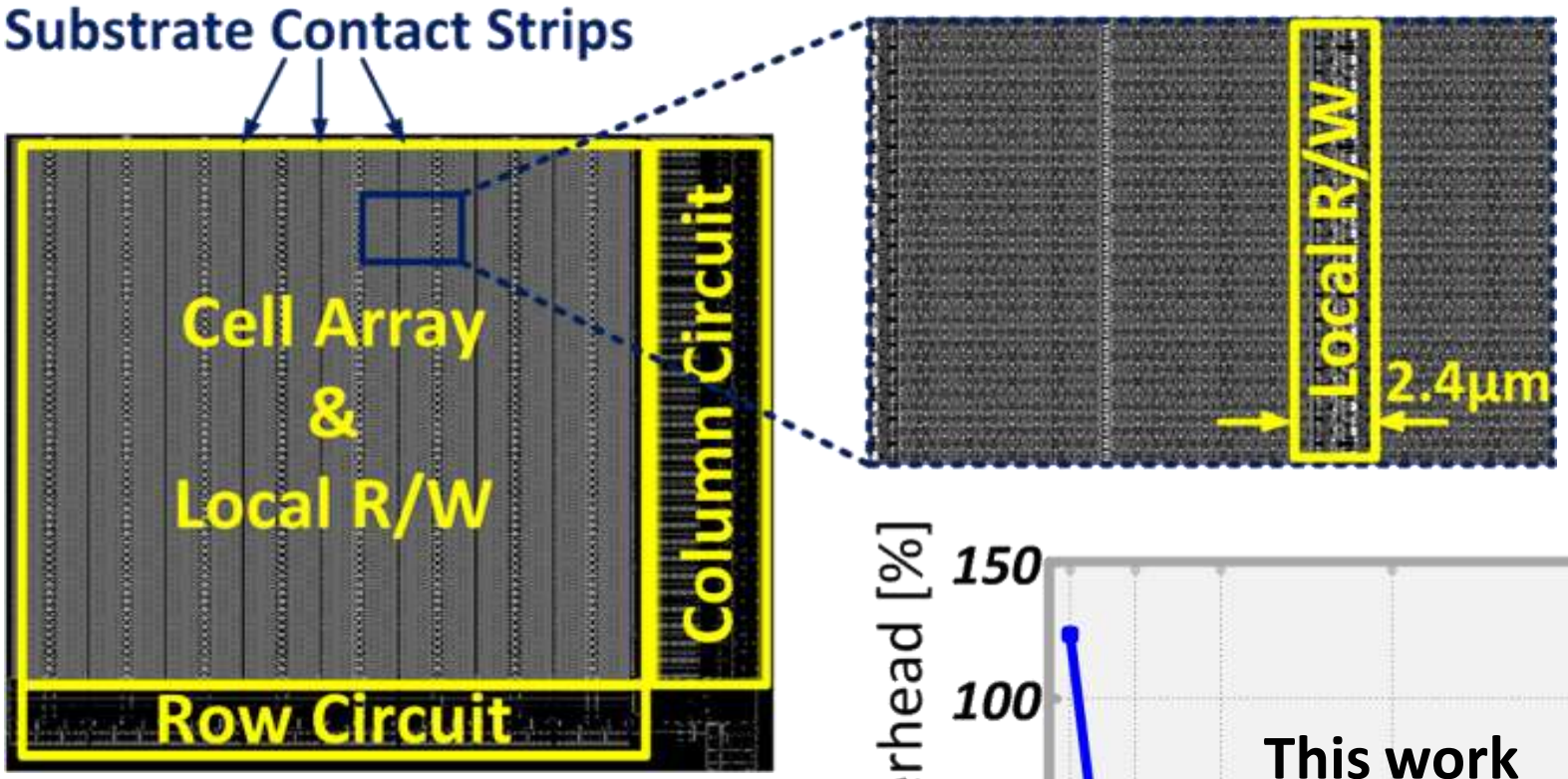
1mV accuracy with three-step search

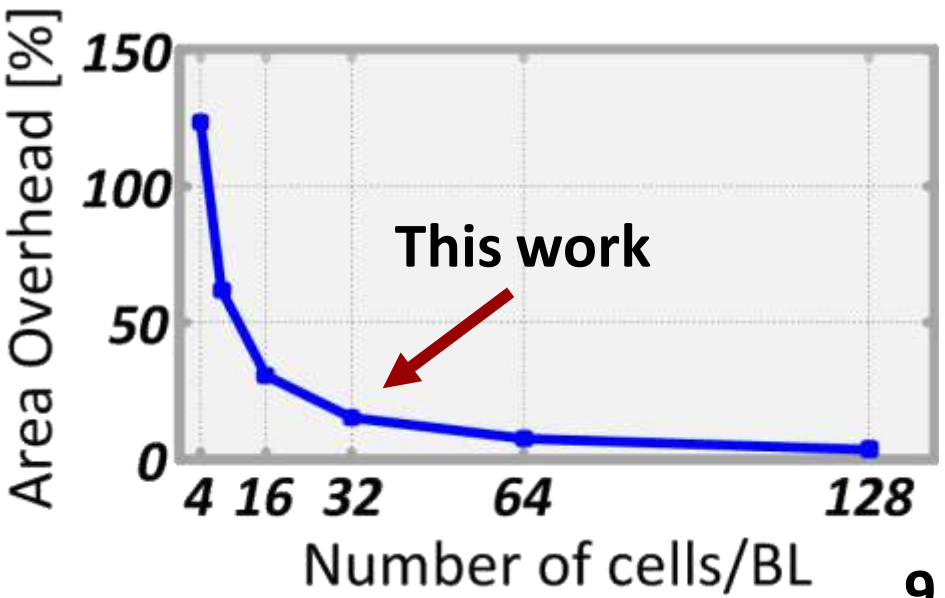


Significant read margin improvement with shorter bit-lines

This Work: 32 cells/BL

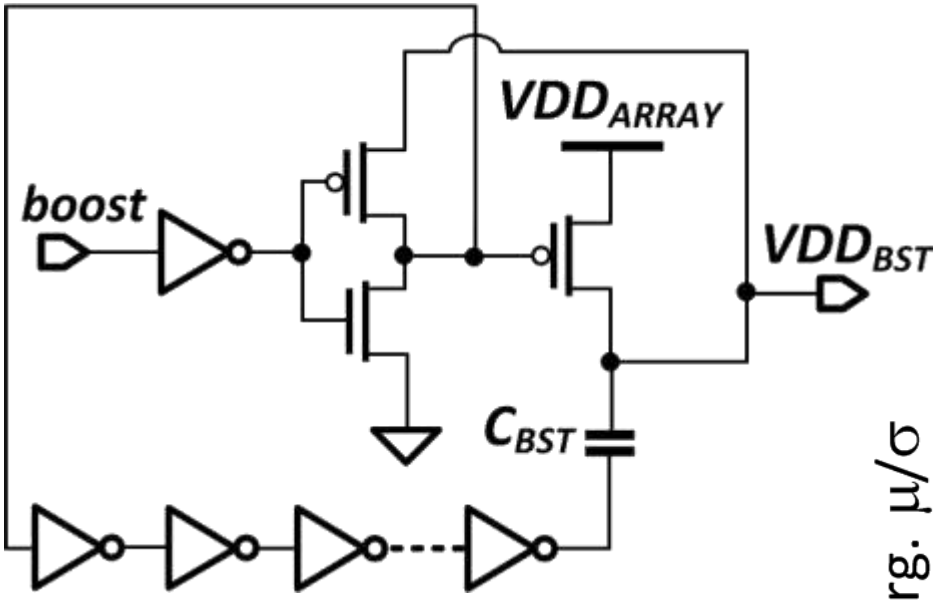
Local R/W Circuit Area Impact



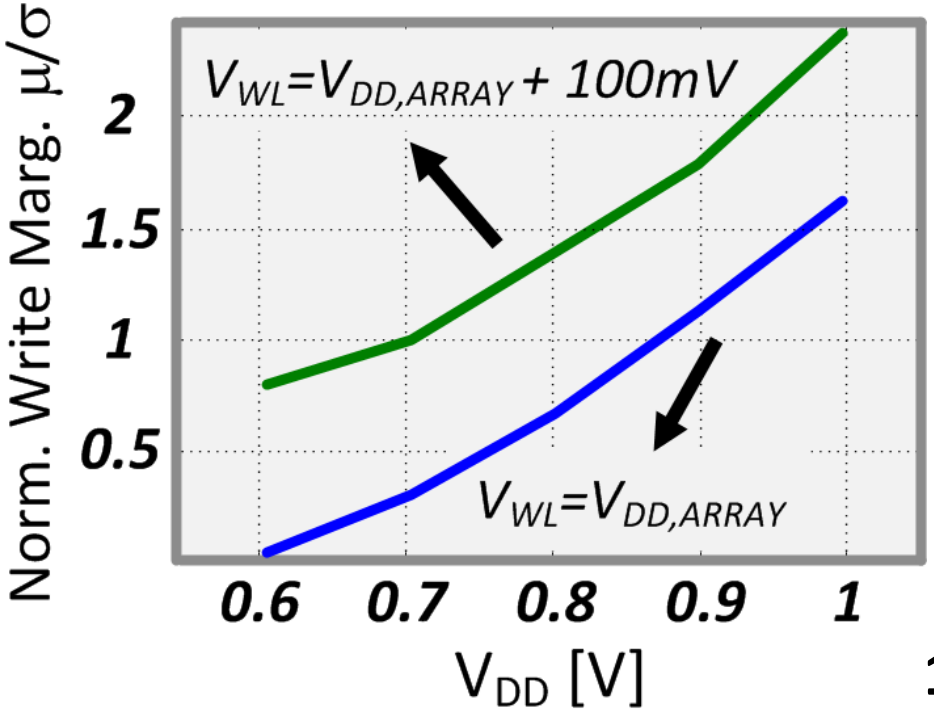


15% area overhead is achieved by careful sizing and layout of local R/W circuitry

Voltage Boosting for Write-ability

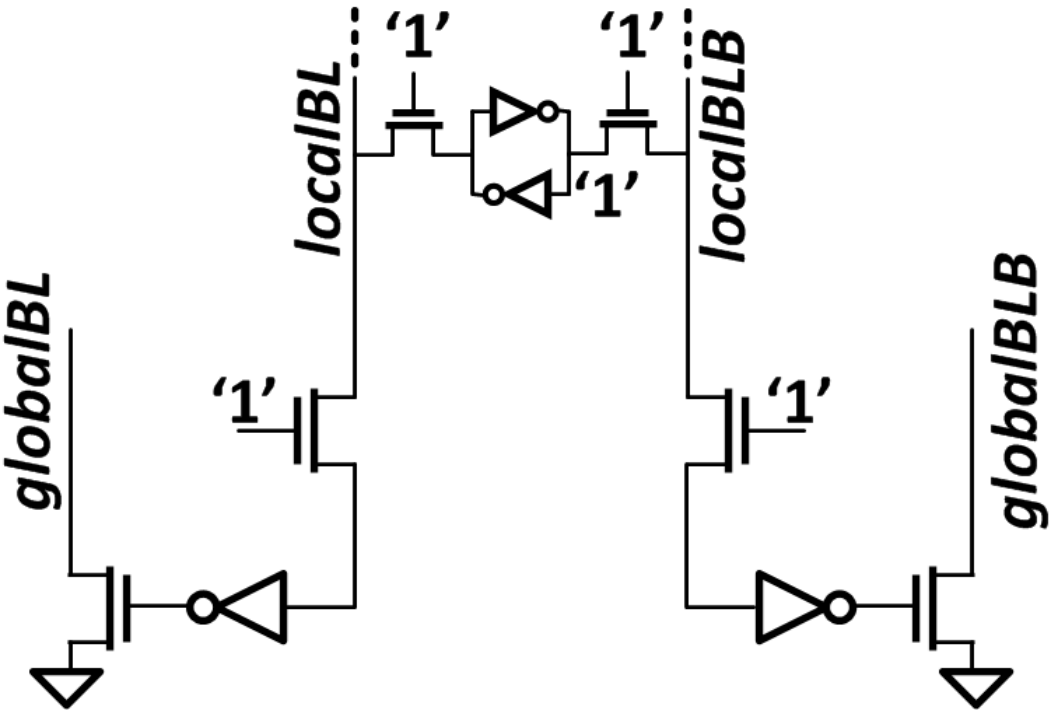


- Boosted voltage, VDD_{BST}, shared across all rows of a sub-block.
- *boost* signal triggered with the negative edge of clk



Write-ability ensured by voltage boosting through shared circuits to limit area overhead

Read Access Time Improvement



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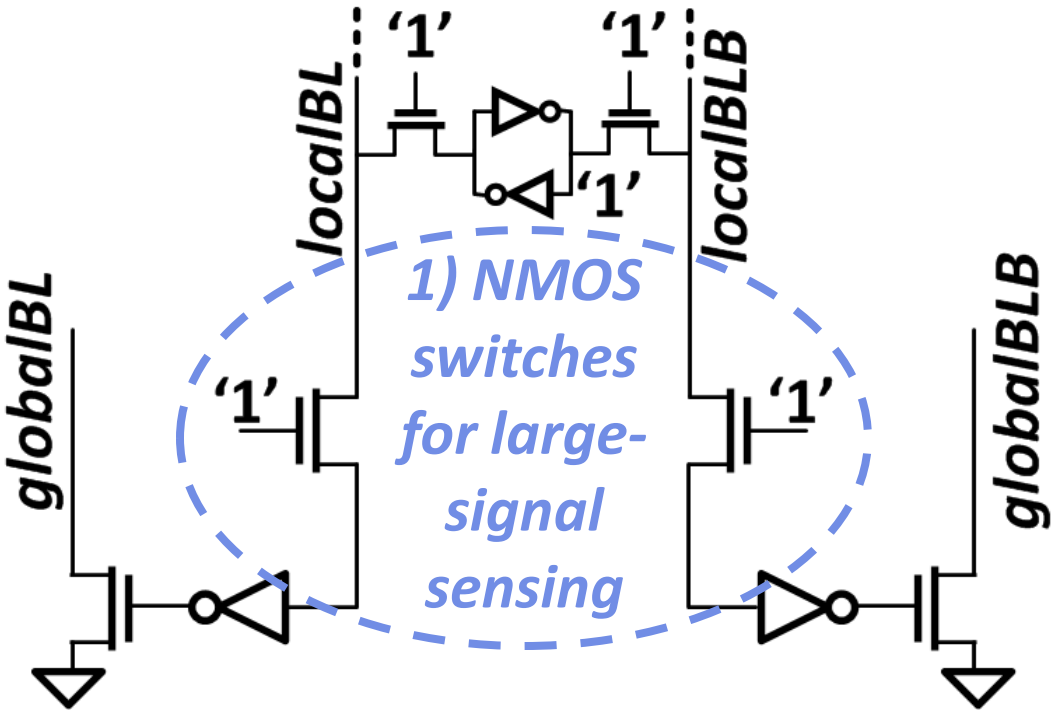

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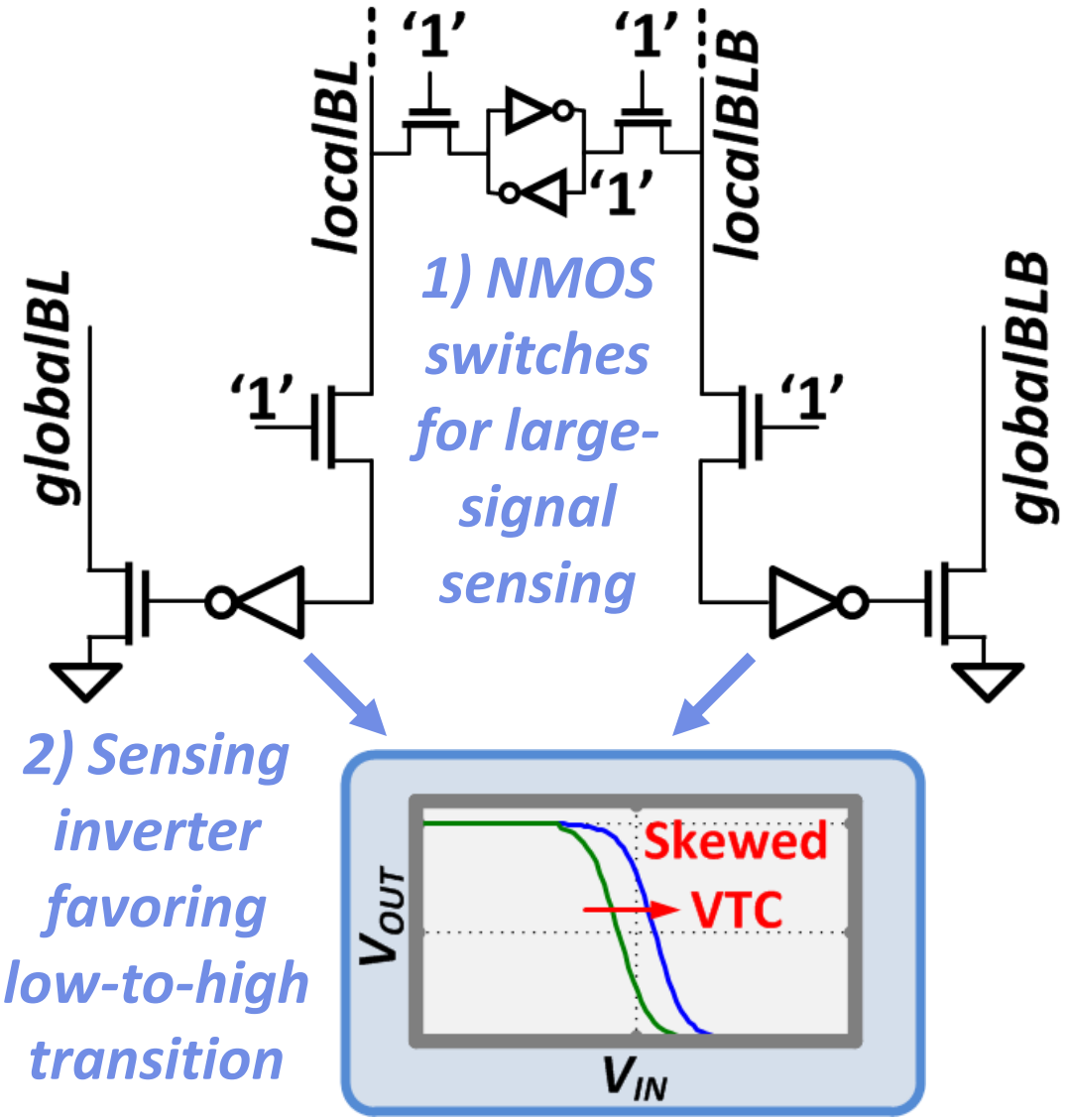

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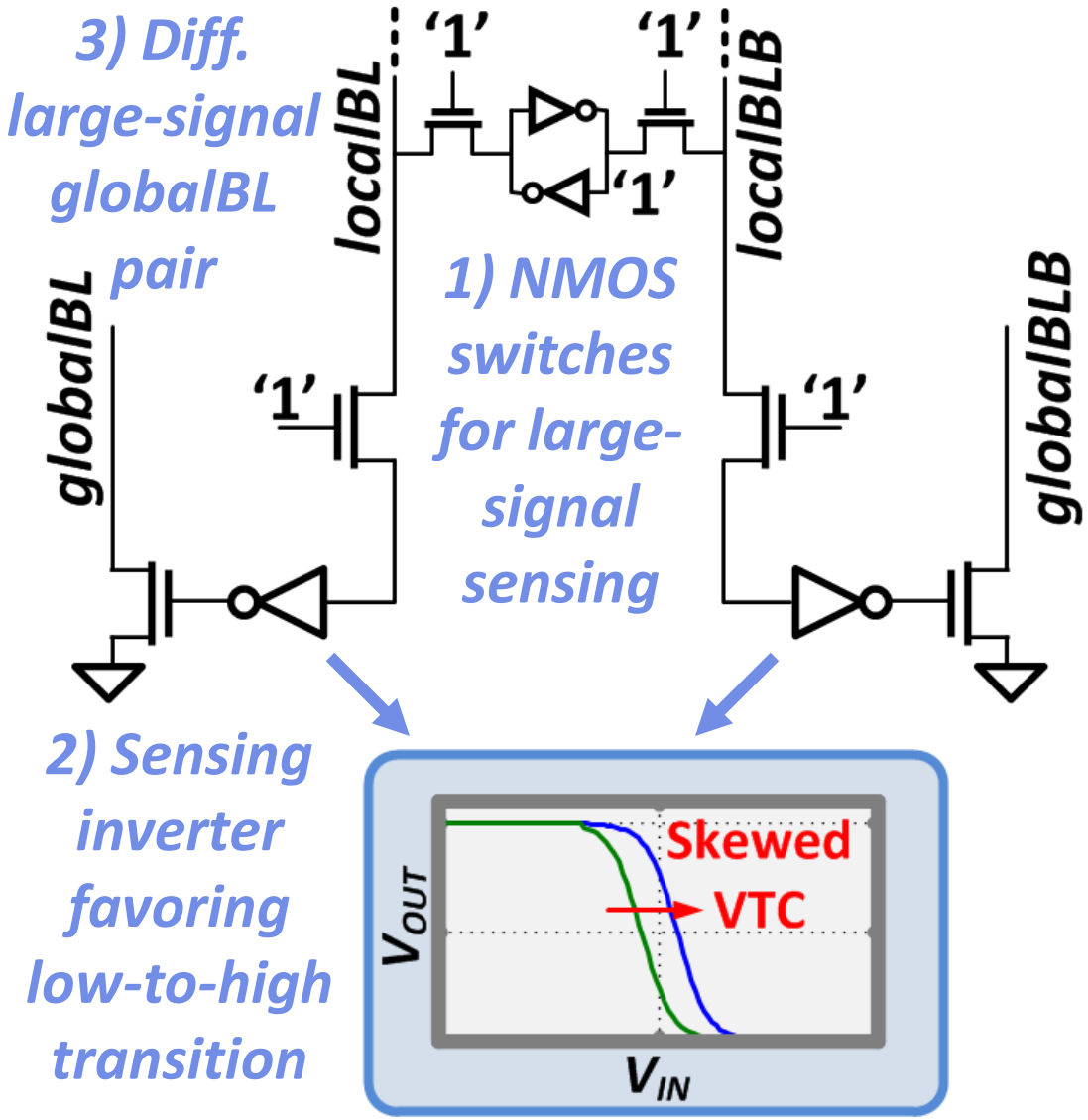

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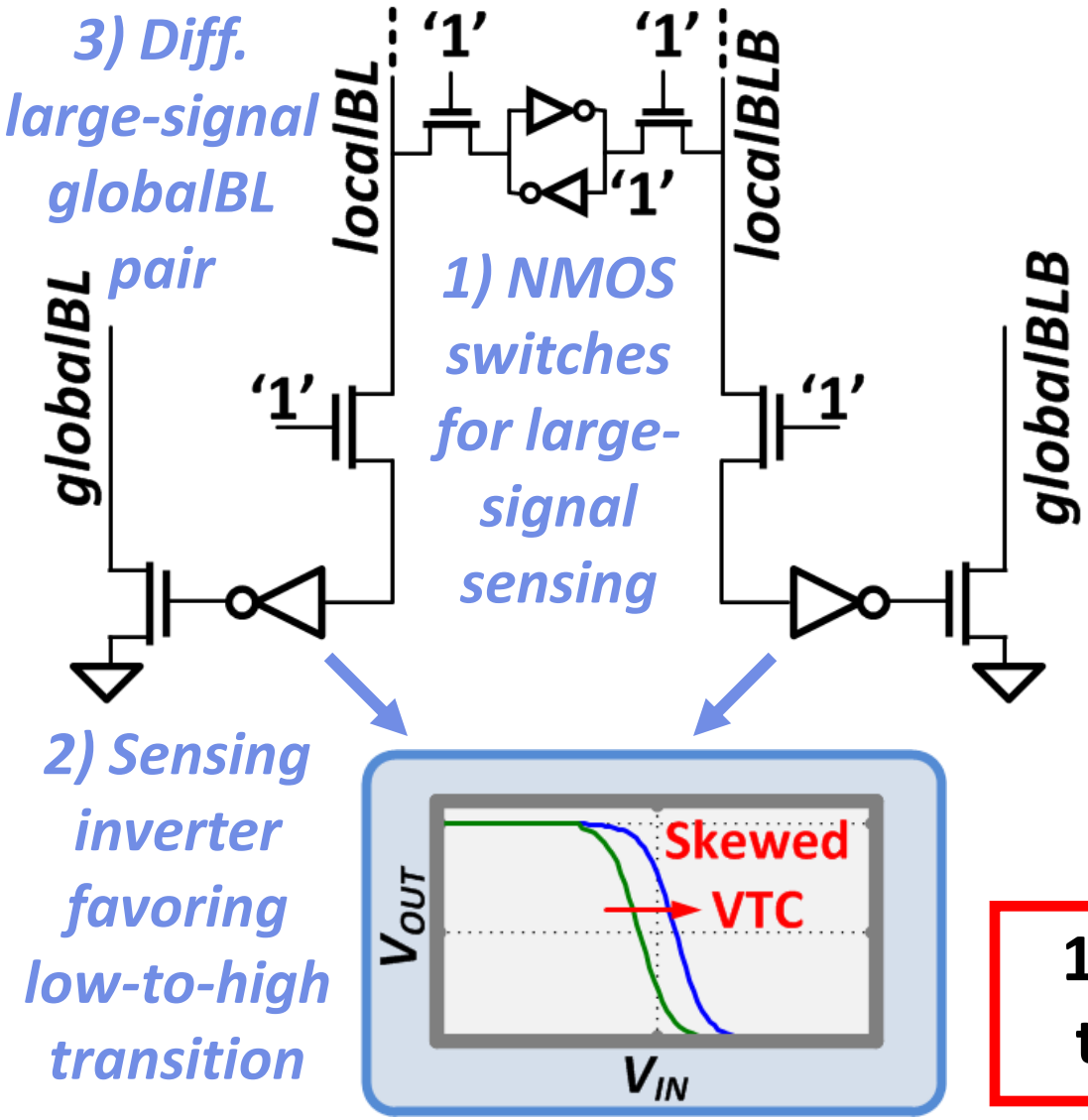
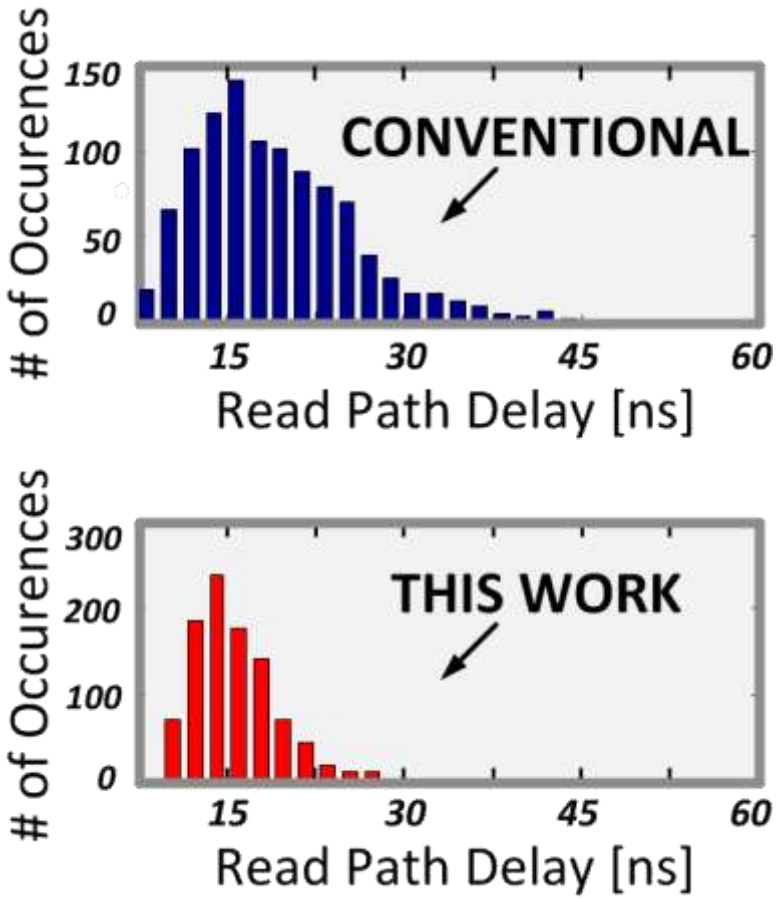
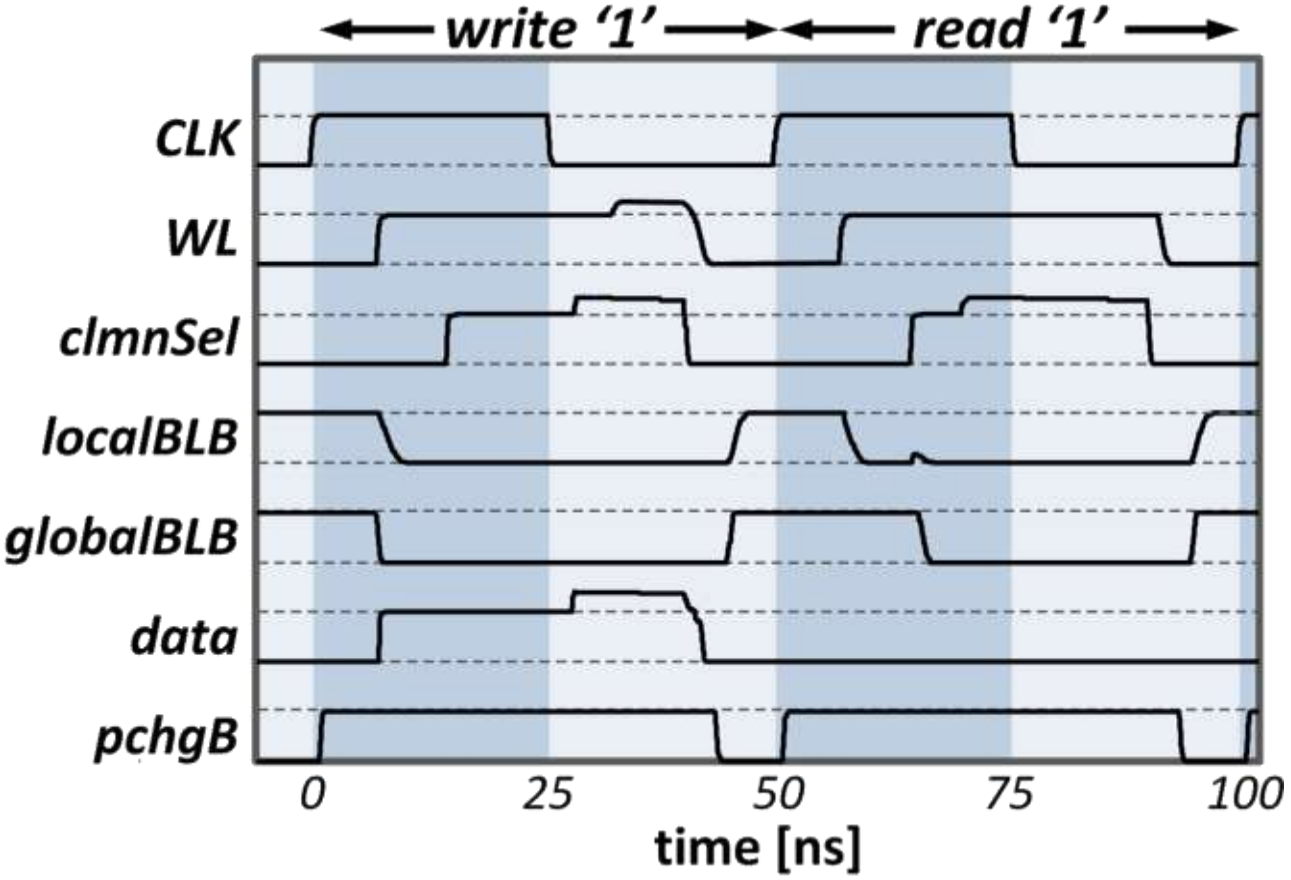




1.8X faster read access time achieved at 0.6V

Simulated Read/Write Waveforms

1) Boosted signals aligned to the negative edge of the clk
2) During read, clmnSel is turned on after a short delay, exposing bit-cell to a smaller capacitance



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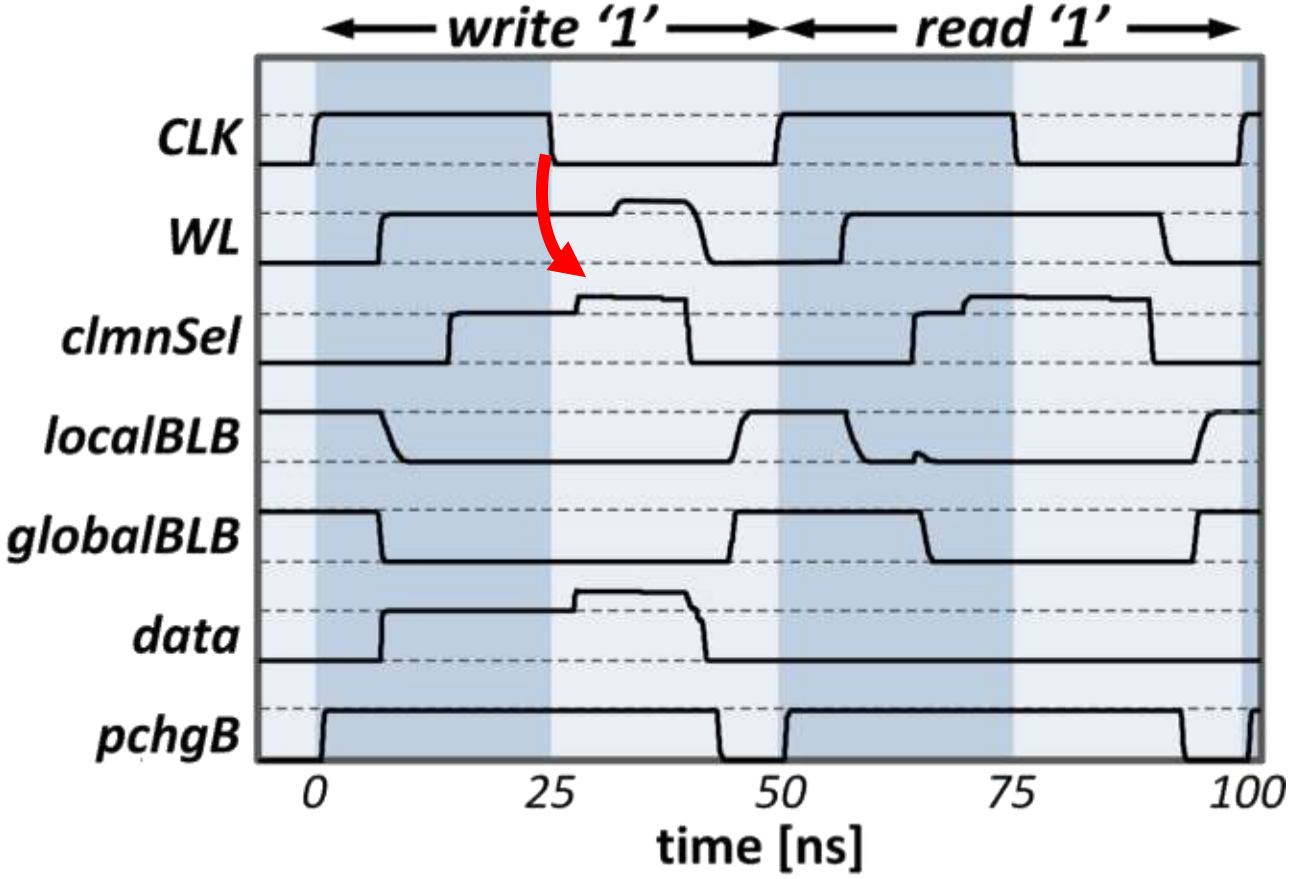

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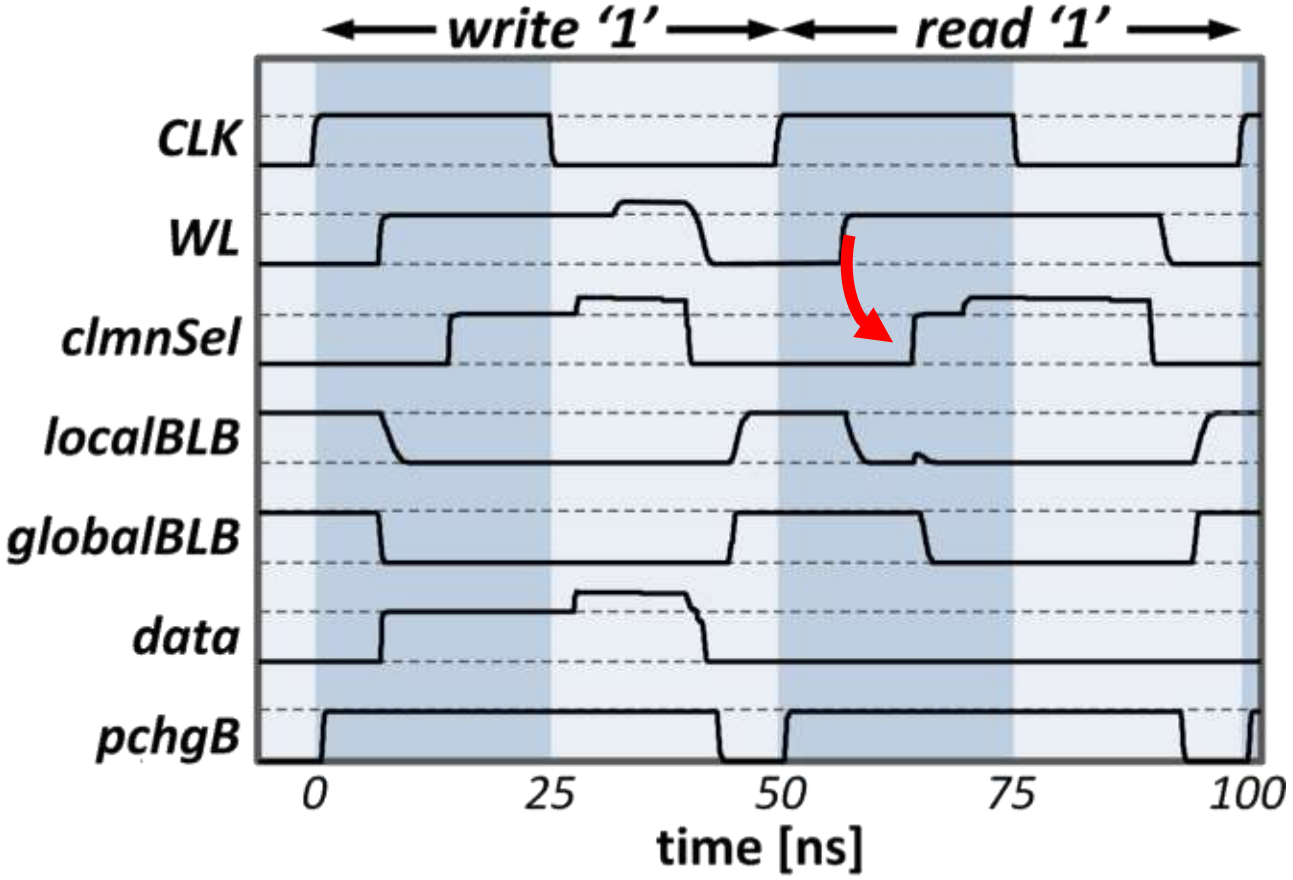
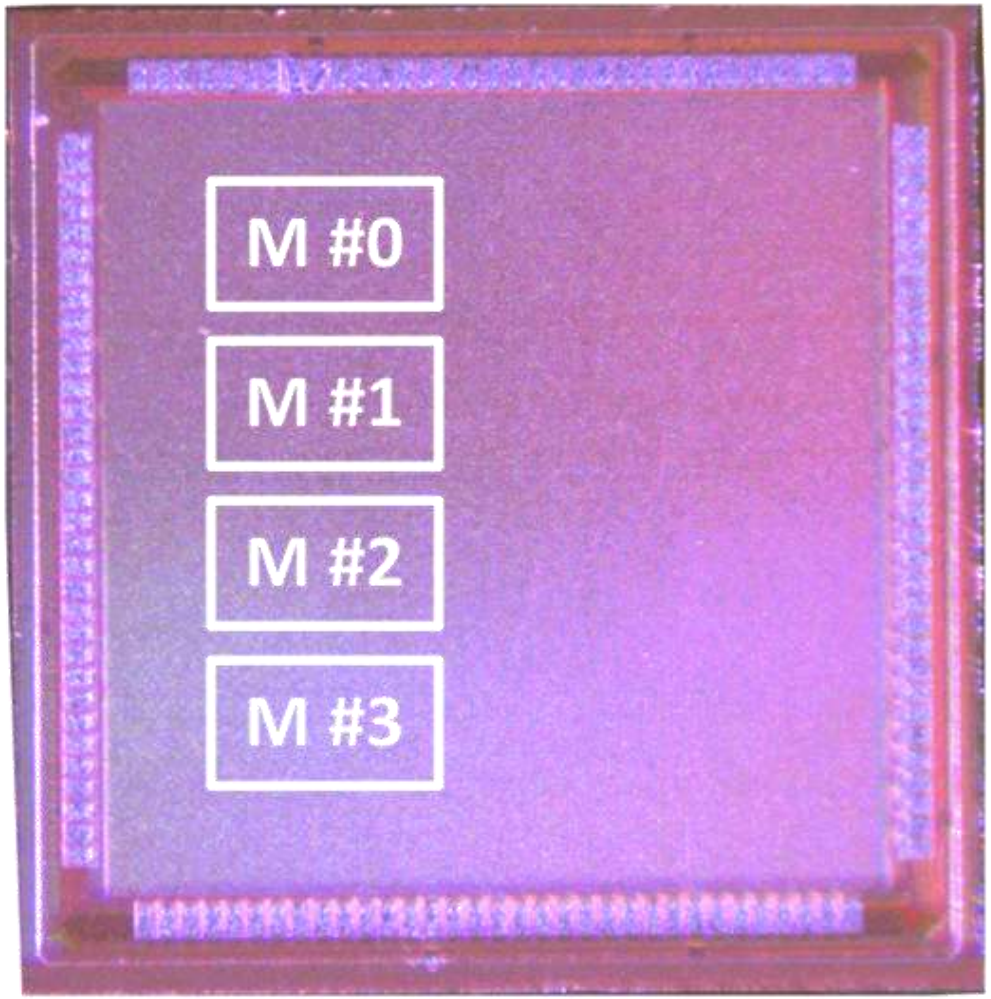


Test Chip Summary

- 28nm Low Standby Power CMOS Process
- 0.12µm² 6T bit-cell
- Die size: 2.3mm x 2.3mm
- Voltage Range: 0.6 to 1V
- Module Size: 128kbit



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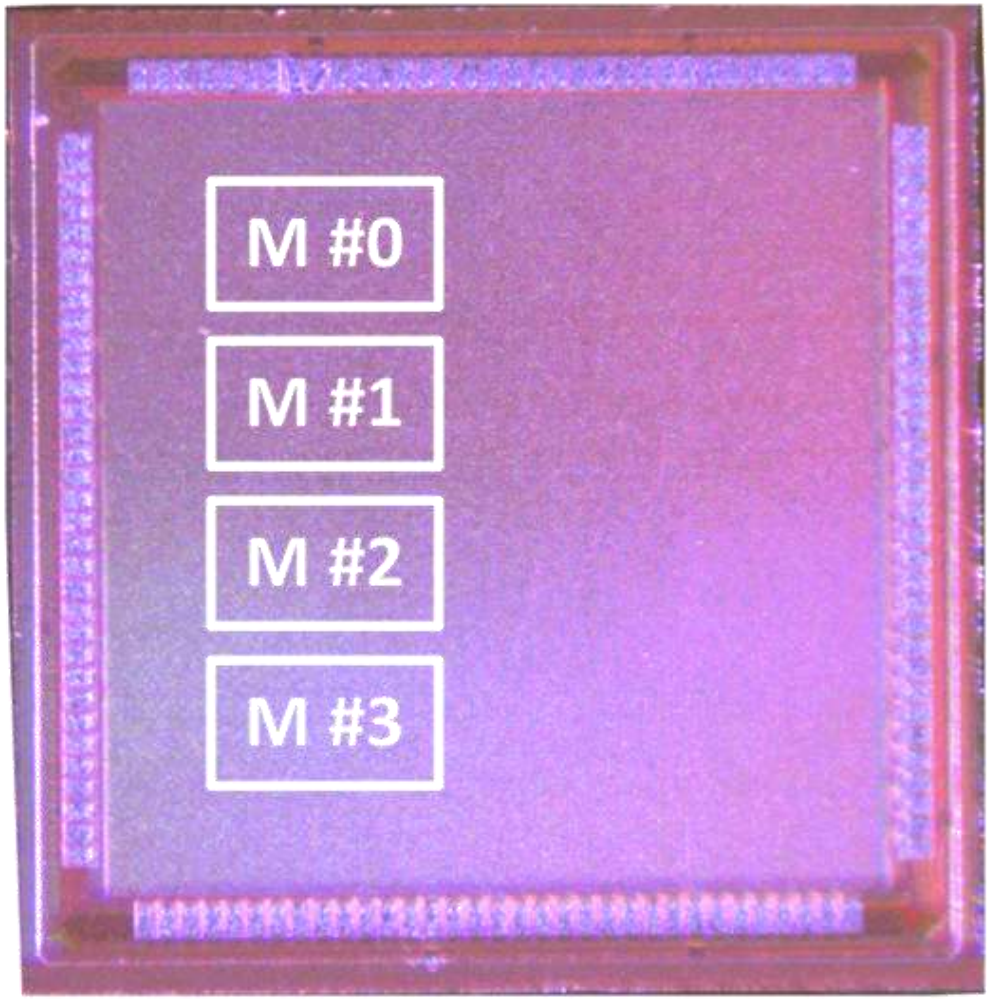
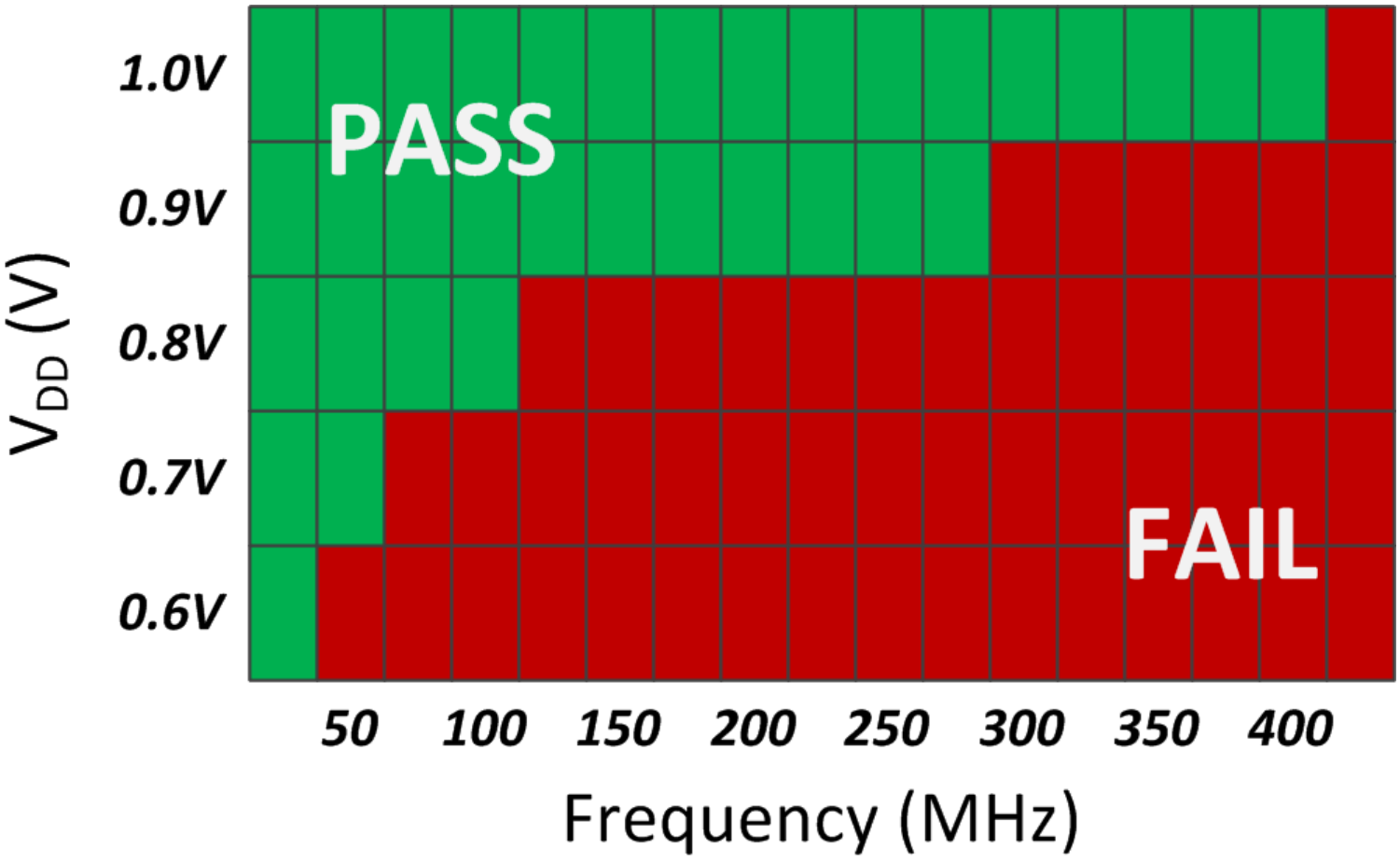
SRAM blocks in this work are also used in a separate DSP chip:

Paper 7.5: A 28nm 0.6V Low-Power DSP for Mobile Applications



Measured Performance

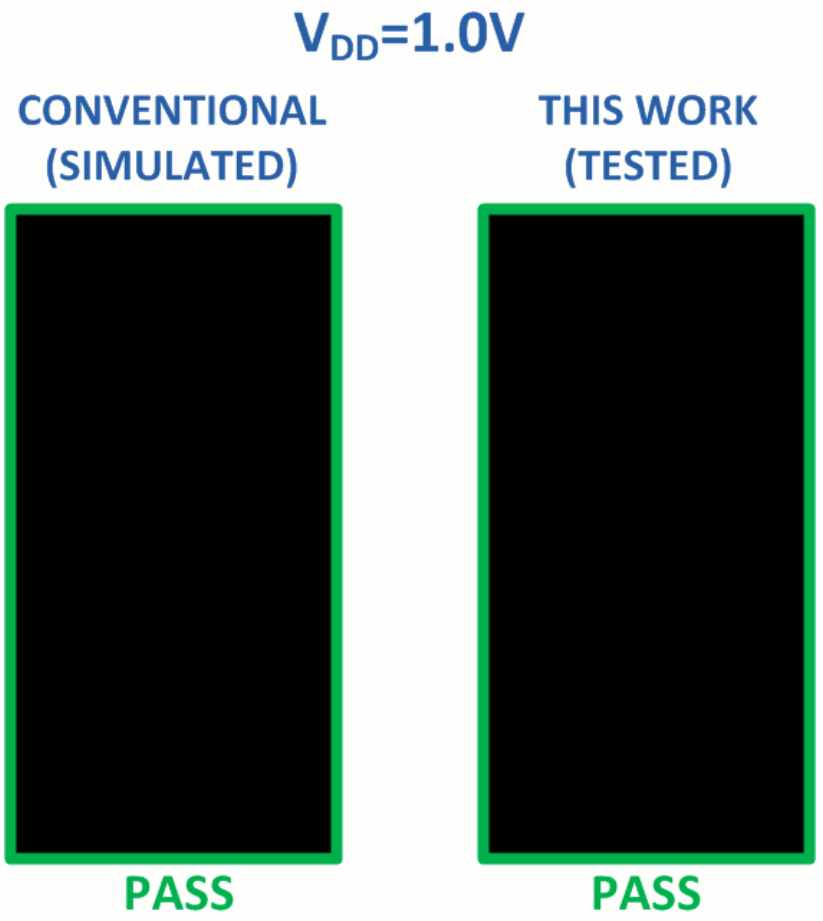
Performance scales from 400MHz to 20MHz



Measured Bit Error Map

- Physical location of bit-cells in the memory array
- 512 Rows x 256 Columns
- Read and write failures (*) in the conventional array due to transistor variation

(*) White color represents failed bits



Proposed techniques extend operating voltage range from 0.9V to 0.6V

Conclusions

- **28nm 6T SRAM constructed with high-density 0.12µm^2 bit-cell**
- **0.6V operation is achieved through peripheral assist circuits**
- **Area-efficient alternative to the 8T SRAMs for low voltage systems**

Acknowledgement: Funding and IC fabrication provided by Texas Instruments, Incorporated

End