# Progress in Copper-Based Wafer Bonding

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# Outline

- Copper Thermo-Compression Bonding
- Reliability of Bonded Cu Layer
- Silicon Multi-Layer Stacking
- Low Temperature Processes
- Dielectric/Copper Hybrid Bonding
- Applications

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- ❑ **Copper Thermo-Compression Bonding**
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# Copper Thermo-compression Bonding

## Metallic bonding

- Electrical and mechanical bond
- *"Via first"* approach, hence lower via aspect ratio and higher via density are possible
- Heat conduit and noise shield

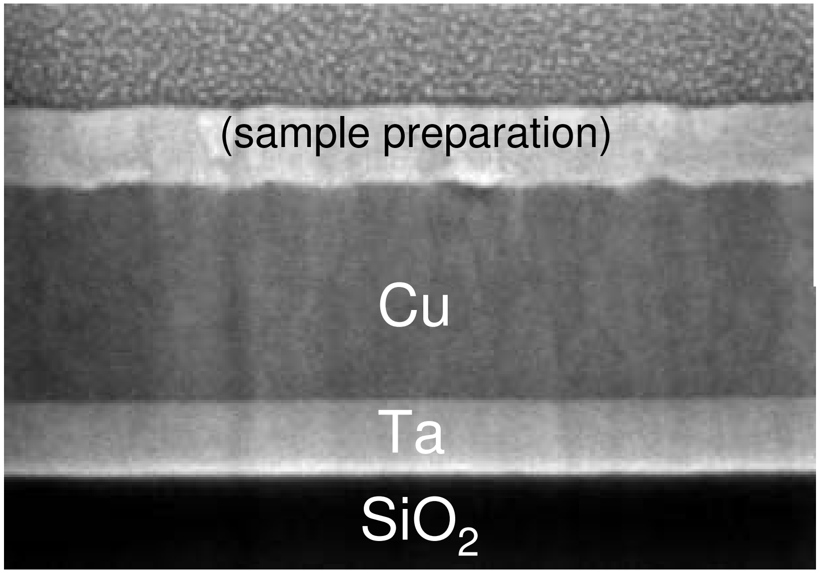
## Copper

- Mainstream CMOS material
- High electrical ($\rho$=1.7 µΩ.cm) and thermal ($K$= 400 W $m^{-1}$ $K^{-1}$) conductivities [Al: 2.8 µΩ.cm, 235 W $m^{-1}$ $K^{-1}$]
- **COPPER BONDS TO ITSELF!!!**

# Bonding Procedures

1. **Bonding –** *single wafer processing*
   - Pressure / Contact Force (*2-4 kN for 6” wafers*)
   - Heating (*300-400 $^oC$*)
   - Duration (*5-60 min*)
   - Ambient (inert: $N_2$ or reduction: $N_2/H_2$)
   - Vacuum
2. **Annealing –** *batch processing*
   - Atmospheric
   - Heating (300-400 $^oC$)
   - Duration (30-60 min)

# Blanket Cu Wafers Bonding (e-beam)




Cu wafer

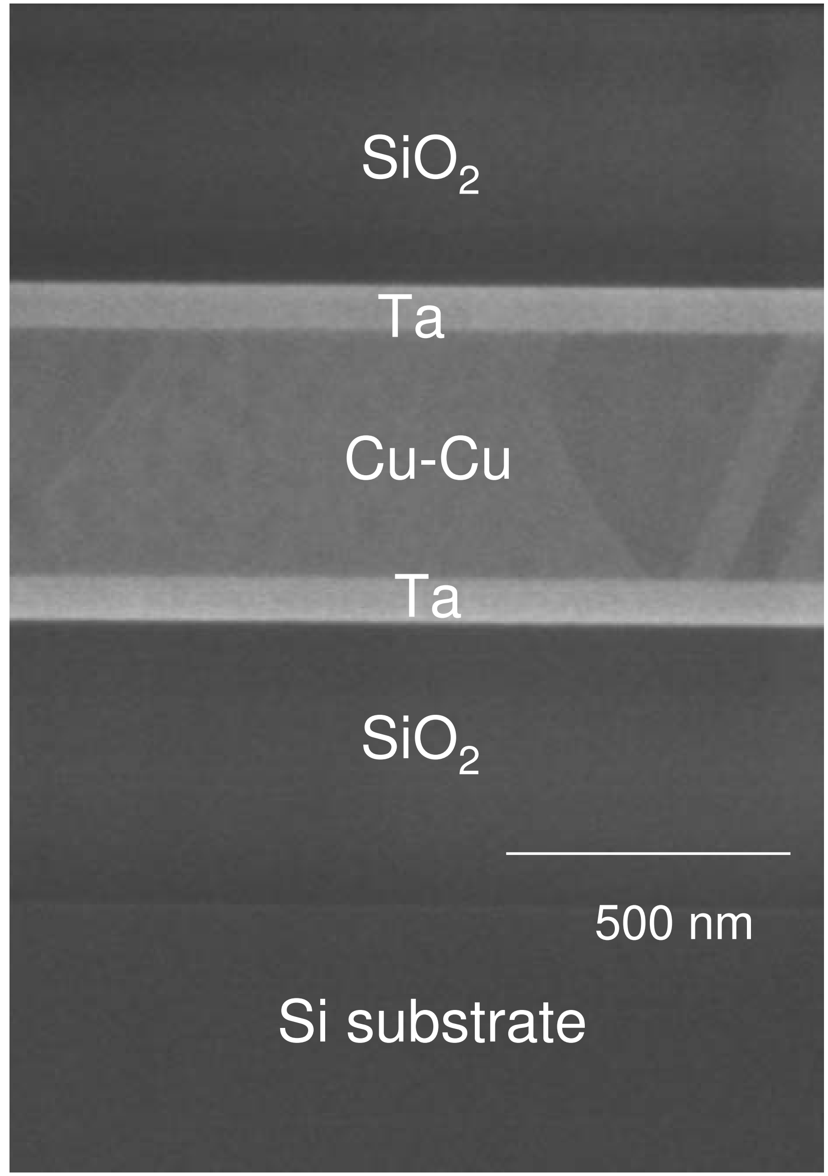
(RMS roughness = 1.99nm)

**Bonding**: 300 $^{o}$C / 1h

**Anneal**: 400 $^{o}$C / 1h

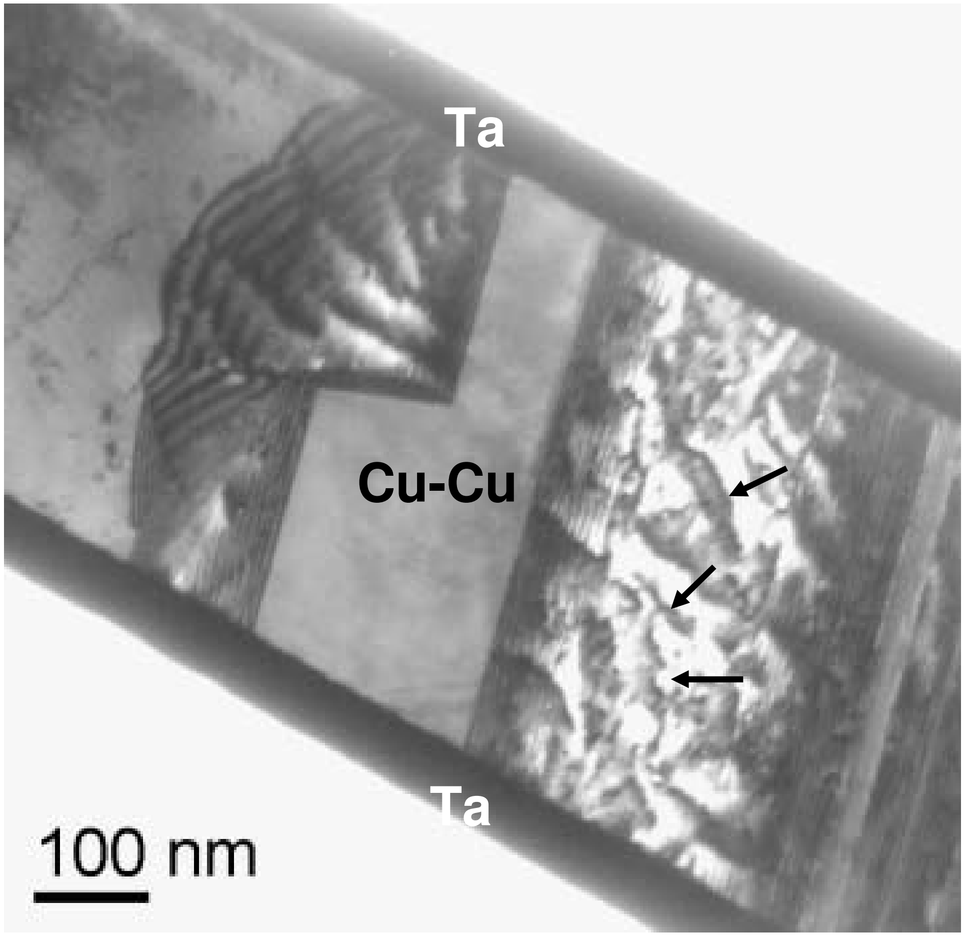
**Vacuum**: $10^{-2}$ - $10^{-3}$ Torr

**Pressure**: 4 kN / 6" wafer → 226 kPa, 2.3 Bar, 34 psi, 2.2 atm




Bonded Cu layer

# Cu Grain Structure in Bonded Layer

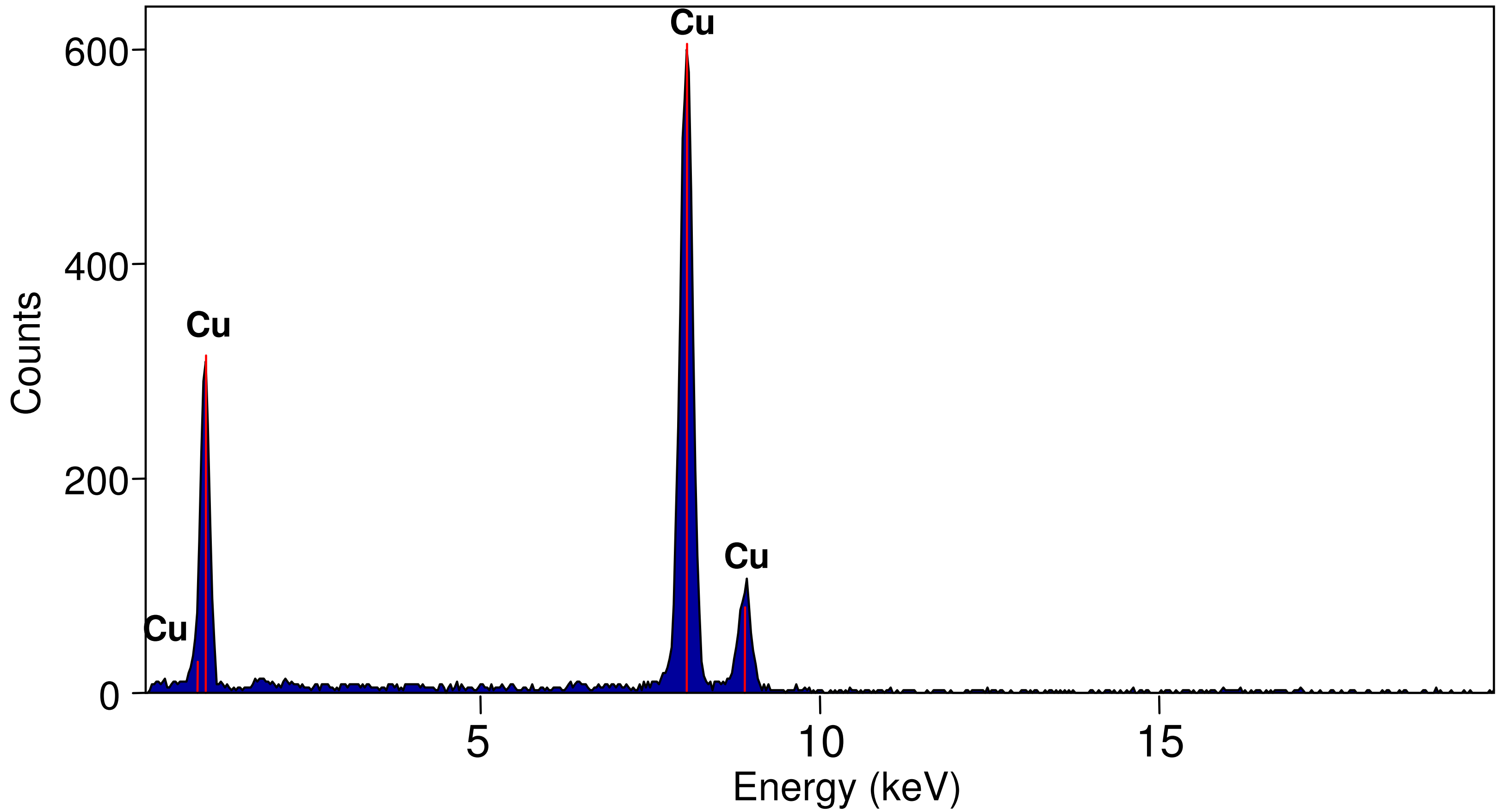



Original bonding interface disappears due to diffusion and grain growth. Cu layers merge and a homogeneous layer is obtained.

(300 $^{o}$C /1h + 400 $^{o}$C /1h )

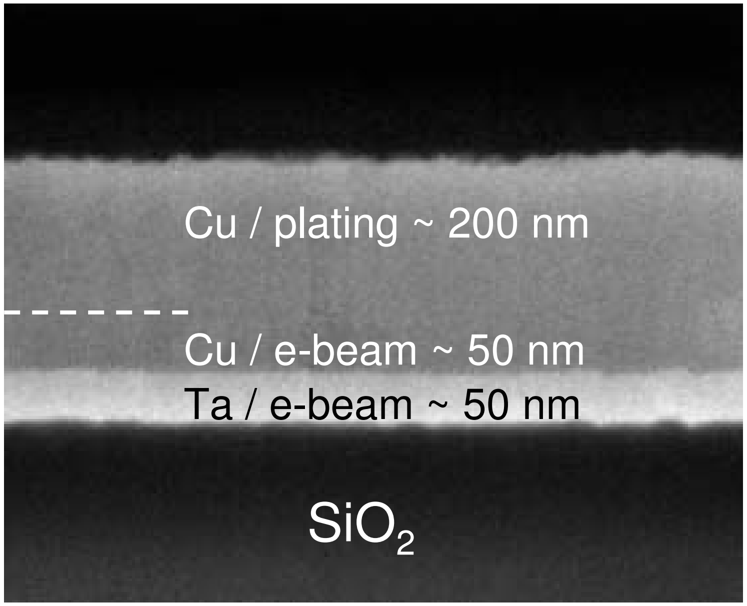
(Tan / TEM Credit: David Theodore, Freescale)

# EDS Analysis of Bonded Cu Layer



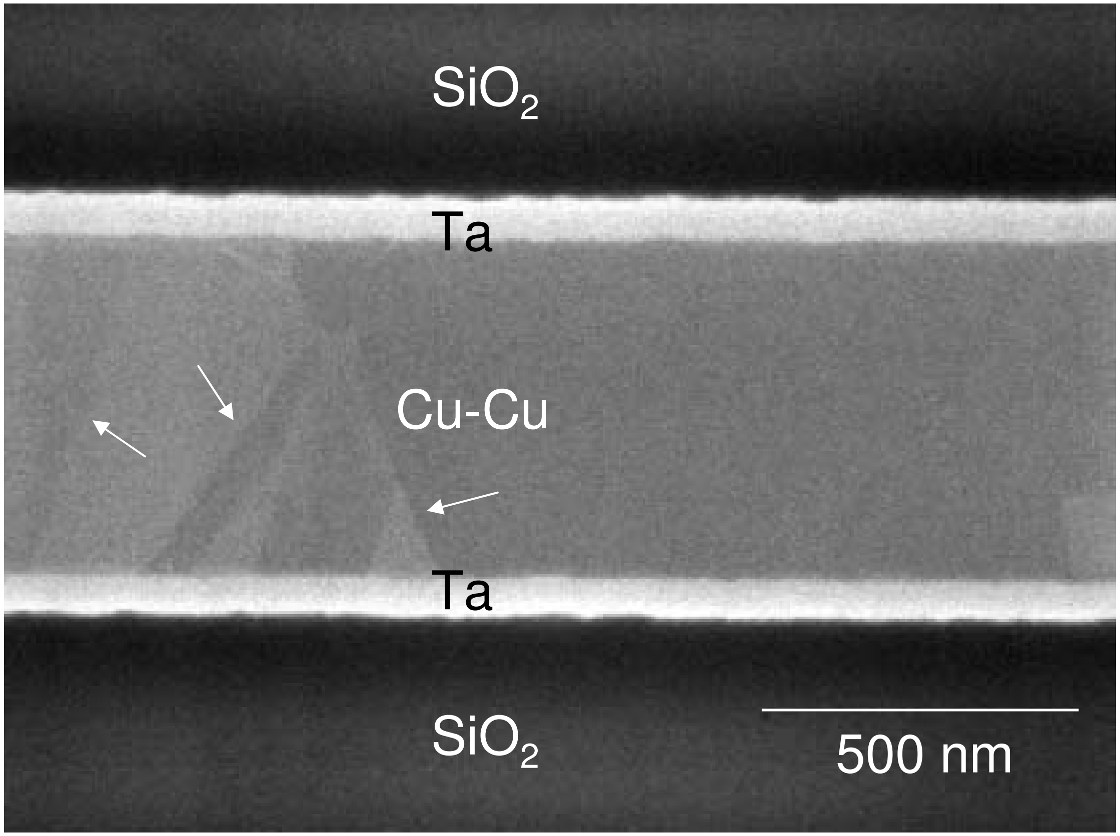

No observable contaminant in the bonded Cu layer.

# Blanket Cu Wafers Bonding (electroplating)



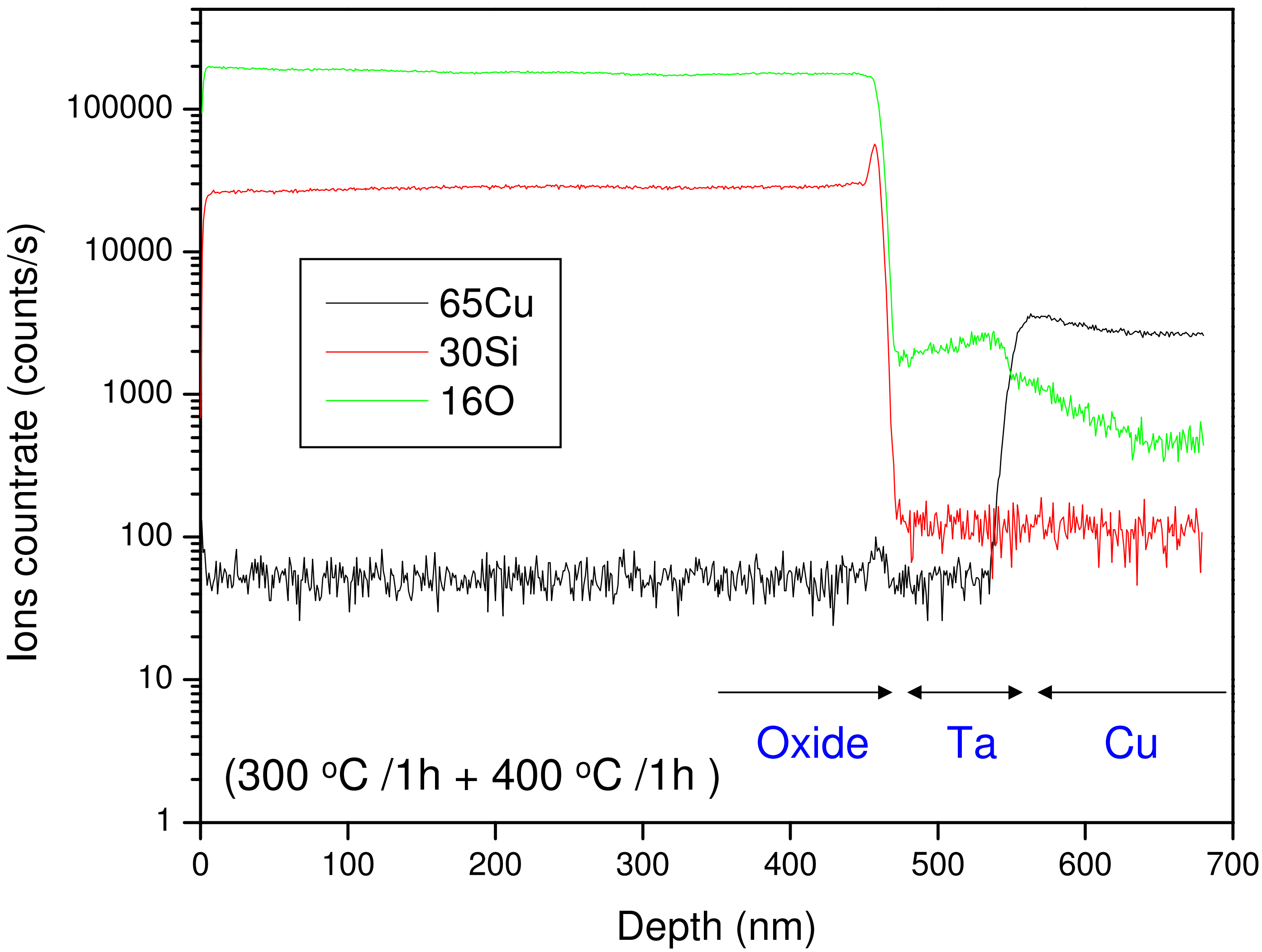

Cu wafer (*Credit: Joyce Wu*)

(300 °C /1h + 400 °C /1h )



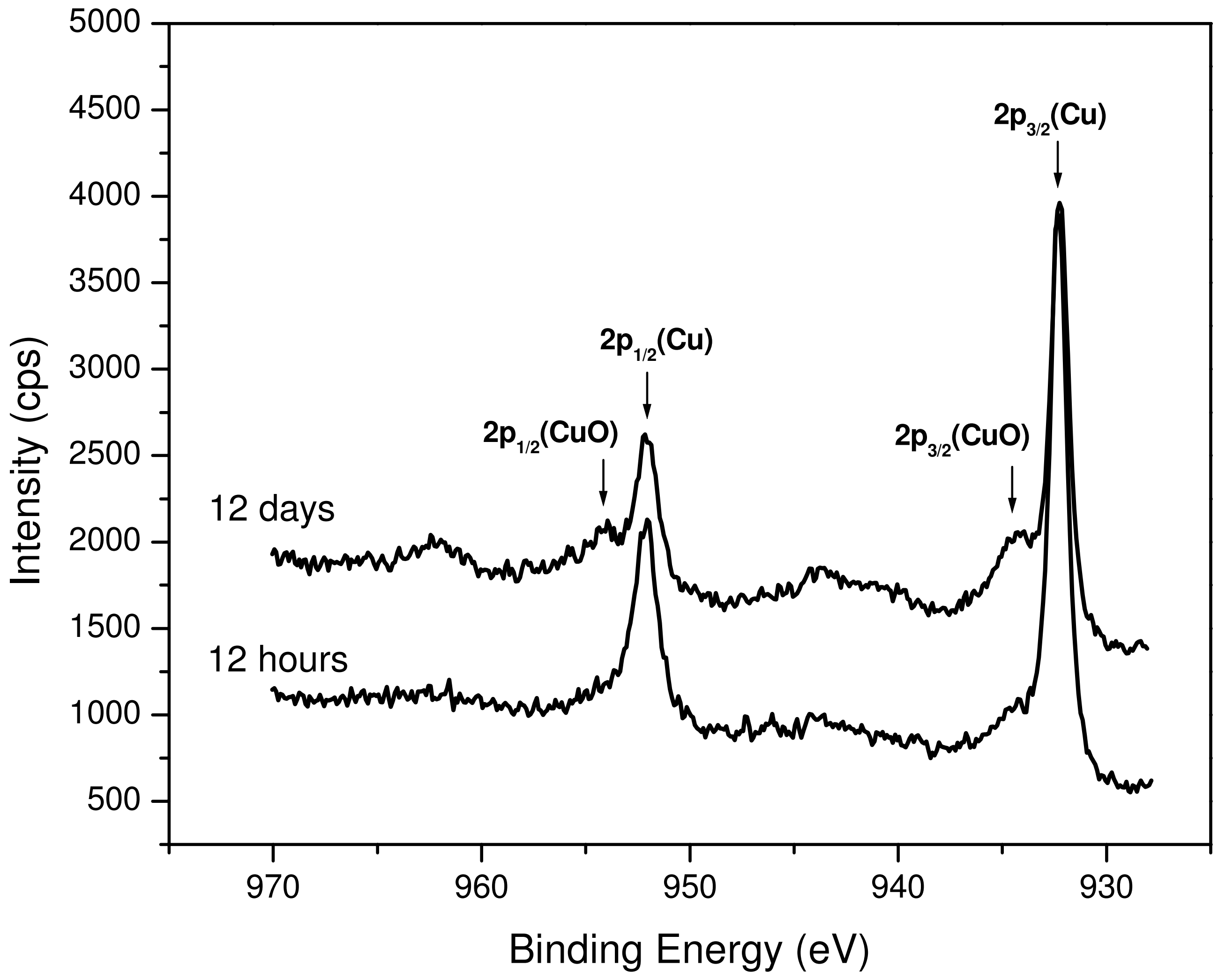

Bonded Cu layer

# Cu Out Diffusion




*No observable Cu out diffusion into the oxide layer, hence Ta acts as effective diffusion barrier during wafer bonding.*

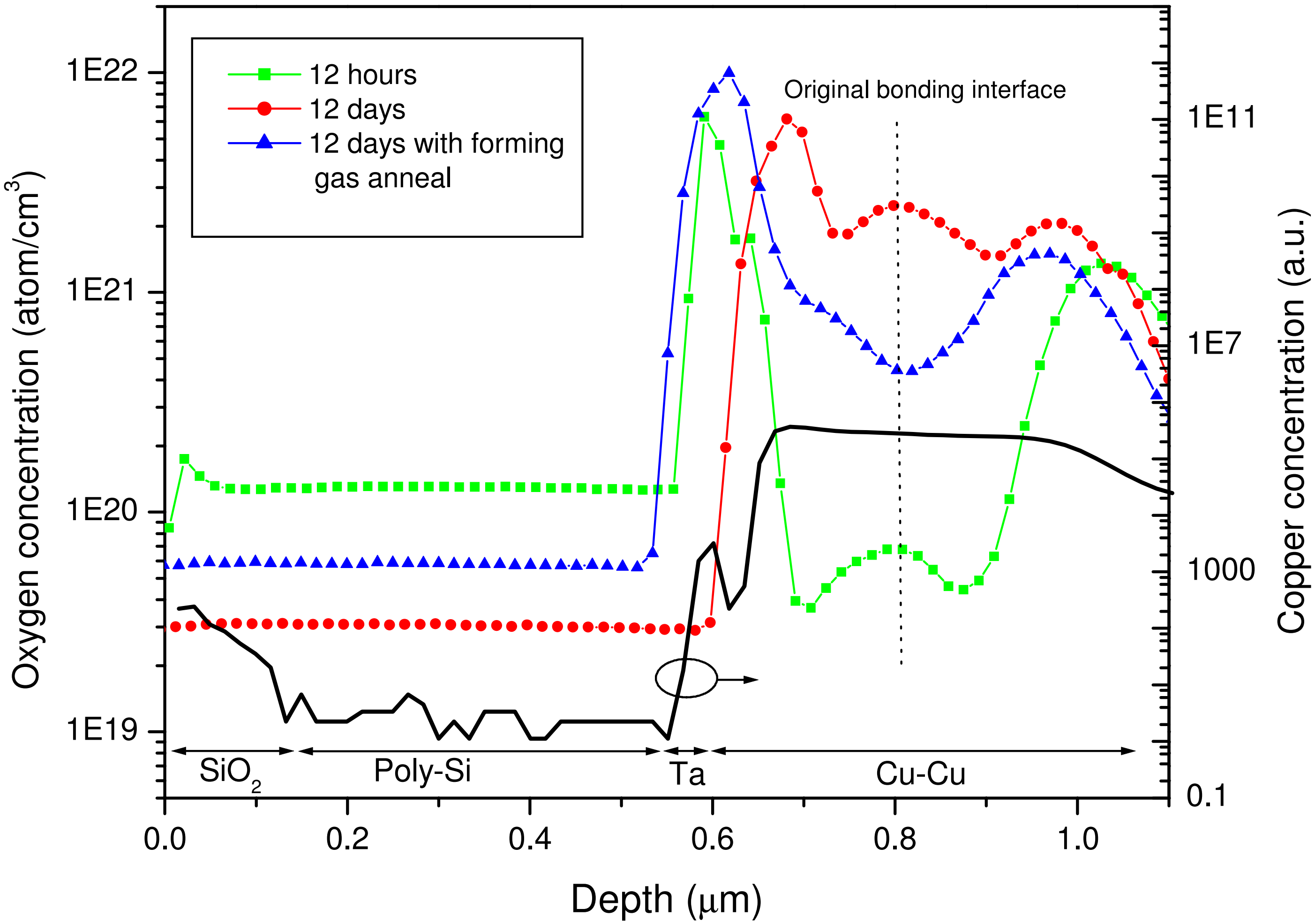
# Surface Oxide - Observation




Clear evidence of CuO formation after 12 days storage of Cu wafer in clean room (20°C, 40% humidity)

(Tan *et al., J. Electronic Materials, 34(12), 2005*)

# Surface Oxide - Treatment




Pre-bonding forming gas treatment: 95%$N_2$/5%$H_2$ at 150°C, 15 mins)

12 hours: *0.08 at %*
12 days: *2.96 at %*
12 days with forming gas anneal: *0.52 at %.*

(300 °C /1h + 400 °C /1h )

(Tan *et al., J. Electronic Materials, 34(12), 2005*)

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- ❑ **Reliability of Bonded Cu Layer**
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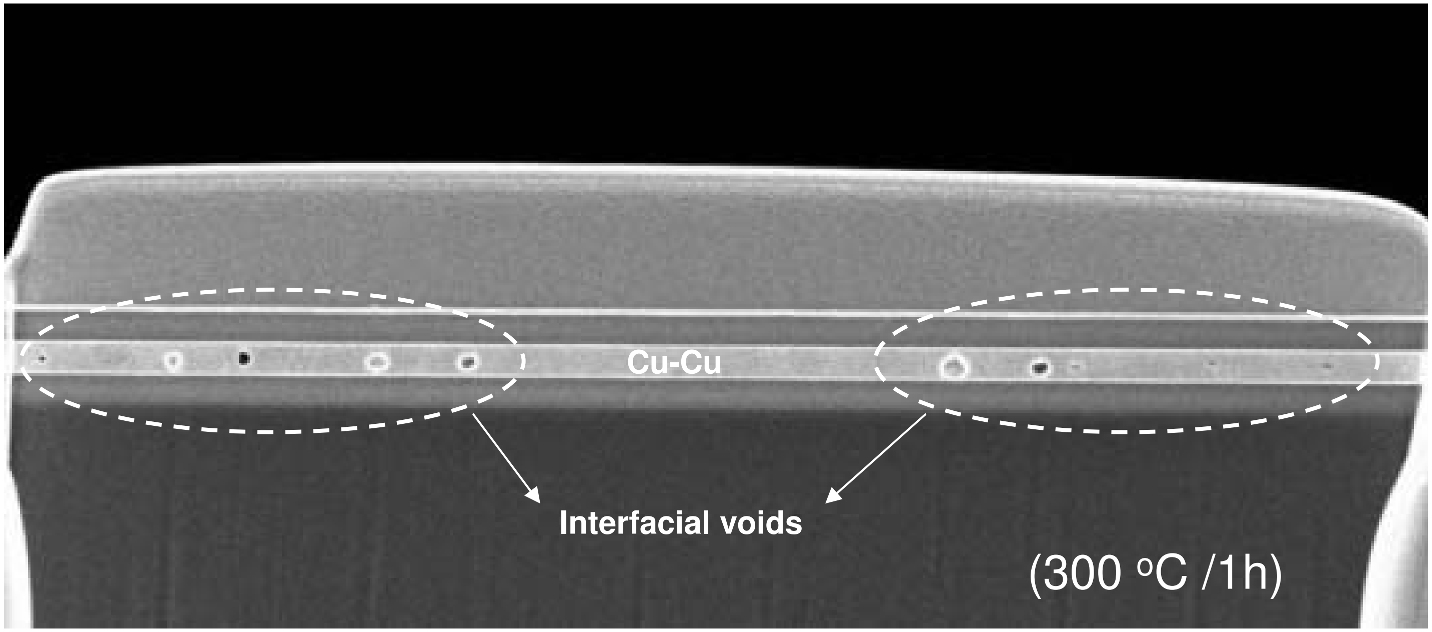
# Reliability of Bonded Cu Layer: Interfacial Voids Observation




**Interfacial voids**

→ *EM sites, increased resistance, open failure*

→ *structural integrity*

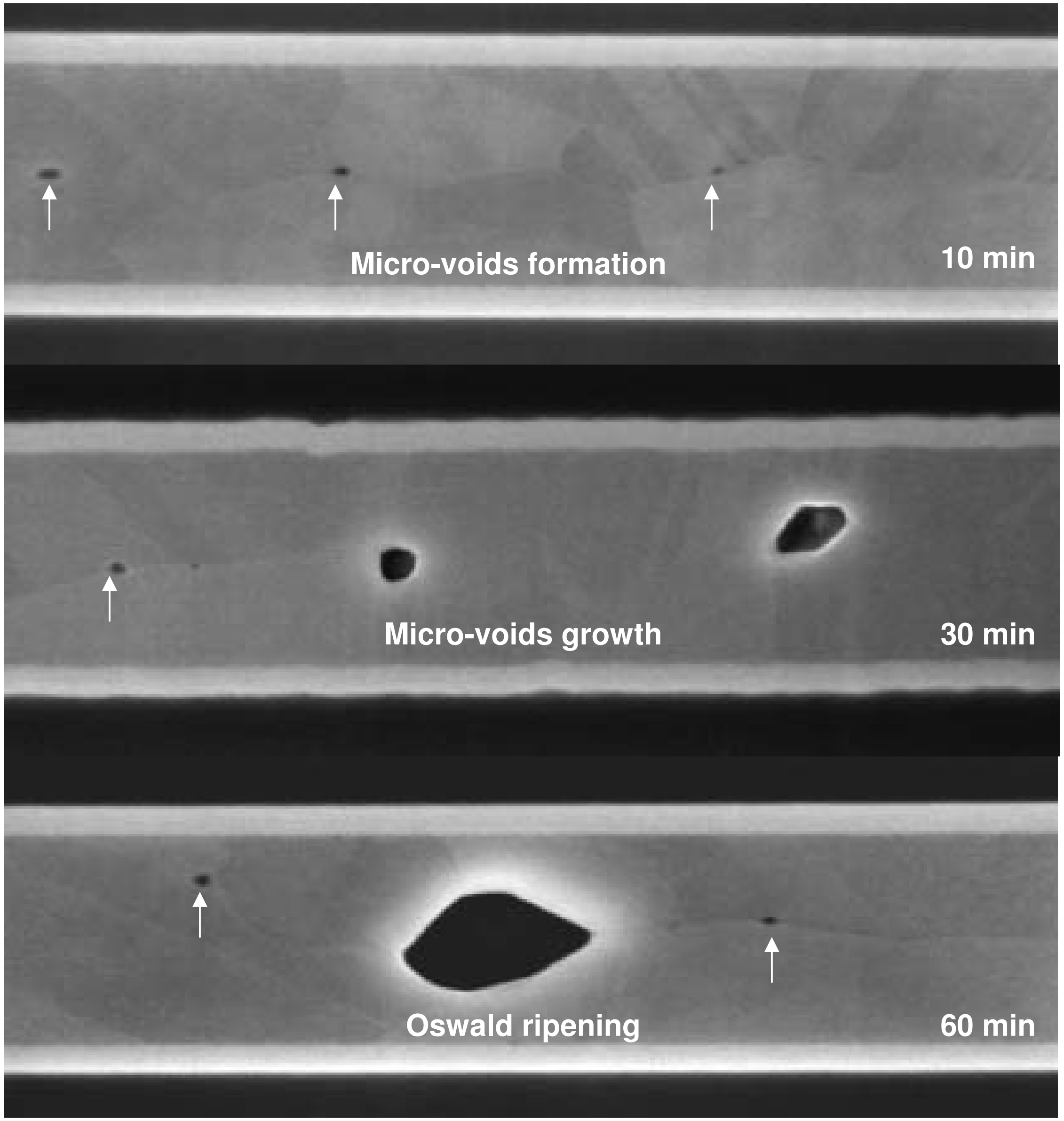
(Tan *et al.*, APL, 87(20), 2005)

# Voids nucleation and growth

(a)

(b)

(c)




(300 $^{o}$C)

**Nucleation:**

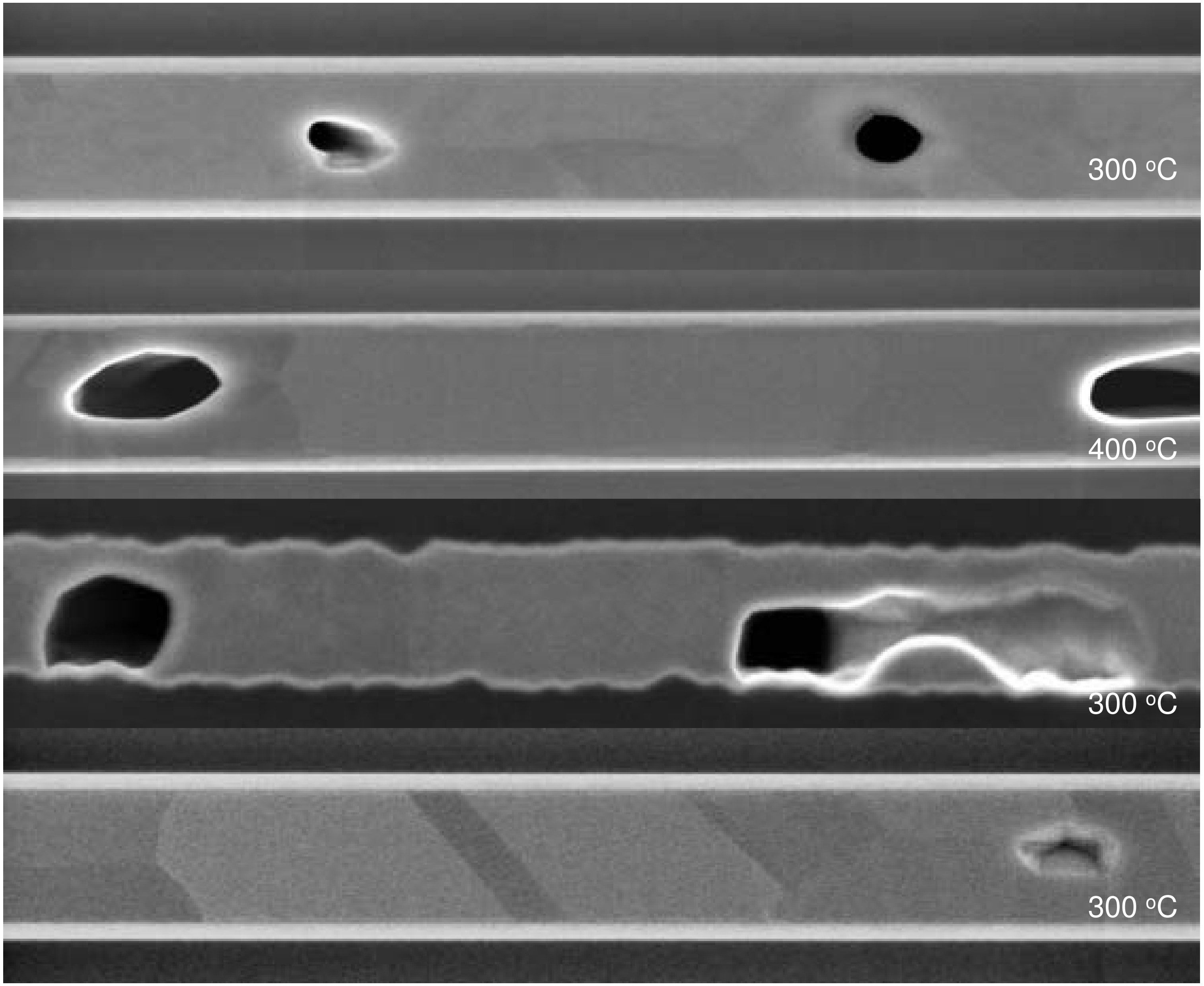
- bonding interface irregularities
- surface contamination

**Growth:**

- grain boundaries diffusion
- vacancies annihilation
- stress gradient

# Counter-Measures

(a)
(b)
(c)
(d)




Surface roughness (1.99 nm)

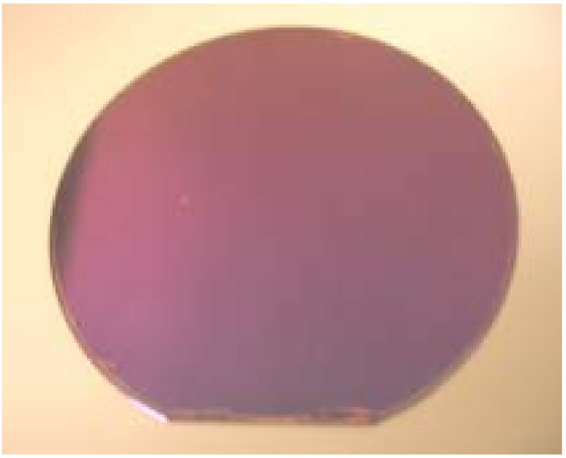
Bonding temperature

Surface roughness (8.59nm)

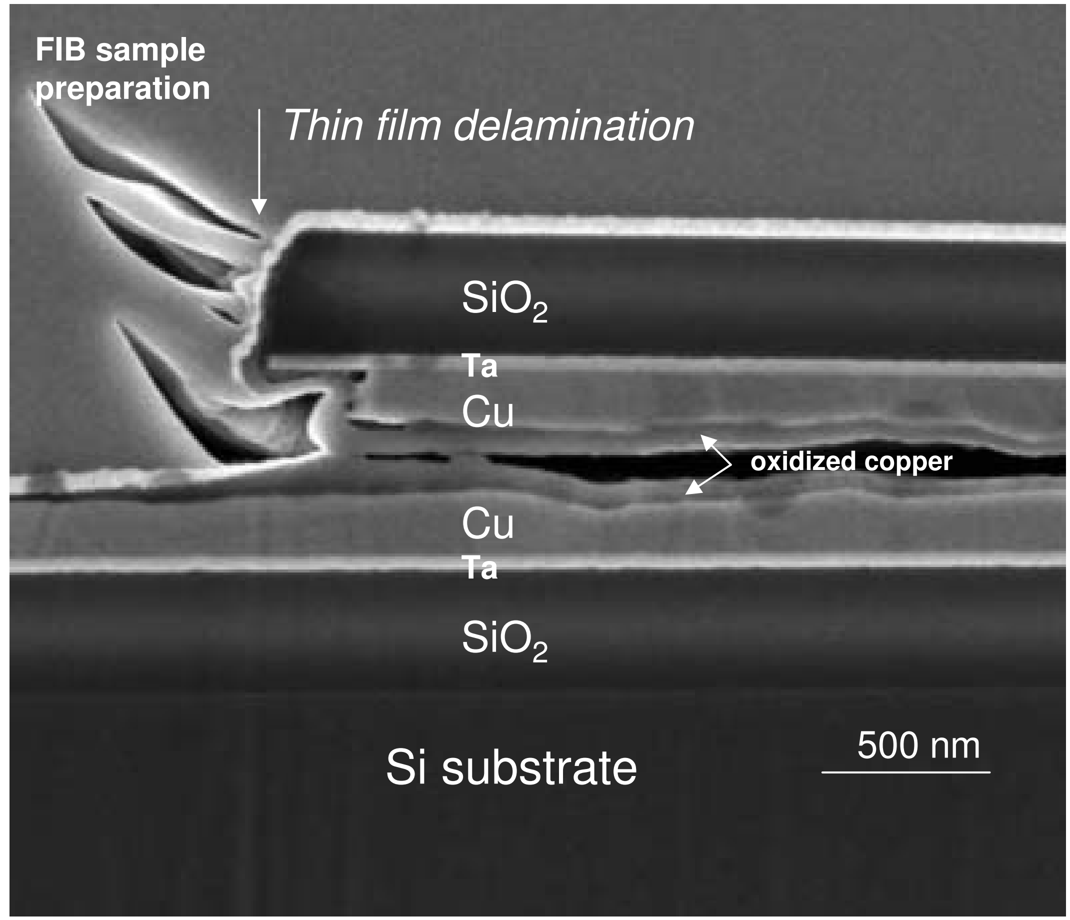
Pre-bonding anneal ($N_2$, 100 °C, 30 min)

# Bonding Uniformity and Films Delamination

(a)



(b)

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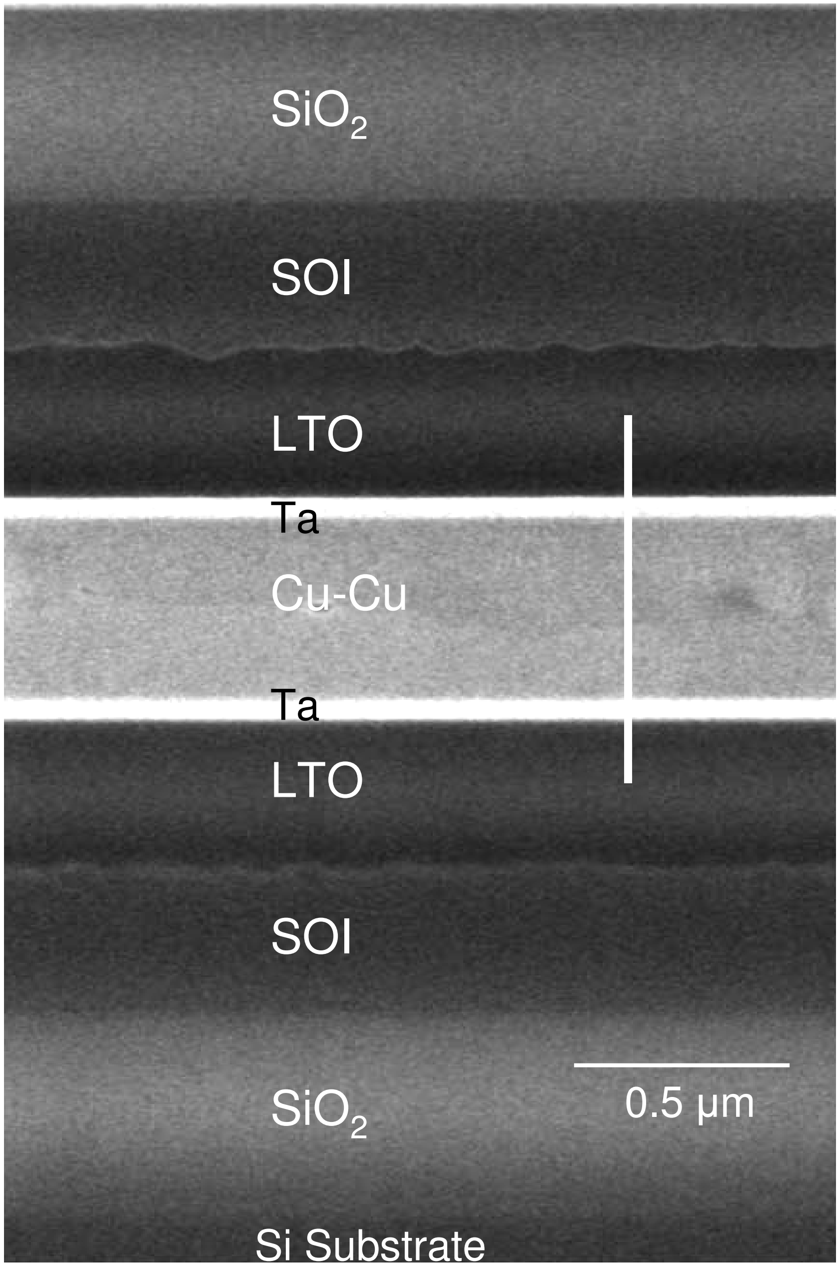
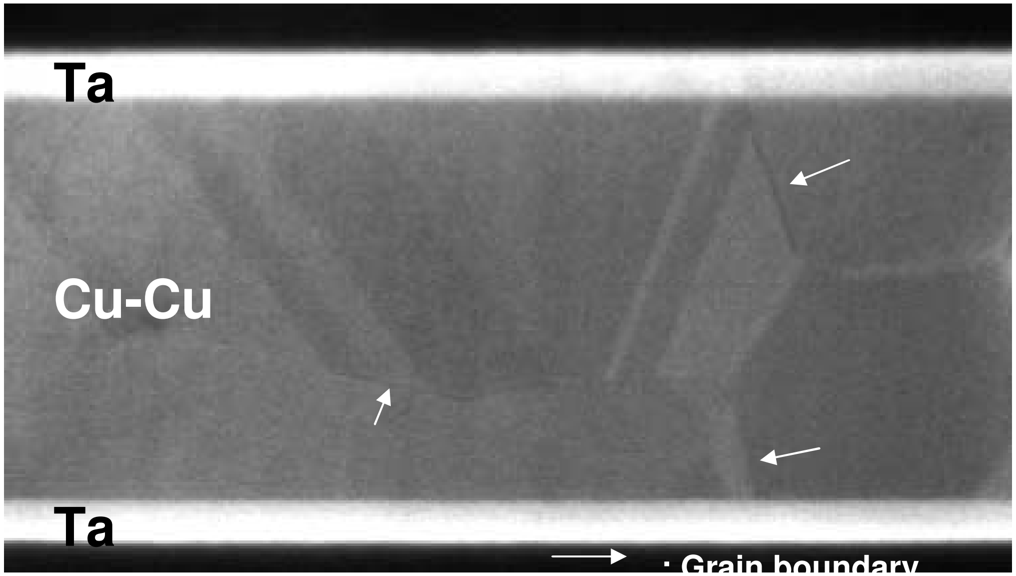
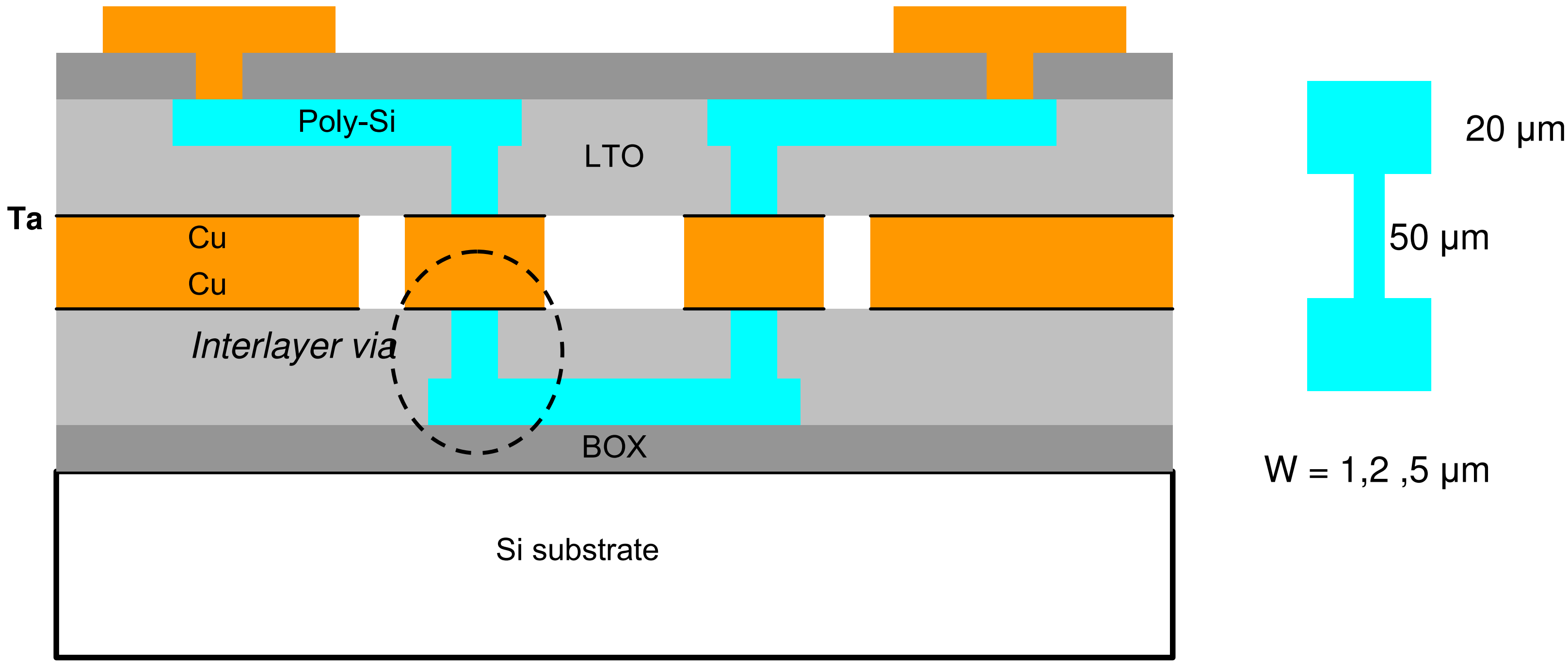
# Face-to-Face Bi-layer Stack

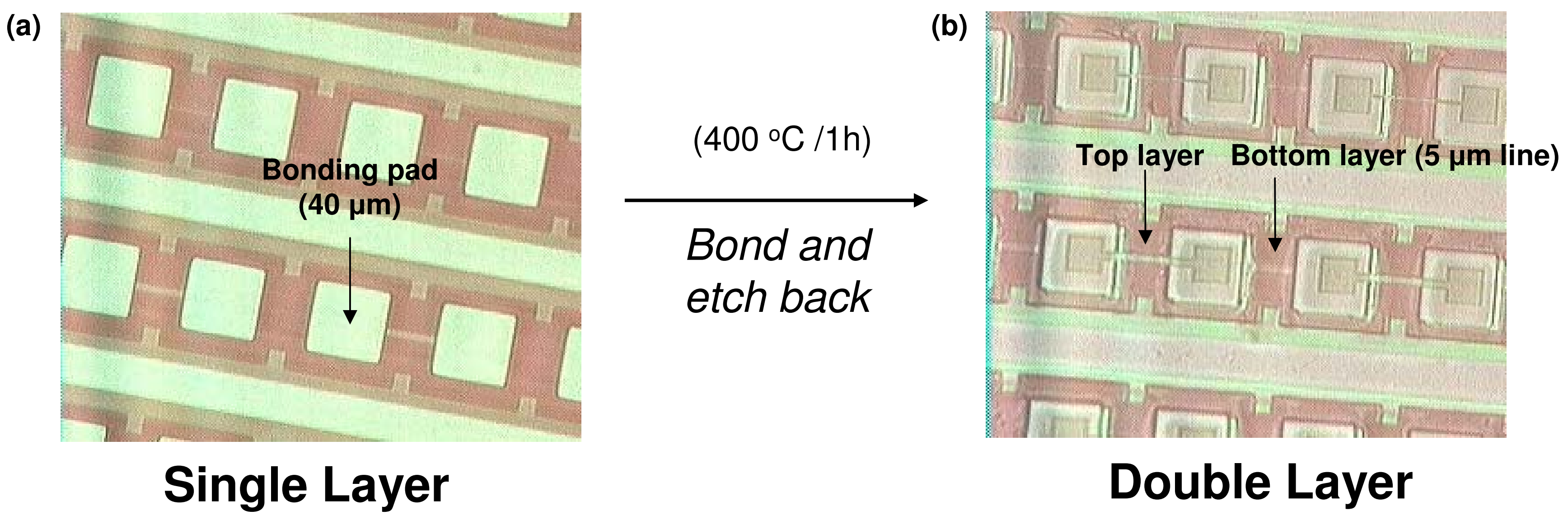



(400/1 + 400/1, with CMP)

# Poly-Silicon Resistors 'Daisy Chain'

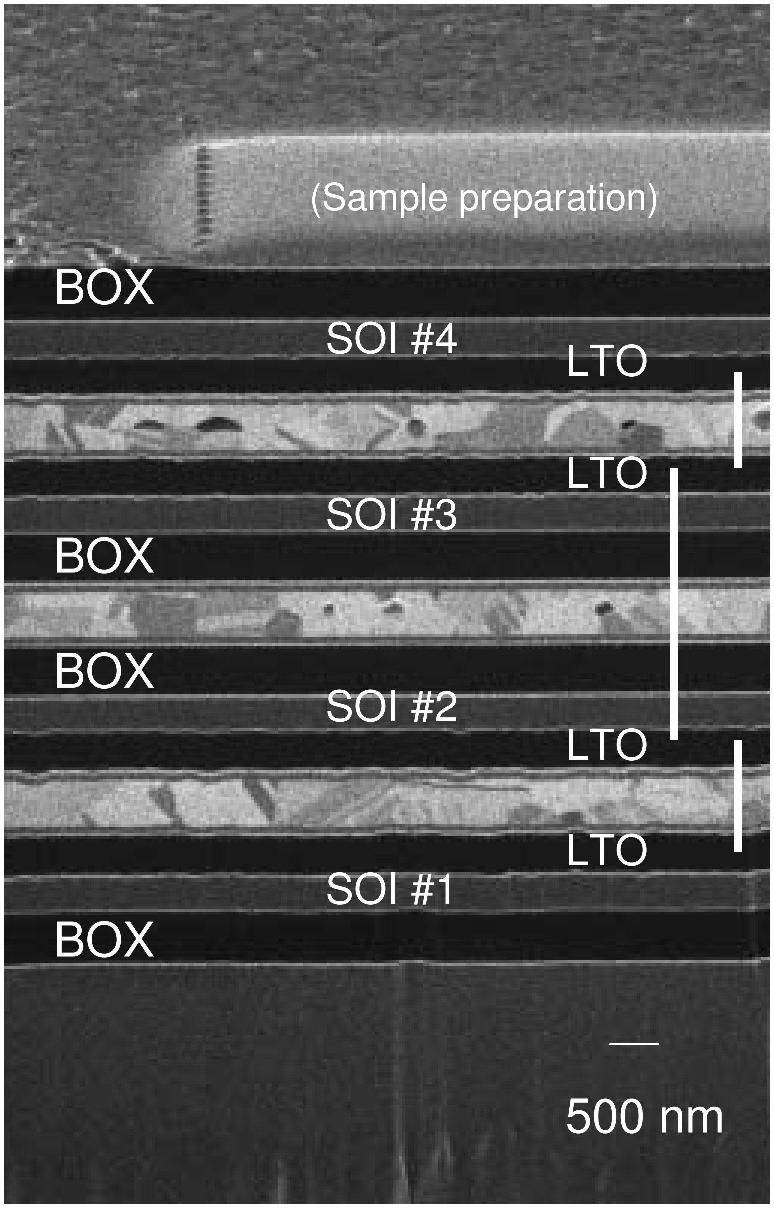


# Silicon Four-Layer Stack

2nd double-layer stack

1st double-layer stack



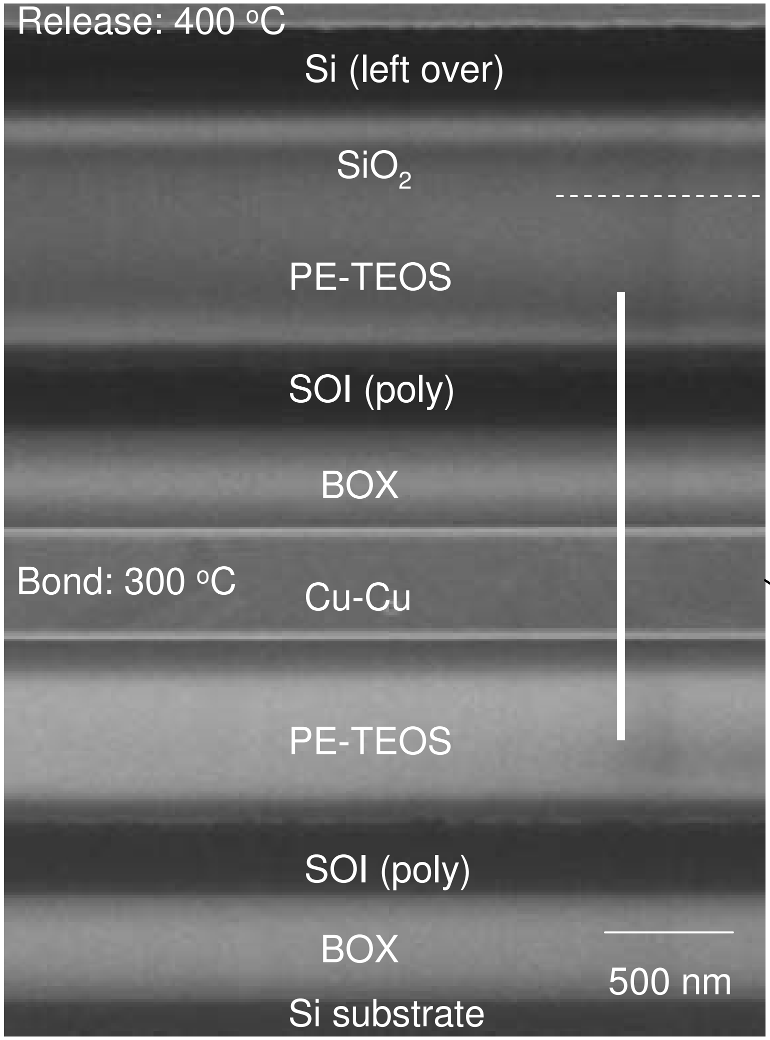

Face-to-Face

Back-to-Back

Face-to-Face

(Tan *et al.*, *Electrochem. Solid-State Lett.*, 8(6), 2005)

# Back-to-Face Bi-layer Stack




(300 °C/1h + 400 °C /1h)

(Tan *et al.*, SOI Conference, 2005)

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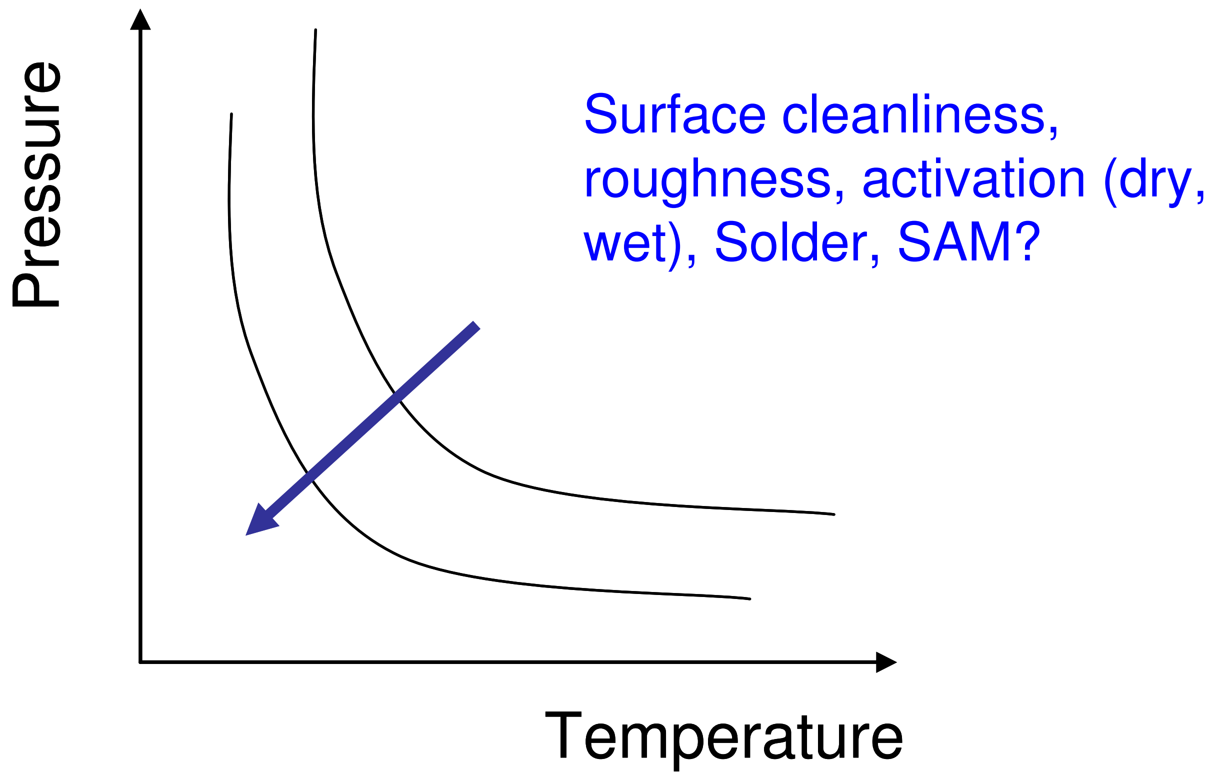
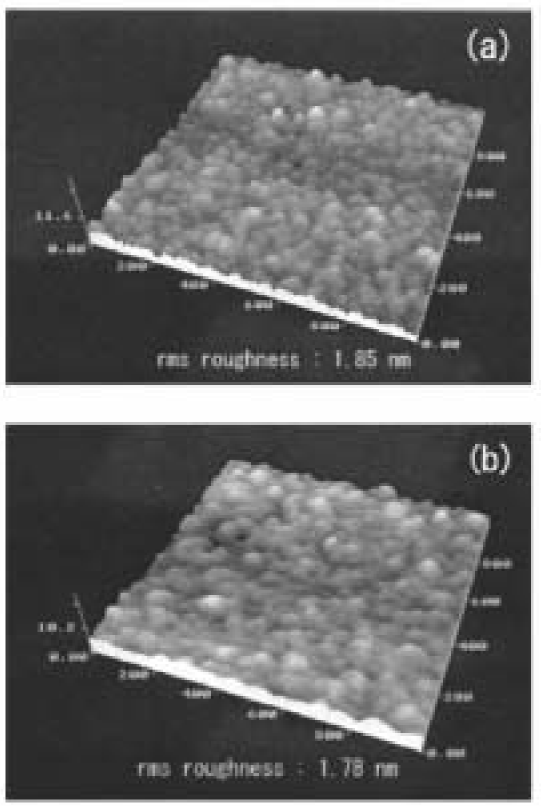
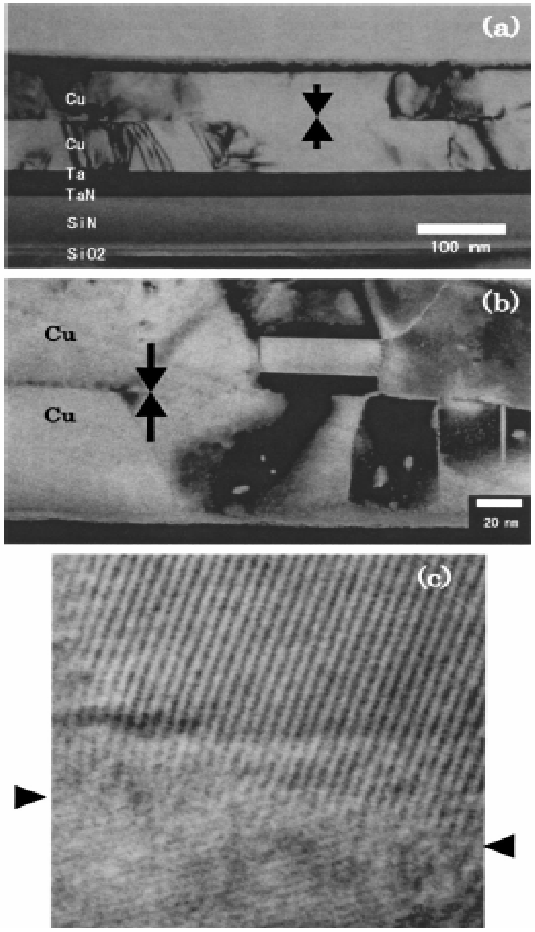
# Low Temperature Bonding



# Low Temperature Bonding – Surface Activated Bonding



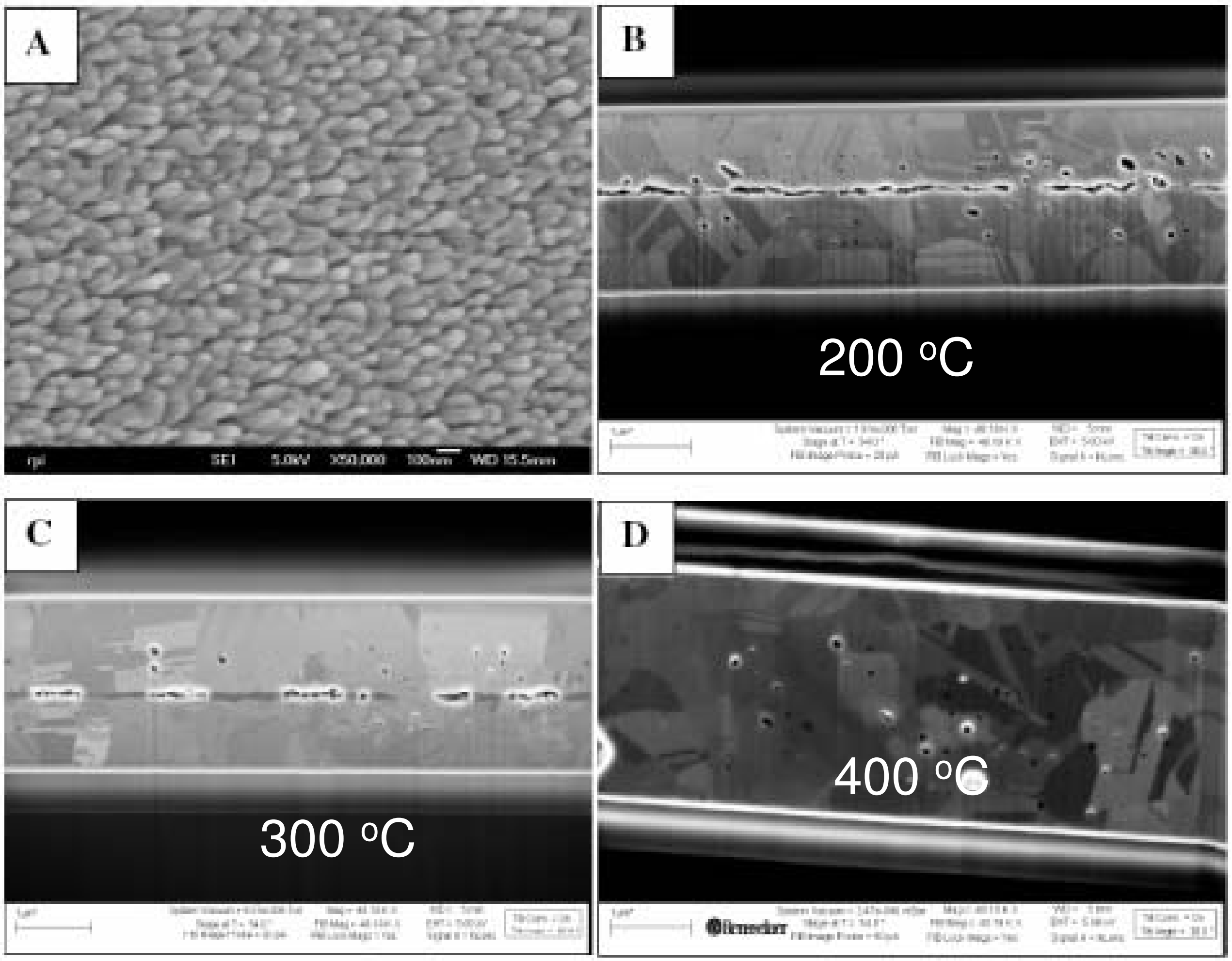




Ar ion beam activation (40-100 eV, 60 s) – surface contaminant and oxide removal, roughness improvement

Bonding in UHV condition – no annealing. Bond strength > 6.47 MPa.

(Kim et al, JVST A, 2003)

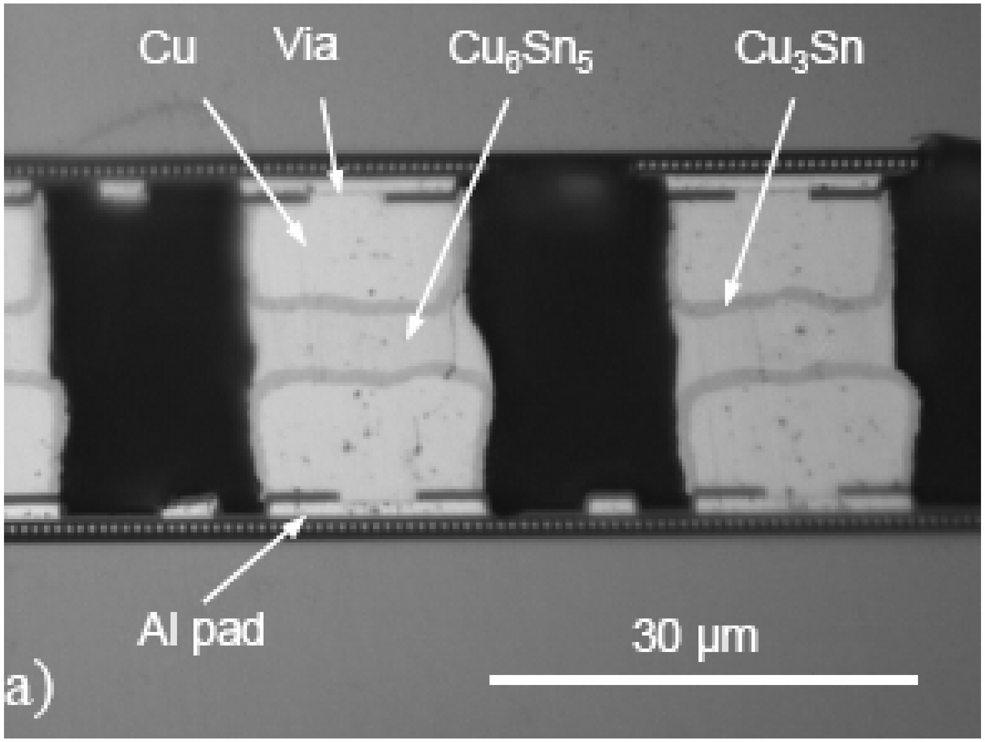
# Low Temperature Bonding – Cu Nano-rod (RPI)




- Cu nano-rod achieved with 85° angle deposition in e-beam. Diameter = 50 nm, Length=760nm;
- Bonding pressure: 0.32 MPa;
- Observation: Cu nano-rod arrays fuse together accompanying by grain growth at temperature as low as 200 °C.

(Wang et al, MRS, Fall 2006)

# Solid Liquid Inter-diffusion Bonding (SLID)




- Cu (high melting T) / Sn (low melting T, 232°C);
- **Reflow**, slightly higher than 232 °C → Cu6Sn5;
- **Curing**: Cu6Sn5 + Cu → Cu3Sn (stable up to 600 °C)
- Resistivity: Cu<Cu3Sn<Sn<Cu6Sn5

(Munding et al)

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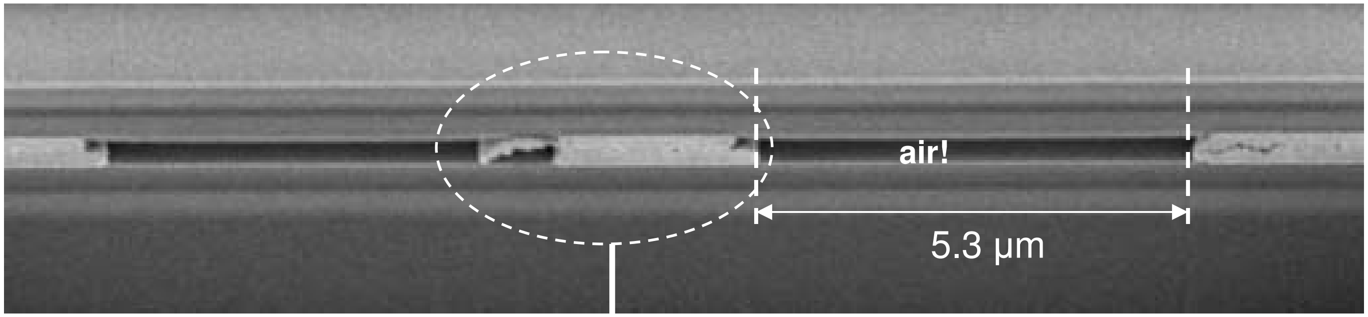
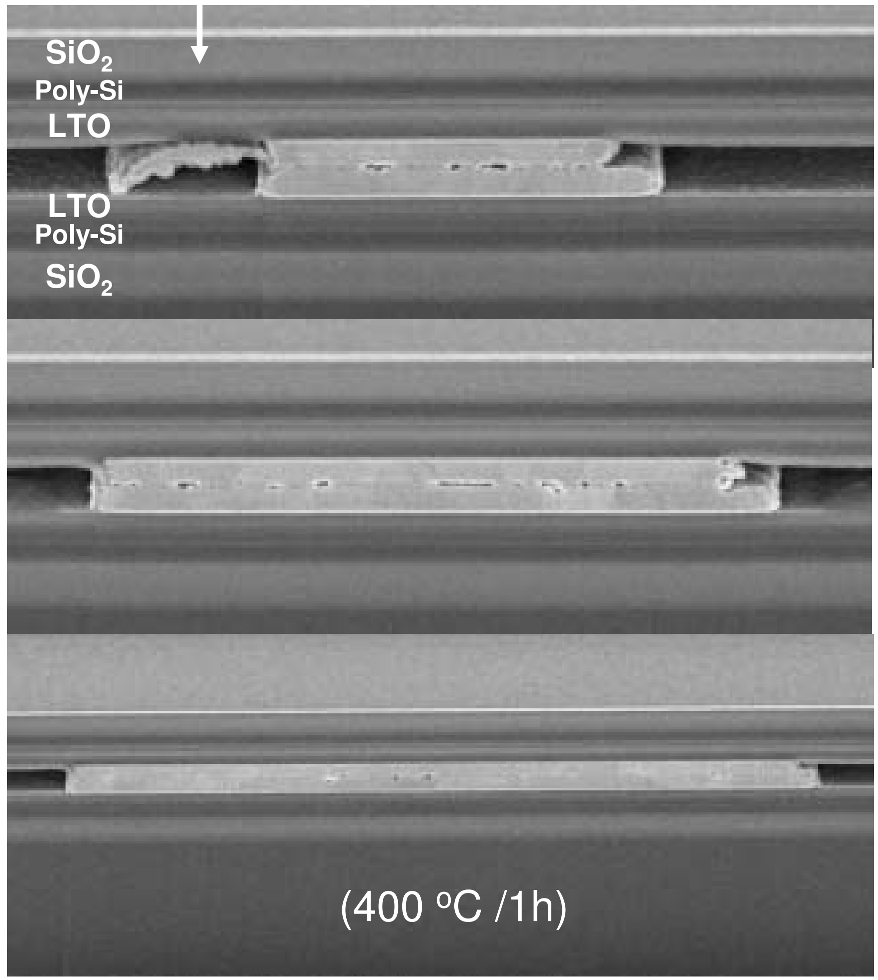
# Cu Line-Line Bonding (and pad-pad bonding for that matter)



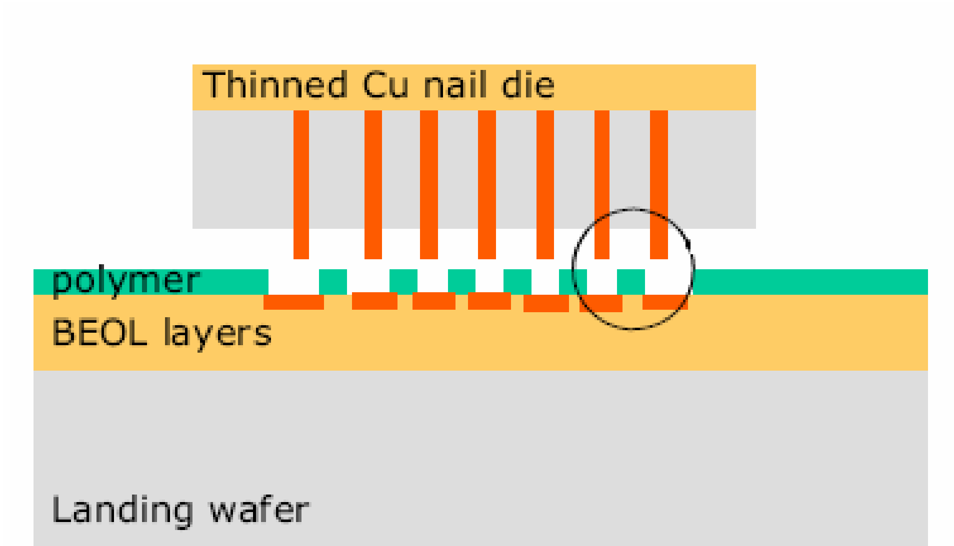

2.0 µm

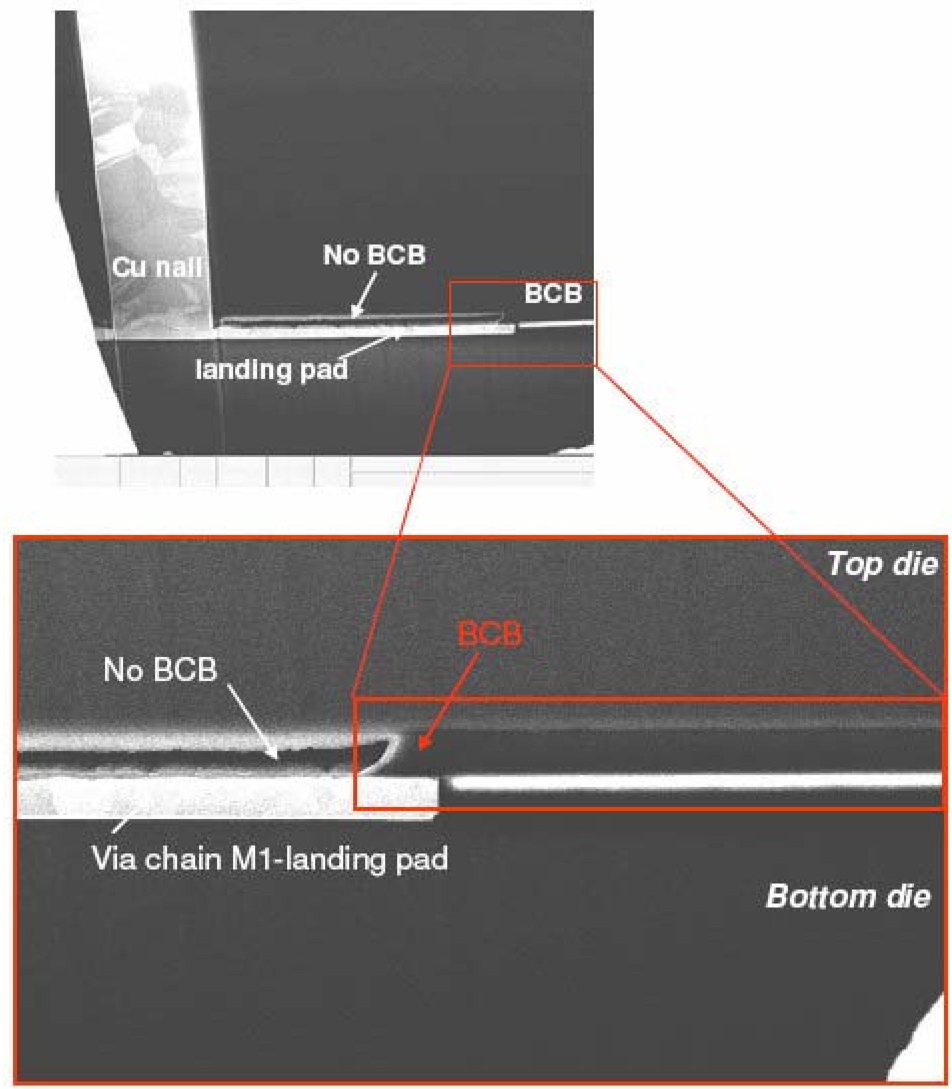
4.1 µm

9.2 µm

- Misalignment < 0.5 µm
- Interfacial voids
- Thin films integrity

# Cu/BCB Hybrid (IMEC)

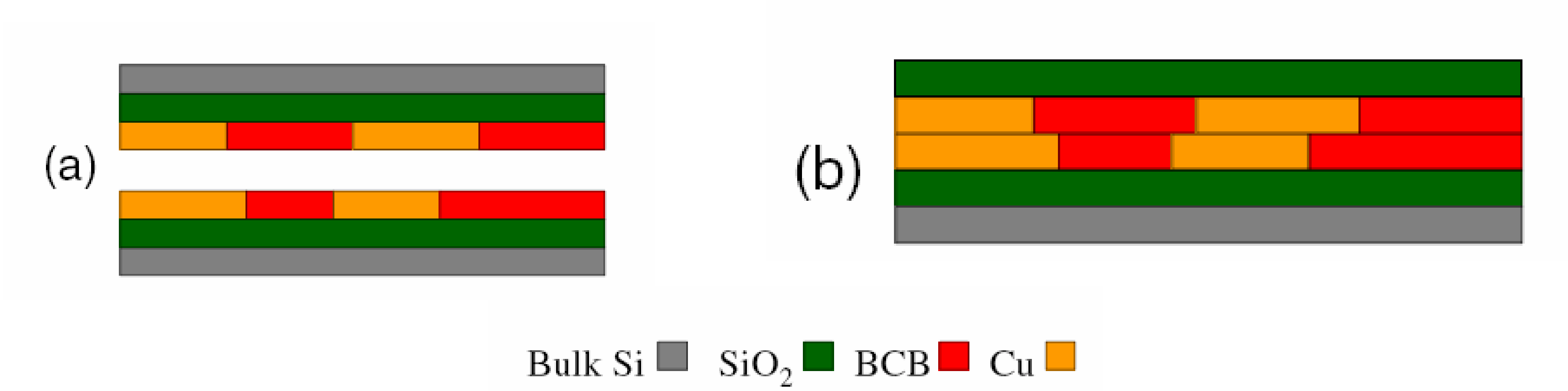


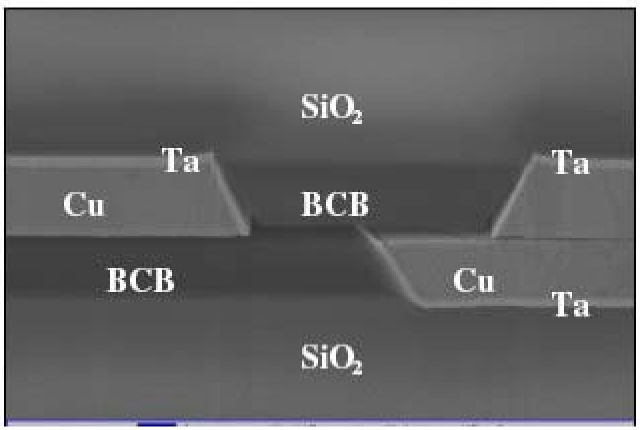




- Chip (Cu nails) to wafer (landing pads)
- Bond #1: BCB-Si + BCB Reflow at 100-150 °C
- Bond #2: Cu-Cu thermo-compression at 300-350 °C.

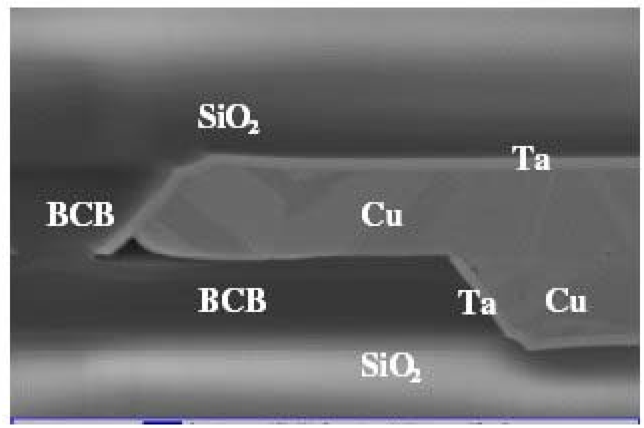
(Jourdain et al, IITC 2007)

# Damascene-Patterned Cu/BCB Hybrid (RPI)



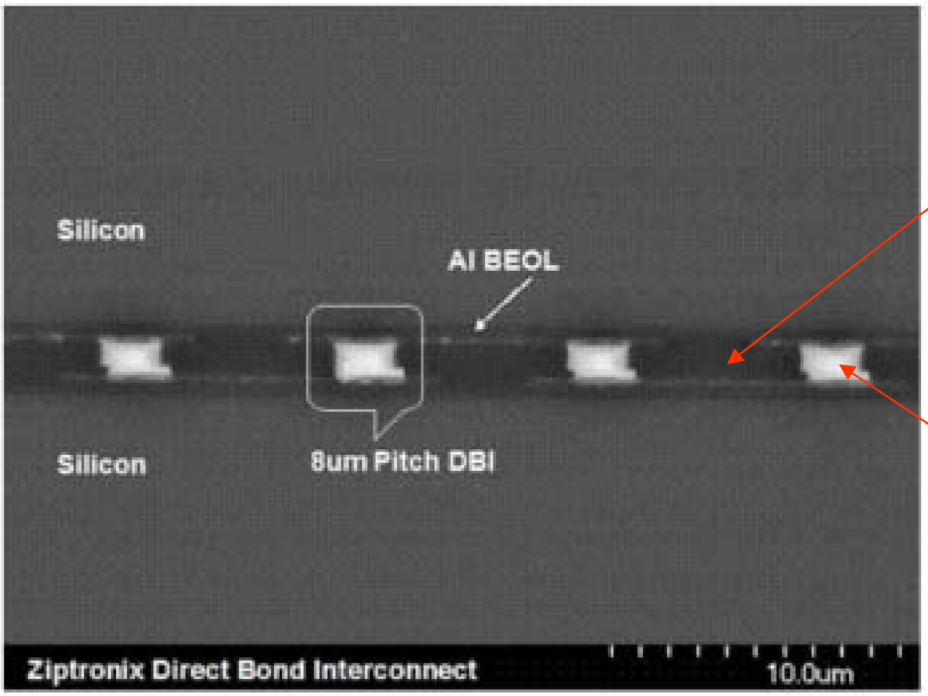

250$^o$C




250$^o$C / 350$^o$C

(Gutmann et al, MRS Fall 2006)

# Cu/Oxide - Direct Bond Interconnect (DBI™)




Scanning Electron Micrograph of 4 serial links in a DBI™ daisy chain.

#1 Low temperature oxide-oxide bond

#2 Cu-Cu bond formed as a result of CTE mismatch between oxide and Cu during annealing

Ziptronix

(Enquist et al, MRS, Fall 2006)

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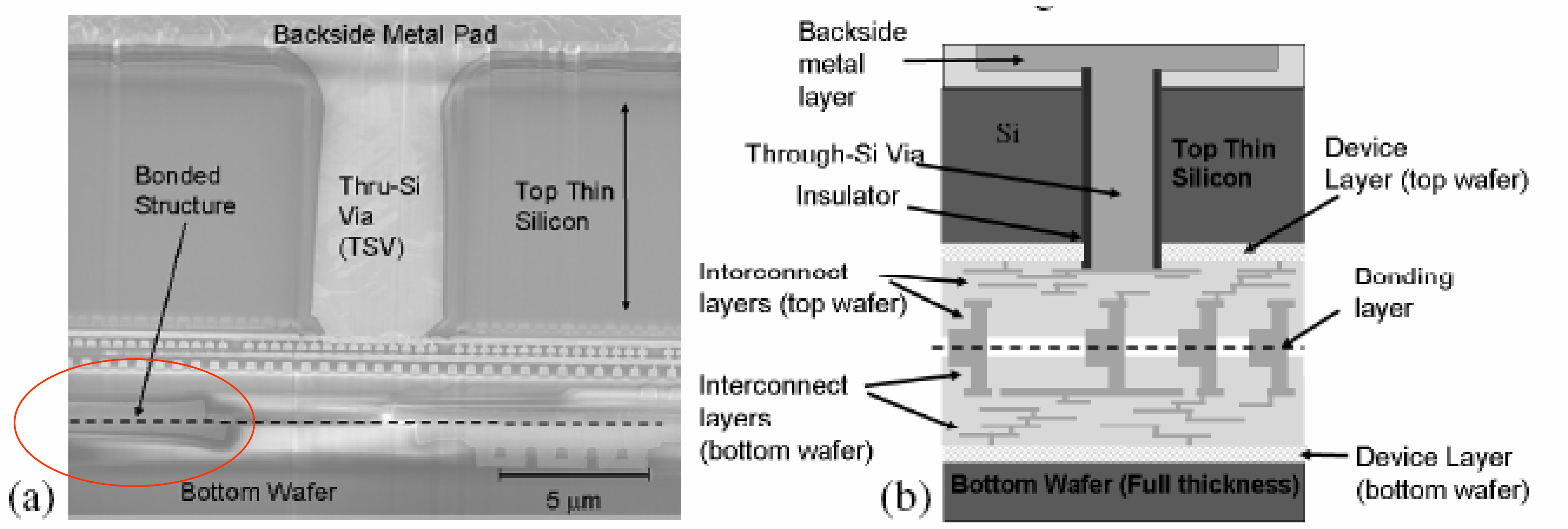
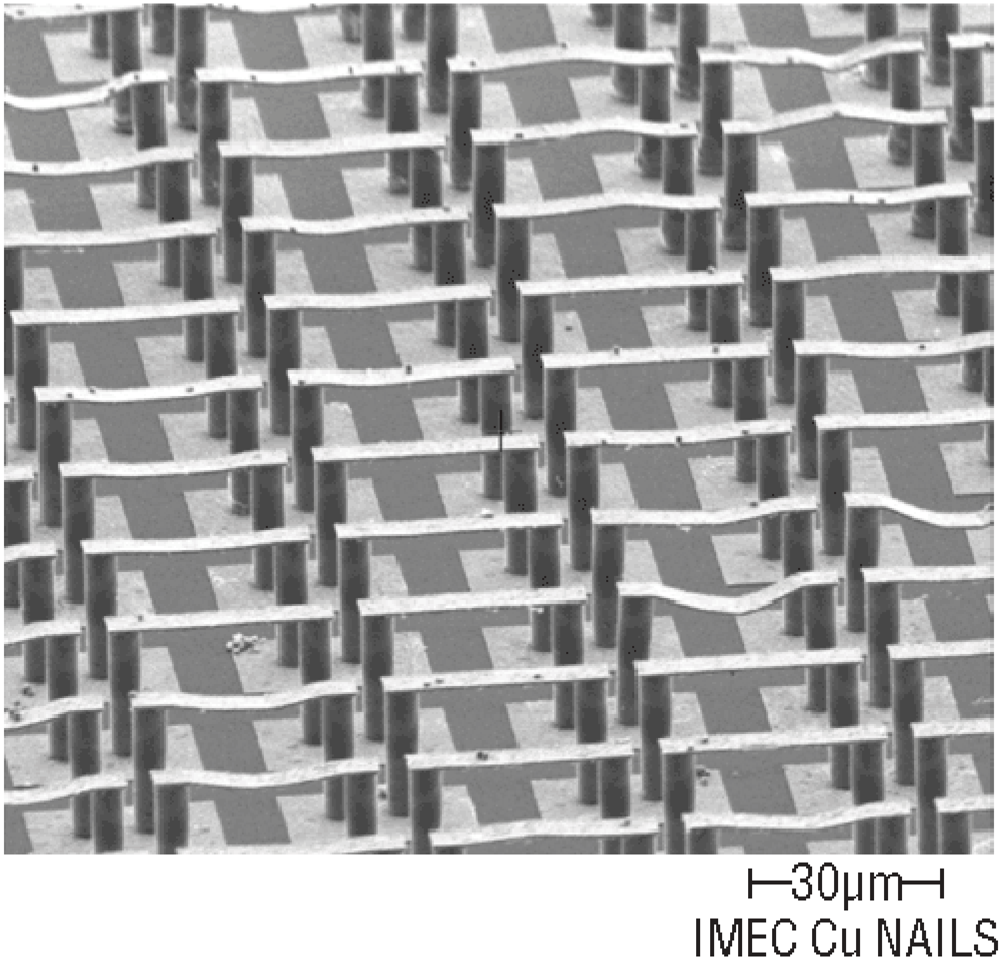
# Intel




Logic + Memory, Logic + Logic

(Morrow et al, EDL 2006, MRS Fall 2006)

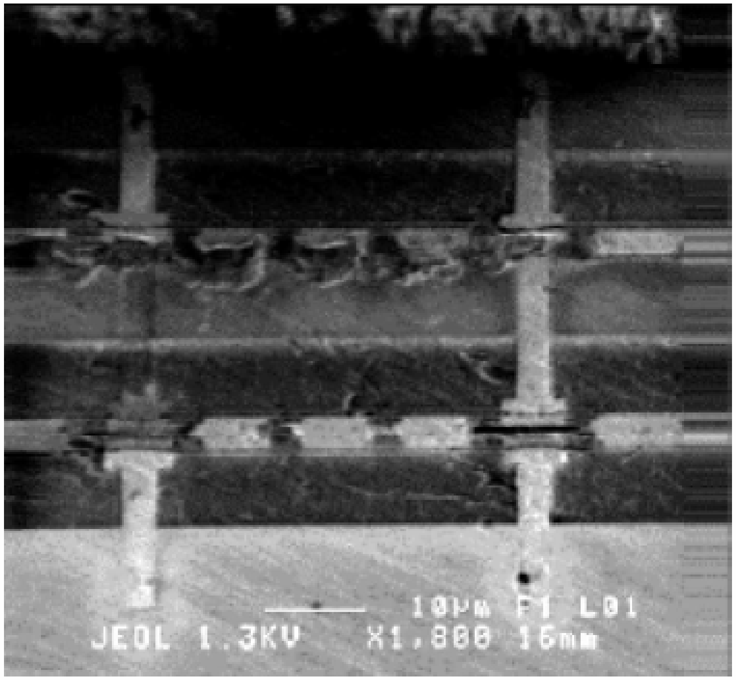
# IMEC



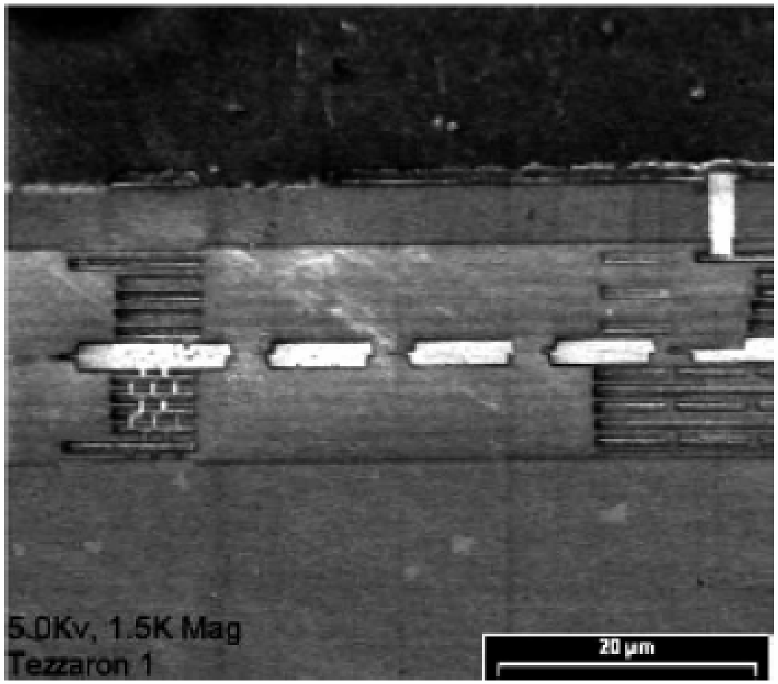

(Swinnen et al, IEDM 2006)

- Cu nails
- Diameter=5um, Height=24um
- 10K/mm$^2$

# Tezzaron




First generation “super-via”




Second generation “super-contact”

(Patti et al, Proceeding of IEEE, 2006)

## Thank You!